POWER SWITCHING REGULATORS

DESIGNER's BOOKLET

1st EDITION

SEPTEMBER 1993

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2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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SELECTION GUIDE

BCD HIGH CURRENT SWITCHING REGULATORS						
PARAMETER	**L4970A**	**L4977A**	**L4975A**	**L4974A**	**L4972A**	**L4972AD**
Max. Input Op. Voltage	50V	50V	50V	50V	50V	50V
Output Voltage Range	5.1V to 40V ±2% (Internal Reference)					
Max. Output Current	10A	7A	5A	3.5A	2A	2A
Power Switch	DMOS R_{DSON} 0.1Ω (Typ.)					
Switch Mode Control System	Continuous Mode, Direct Duty Cycle Control with Feed Forward (Improved Transient Response)					
Chopping Frequency	500kHz	500kHz	500kHz	200kHz	200kHz	200kHz
Efficiency V_{IN} = 35V V_O = 5.1V 100kHz	10A 83%	7A 84%	5A 84%	3.5A 84%	2A 83%	2A 83%
Current Limiting	True Current Generator					
Soft Start	Yes					
Reset and Power Fail	Yes					
Crowbar	Yes					
Package	Multiwatt15	Multiwatt15	Multiwatt15	Powerdip 16+2+2	Powerdip 16+2+2	SO20 16+2+2
Max. $R_{thj\text{-}case\ (PIN)}$	3°C/W	3°C/W	3°C/W	12°C/W	12°C/W	15°C/W

BIPOLAR HIGH CURRENT SWITCHING REGULATORS						
PARAMETER	**L296P**	**L4960**	**L4962**	**L4964**	**L4963**	**L4963D**
Output Current	4A	2.5A	1.5A	4A	1.5A	0.5A
fsw	100kHz				variable	
Input Voltage	9V to 46V				9V to 46V	
Output Voltage	5.1V to 40V				5.1V to 36V	
Current Limiting	Soft Start Triggers				Constant Current	
Operating Mode	Continuous Mode				Discontinuous Mode	
Soft Start	yes				no	
Reset and Power Fail	yes	no	no	yes	yes	yes
Crowbar	yes	no	no	yes	no	no
Package	Multiwatt15	Heptawatt	Powerdip 12+2+2	Multiwatt15	Powerdip 12+3+3	SO20 16+2+2
Max. $R_{thj\text{-}case\ (PIN)}$	3°C/W	4°C/W	14°C/W	3°C/W	12°C/W	15°C/W

POWER FACTOR CORRECTOR CONTROLLERS			
Parameter	**L4981A**	**L4981B**	**L6560**
Operating Mode	Average Current	Average Current	Transition
Single Ended DMOS Output	●	●	●
Switching Frequency	Up to 200KHz	Up to 200KHz (Modulated)	Variable
Low Current Start Up (Max)	1mA	1mA	0.7mA
Voltage Reference	±2%	±2%	±2%
Over Current Protection	●	●	–
Over Voltage Protection	●	●	●
Synchronization	●	–	–
Load Feed Forward	●	●	–
Under Voltage Lockout	●	●	●
Soft Start	●	●	–
Package	DIP20/S020	DIP20/SO20	Minidip/SO8

DATASHEETS

SGS-THOMSON
MICROELECTRONICS

L296
L296P

HIGH CURRENT SWITCHING REGULATORS

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

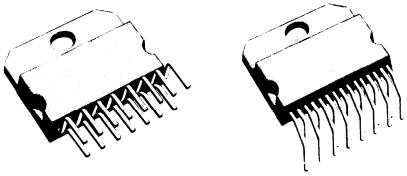
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

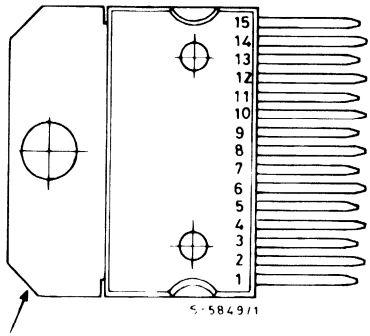
Multiwatt
(15-lead)



ORDER CODES :

L296	L296HT
L296P	L296PHT

PIN CONNECTION (top view)



CROWBAR DRIVE
RESET OUTPUT
RESET DELAY
RESET INPUT
OSCILLATOR
FEEDBACK INPUT
FREQUENCY COMPENSATION
GROUND
SYNC. INPUT
INHIBIT INPUT
SOFT-START
CURRENT LIMIT
SUPPLY VOLTAGE
OUTPUT
CROWBAR INPUT

Tab connected to pin 8

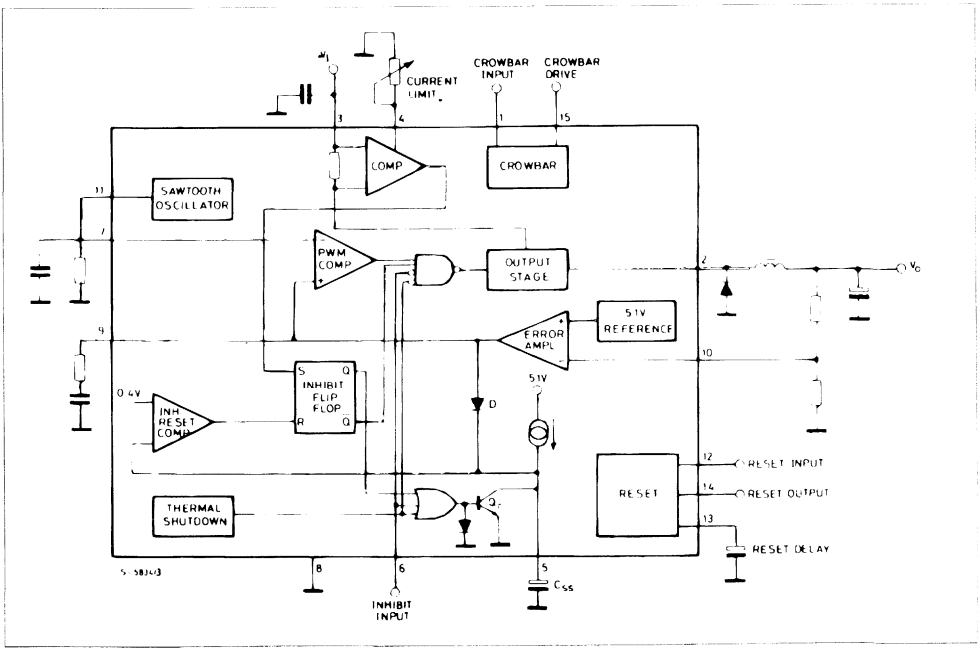
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Input Voltage (pin 3)	50	V
$V_i - V_2$	Input to Output Voltage Difference	50	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 200KHz	− 1 − 7	V V
V_1, V_{12}	Voltage at Pins 1, 12	10	V
V_{15}	Voltage at Pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at Pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at Pins 10 and 6	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	− 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

BLOCK DIAGRAM



PIN FUNCTIONS

N	Name	Function
1	CROWBAR INPUT	Voltage Sense Input for Crowbar Overvoltage Protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20 %. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unrergulated Voltage Input. An internal Regulator Powers the L296s Internal Logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – Level Remote Inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal on the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC networki connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1 V to 40 V and delivering 4 A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 2 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor Css and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

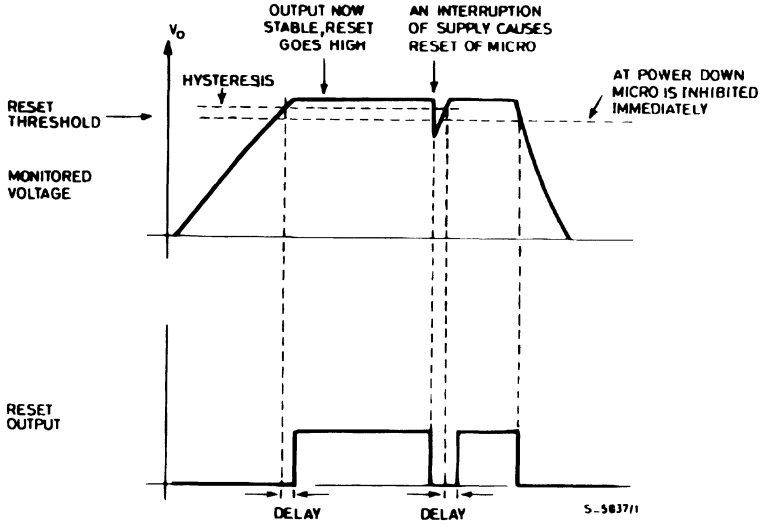
The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The scrowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20 %. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 °C and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.



CIRCUIT OPERATION (continued)

Figure 2 : Soft Start Waveforms.

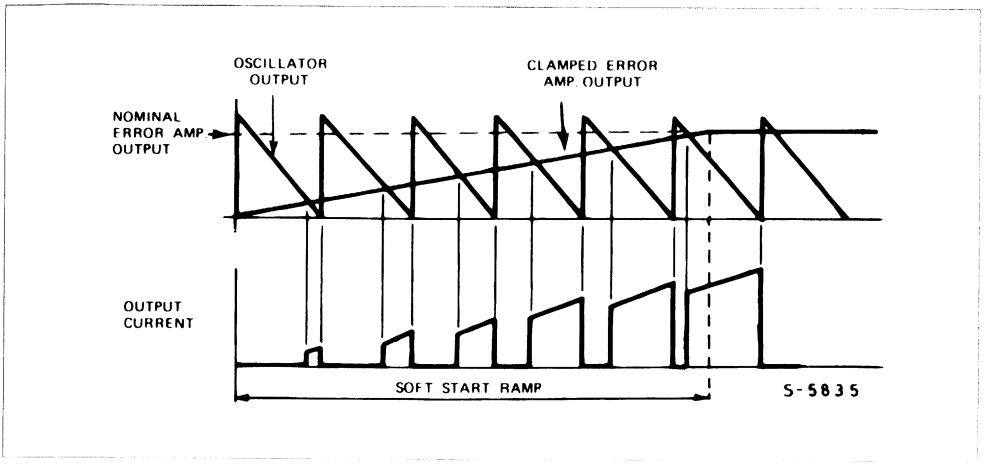
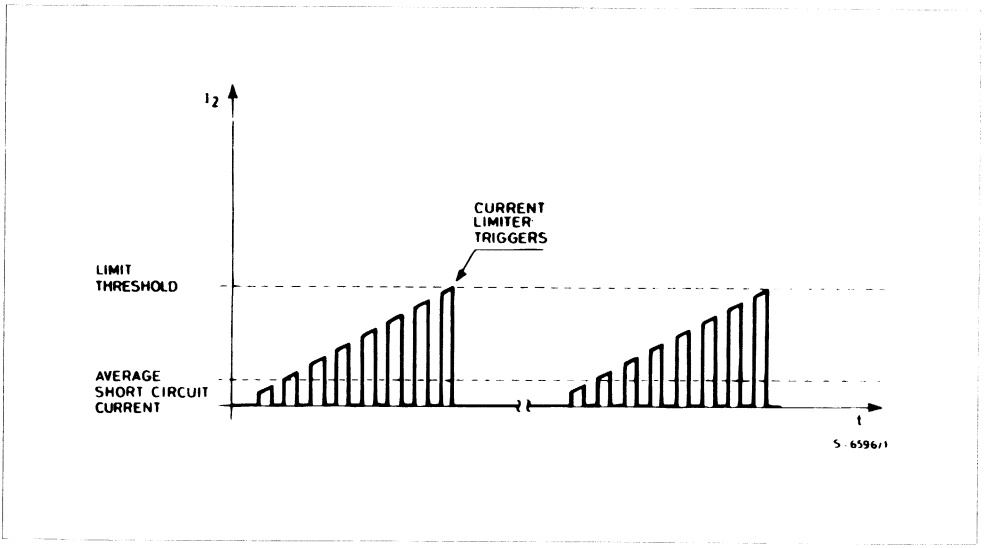


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 35 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)							
V_o	Output Voltage Range	V_i = 46 V I_o = 1 A	V_{ref}		40	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 36 V $I_o \leq 3$ A	9		46	V	4
V_i	Input Voltage Range	Note (1) $V_o = V_{REF}$ to 36 V I_o = 4 A			46	V	4
ΔV_o	Line Regulation	V_i =10 V to 40 V, $V_o = V_{ref}$, I_o = 2 A		15	50	mV	4
ΔV_o	Load Regulation	I_o = 2 A to 4 A		10	30	mV	4
		$V_o = V_{ref}$ I_o = 0.5 A to 4 A		15	45	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 46 V I_o = 2 A	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/ °C	
V_d	Dropout Voltage Between Pin 2 and Pin 3	I_o = 4 A		2	3.2	V	4
		I_o = 2 A		1.3	2.1	V	4
I_{2L}	Current Limiting Threshold (pin 2)	L296 Pin 4 Open V_i = 9 V to 40 V $V_o = V_{ref}$ to 36 V	4.5		7.5	A	4
		L296P Pin 4 Open	5		7	A	4
		V_i = 9 V to 40 V R_{lim} = 22 KΩ $V_o = V_{ref}$	2.5		4.5	A	4
I_{SH}	Input Average Current	V_i = 46 V; Output Short-circuited		60	100	mA	4
η	Efficiency	I_o = 3 A $V_o = V_{ref}$		75		%	4
		V_o = 12 V		85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms} f_{ripple} = 100 Hz $V_o = V_{ref}$ I_o = 2 A	50	56		dB	4
f	Switching Frequency		85	100	115	KHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9 V to 46 V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0 °C to 125 °C		1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; I_o = 1 A	200			KHz	–
T_{sd}	Thermal Shutdown Junction Temperature	Note (2)	135	145		°C	–
DC CHARACTERISTICS							
I_{3Q}	Quiescent Drain Current	V_i = 46 V V_7 = 0 V V_6 = 0 V		66	85	mA	6a
		S1 : B V_6 = 3V S2 : B		30	40	mA	6a
$-I_{2L}$	Output Leakage Current	V_i = 46 V, V_6 = 3 V, S1 : B, S2 : A, V_7 = 0 V			2	mA	6a

Note (1) : Using min. 7 A schottky diode.
(2) : Guaranteed by design, not 100 % tested in production.

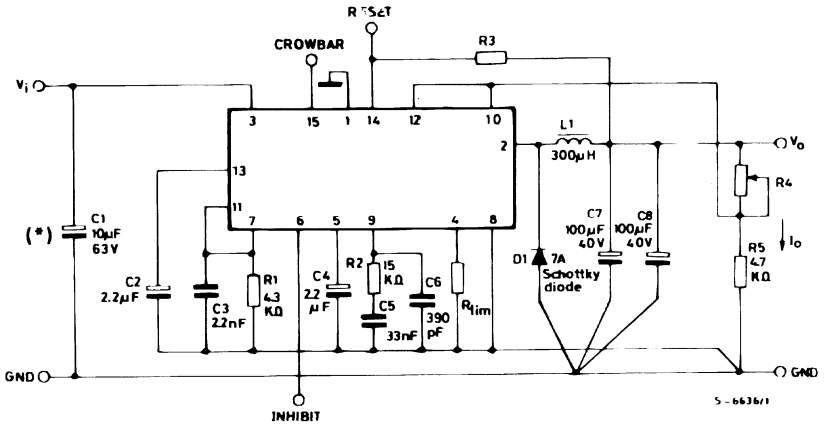
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
SOFT START								
$I_{5\,so}$	Source Current	$V_6 = 0$ V, $V_5 = 3$ V		80	130	150	µA	6b
$I_{5\,si}$	Sink Current	$V_6 = 3$ V, $V_5 = 3$ V		50	70	120	µA	6b
INHIBIT								
V_{6L}	Low Input Voltage	$V_i = 9$ V to 46 V	S1 : B S2 : B	− 0.3		0.8	V	6a
V_{6H}	High Input Voltage	$V_7 = 0$ V		2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	$V_i = 9$ V to 46 V	$V_6 = 0.8$ V			10	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	$V_7 = 0$ V S1 : B S2 : B	$V_6 = 2$ V			3	µA	6a
ERROR AMPLIFIER								
V_{9H}	High Level Output Voltage	$V_{10} = 4.7$ V, $I_9 = 100$ µA,	S1 : A, S2 : A	3.5			V	6c
V_{9L}	Low Level Output Voltage	$V_{10} = 5.3$ V, $I_9 = 100$ µA,	S1 : A, S2 : E			0.5	V	6c
$I_{9\,si}$	Sink Output Current	$V_{10} = 5.3$ V,	S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	$V_{10} = 4.7$ V,	S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	$V_{10} = 5.2$ V,	S1 : B		2	10	µA	6c
		$V_{10} = 6.4$ V,	S1 : B, L296P		2	10	µA	6c
G_v	DC Open Loop Gain	$V_9 = 1$ V to 3 V,	S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR								
$-I_7$	Input Bias Current of PWM Comparator	$V_7 = 0.5$ V to 3.5 V				5	µA	6a
$-I_{11}$	Oscillator Source Current	$V_{11} = 2$ V,	S1 : A S2 : B	5				mA
RESET								
$V_{12\,R}$	Rising Threshold Voltage	$V_i = 9$ V to 46 V,	S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\,F}$	Falling Threshold Voltage			4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\,D}$	Delay Thershold Voltage	$V_{12} = 5.3$ V,	S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\,H}$	Delay Threshold Voltage Hysteresis				100		mV	6d
$V_{14\,S}$	Output Saturation Voltage	$I_{14} = 16$ mA; $V_{12} = 4.7$ V;	S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	$V_{12} = 0$ V to V_{ref},	S1 : B, S2 : B		1	3	µA	6d
$-I_{13\,so}$	Delay Source Current	$V_{13} = 3$ V S1 : A S2 : B	$V_{12} = 5.3$ V	70	110	140	µA	6d
$I_{13\,si}$	Delay Sink Current		$V_{12} = 4.7$ V	10			mA	6d
I_{14}	Output Leakage Current	$V_i = 46$ V, $V_{12} = 5.3$ V,	S1 : B, S2 : A			100	µA	6d

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
CROWBAR								
V_1	Input Threshold Voltage	S1 : B		5.5	6	6.4	V	6b
V_{15}	Output Saturation Voltage	V_i = 9 V to 46 V. I_{15} = 5 mA	V_i = 5.4 V S1 : A		0.2	0.4	V	6b
I_1	Input Bias Current	V_1 = 6 V.	S1 : B			10	µA	6b
$-I_{15}$	Output Source Current	V_i = 9 V to 46 V. V_{15} = 2 V	V_1 = 6.5 V S1 : B	70	100		mA	6b

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A Core type : MAGNETICS 58930 - A2 MPP
N turns : 43 Wire Gauge : 1 mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10 µF) to avoid oscillations. Ripple consideration leads to typical value of 1000 µF or higher.

Figure 5 : PC. Board and Component Layout of the Circuit of Figure 4 (1:1 scale).

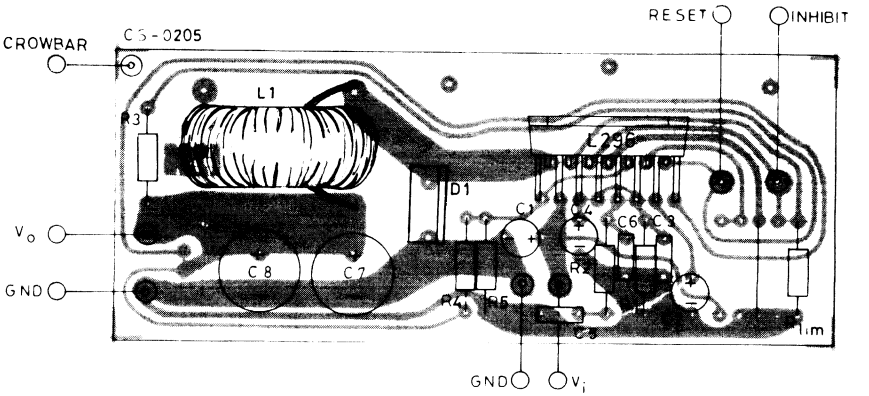


Figure 6 : DC Test Circuits.

Figure 6a.

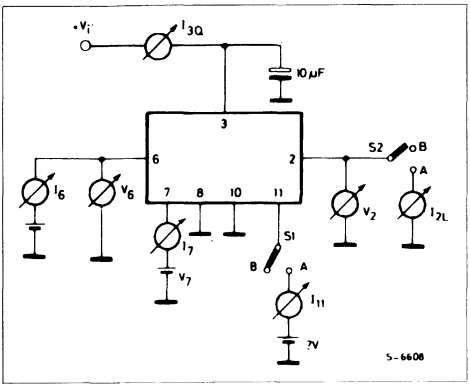


Figure 6b.

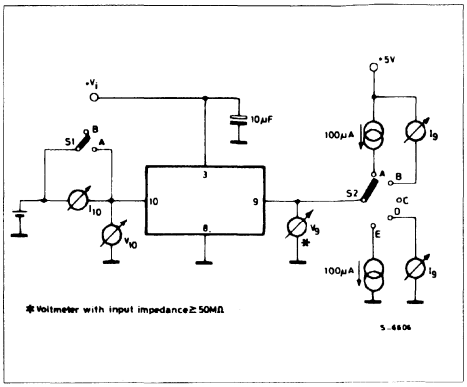


Figure 6c.

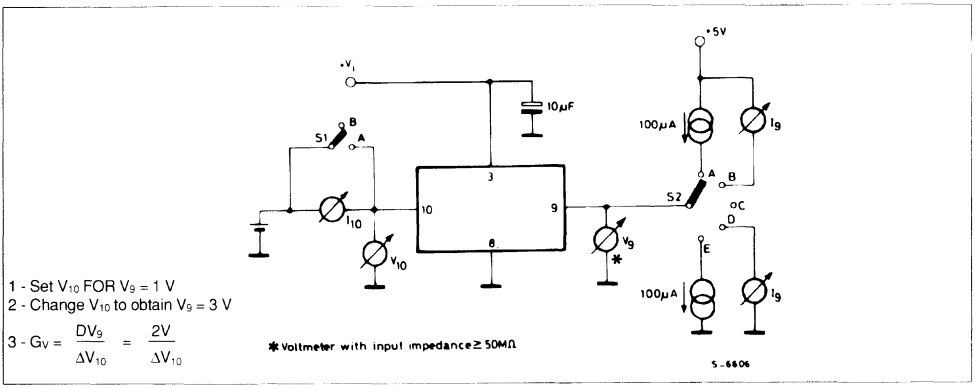


Figure 6d.

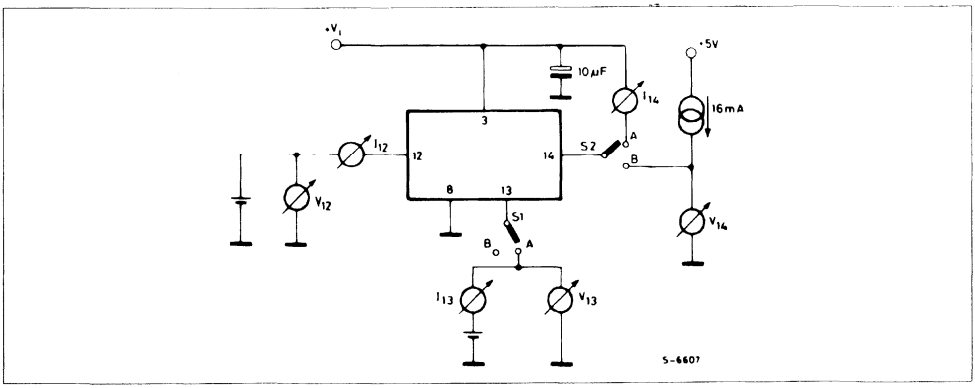


Figure 7 : Quienscent Drain Current vs. Supply Voltage (0 % Duty Cycle - see fig. 6a).

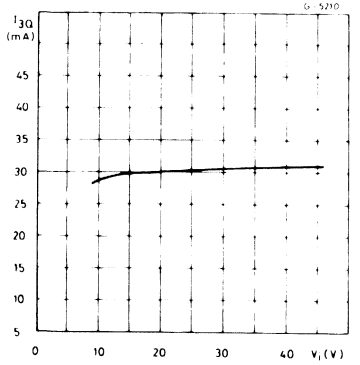


Figure 8 : Quienscent Drain Current vs. Supply Voltage (100 % Duty Cycle see fig. 6a).

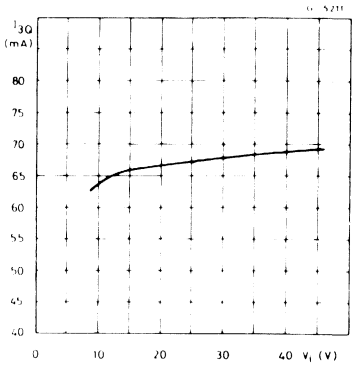


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % Duty Cycle - see fig. 6a).

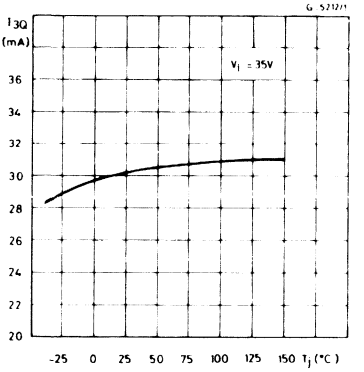


Figure 10 : Quiescent Drain Current vs. Junction Temperature (100 % Duty Cycle - see fig. 6a).

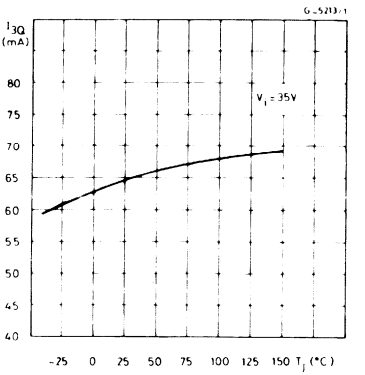


Figure 11 : Reference Voltage (pin 10) vs. V_I (see fig. 4).

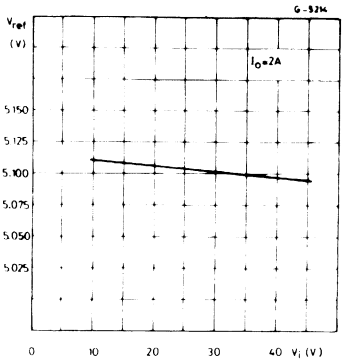


Figure 12 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

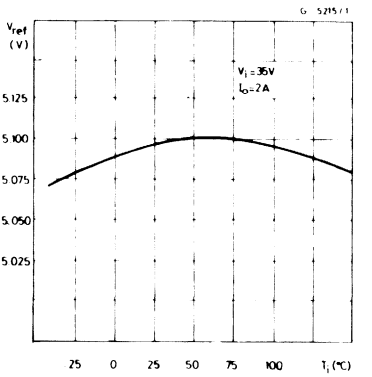


Figure 13 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

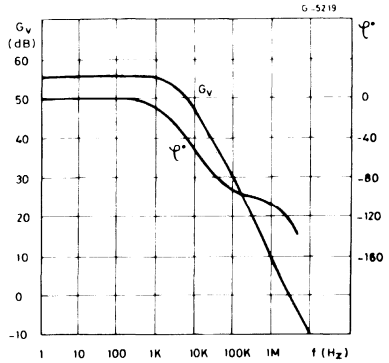


Figure 14 : Switching Frequency vs. Input Voltage (see fig. 4).

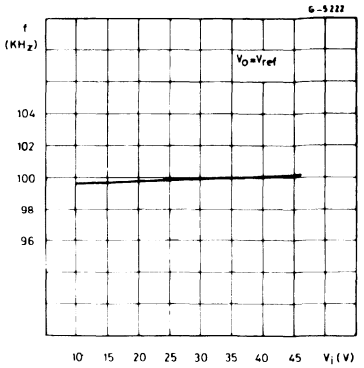


Figure 15 : Switching Frequency vs. Junction Temperature (see fig. 4).

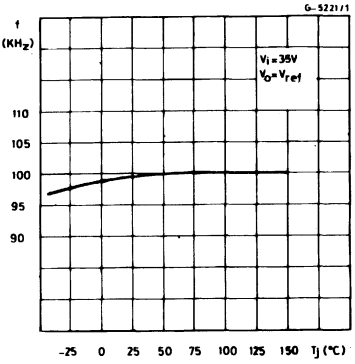


Figure 16 : Switching Frequency vs. R1 (see fig. 4).

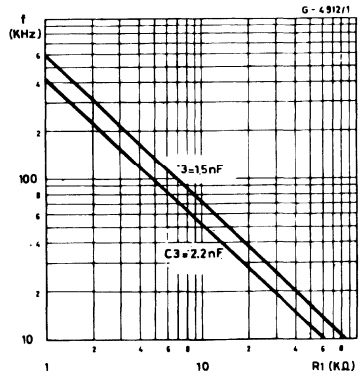


Figure 17 : Line Transient Response (see fig. 4).

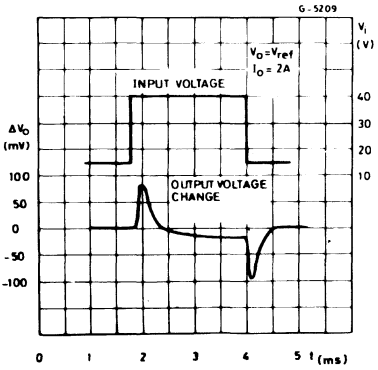


Figure 18 : Load Transient Response (see fig. 4).

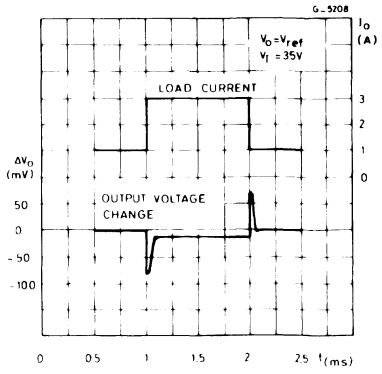


Figure 19 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 4).

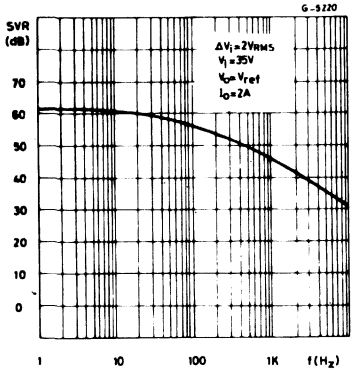


Figure 20 : Dropout Voltage Between Pin 3 and Pin 2 vs. Current at Pin 2.

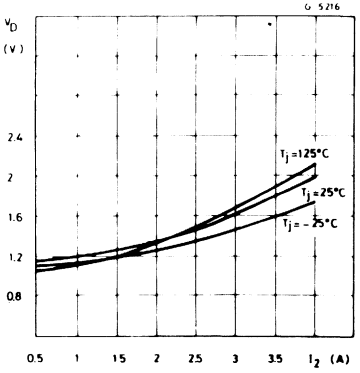


Figure 21 : Dropout Voltage Between Pin 3 and Pin 2 vs. Junction Temperature.

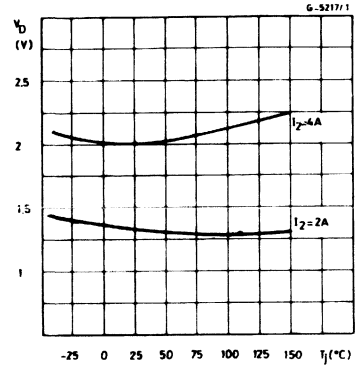


Figure 22 : Power Dissipation Derating Curve.

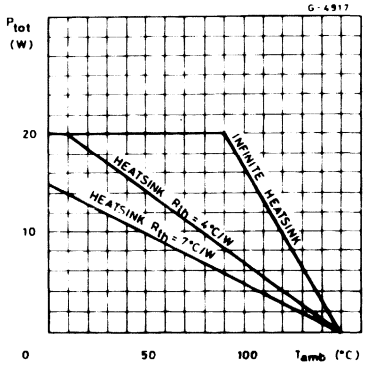


Figure 23 : Power Dissipation (device only) vs. Input Voltage.

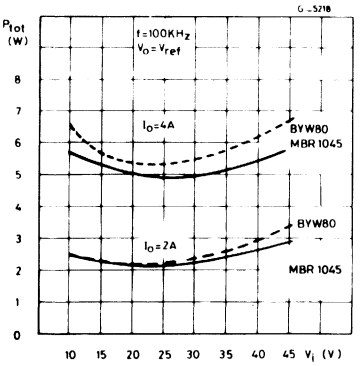


Figure 24 : Power Dissipation (device only) vs. Input voltage.

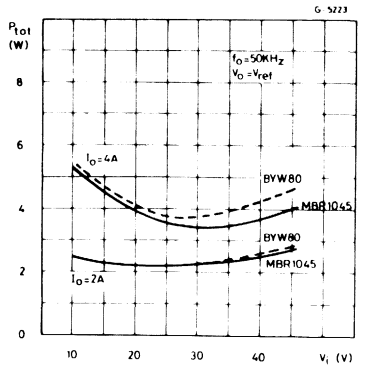


Figure 25 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

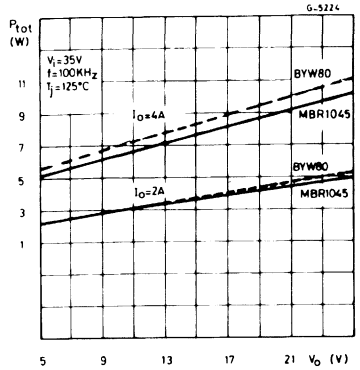


Figure 26 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

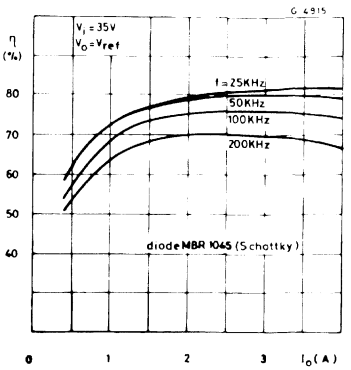


Figure 27 : Voltage and Current Waveforms at Pin 2 (see fig. 4).

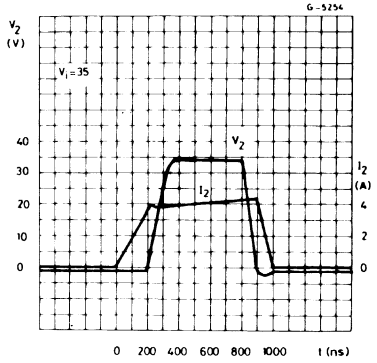


Figure 28 : Efficiency vs. Output Current.

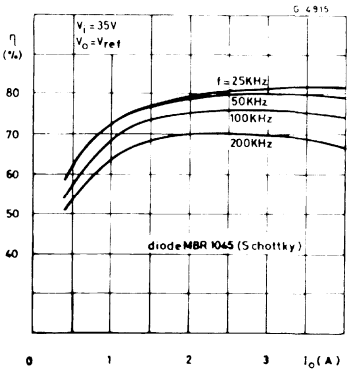


Figure 29 : Efficiency vs. Output Voltage.

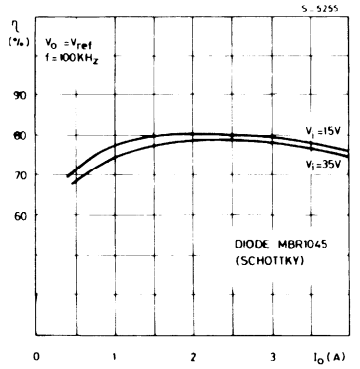


Figure 30 : Efficiency vs. Output Voltage.

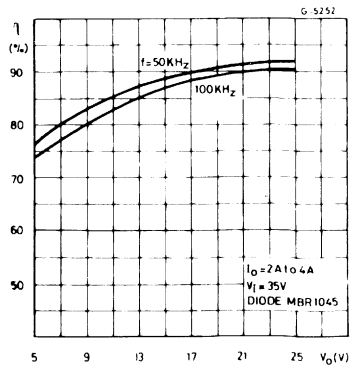


Figure 31 : Current Limiting Threshold vs. $R_{pin\ 4}$ (L296P only).

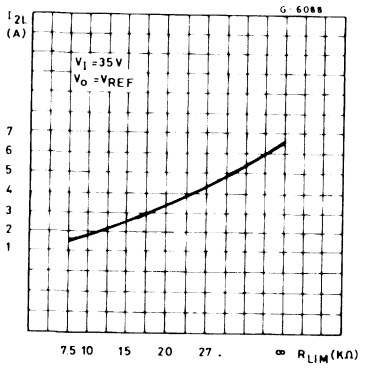


Figure 32 : Current Limiting Threshold vs. Junction Temperature.

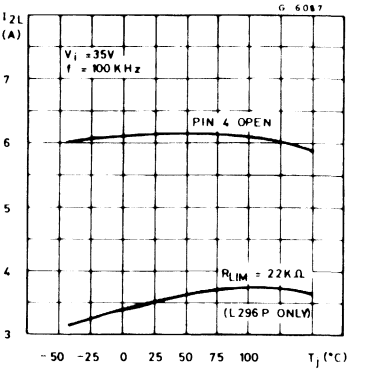
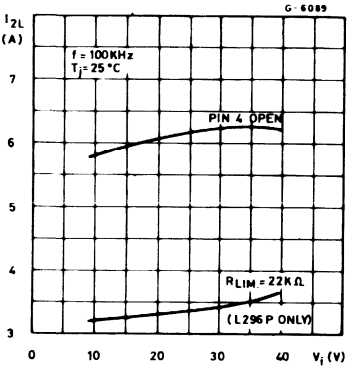
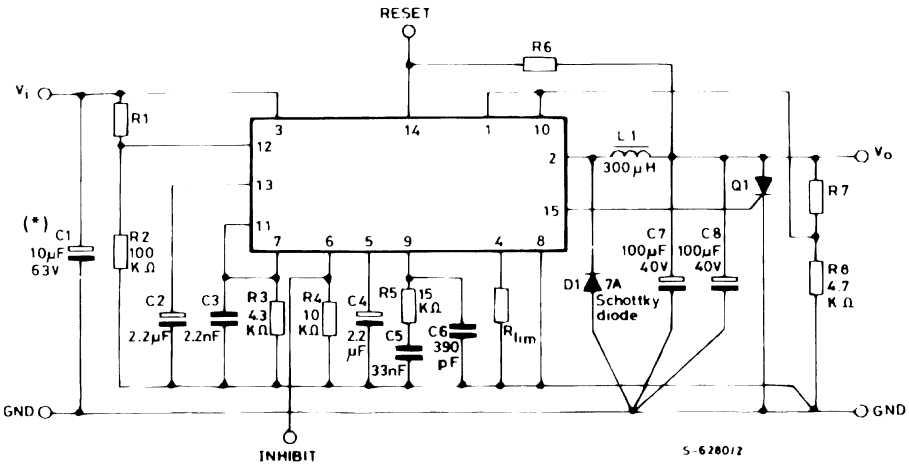


Figure 33 : Current Limiting Threshold vs. Supply Voltage.



APPLICATION INFORMATION

Figure 34 : Typical Application Circuit.



(*) Minimum value (10 µF) to avoid oscillations : ripple consideration leads to typical value of 1000 µF or higher L1 : 58930 - MPP COGEMA 946044 ; GUP 20 COGEMA 946045

SUGGESTED INDUCTOR (L1)

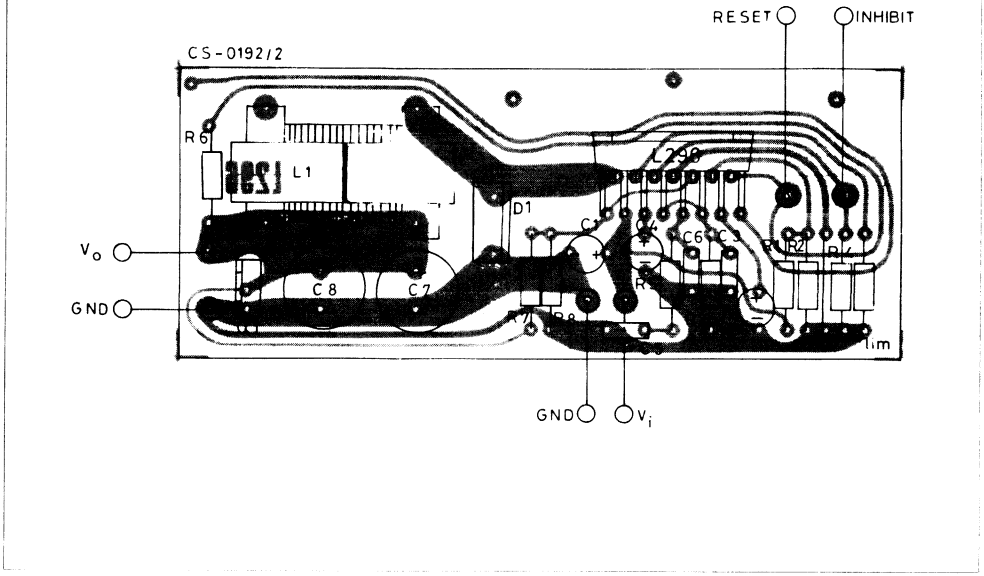
Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	65	0.8 mm	1 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–

VOGT 250 µH Toroidal Coil, Part Number 5730501800

Resistor Values for Standard Output Voltages

V_o	R8	R7
12 V	4.7 KΩ	6.2 KΩ
15 V	4.7 KΩ	9.1 KΩ
18 V	4.7 KΩ	12 KΩ
24 V	4.7 KΩ	18 KΩ

Figure 35 : P.C. Board and Component Layout of the Circuit of fig. 34 (1:1 scale).



SELECTION OF COMPONENT VALUES (see fig. 34)

Component	Recommended Value	Purpose	Allowed Rage Min.	Allowed Rage Max.	Notes
R1 R2	– 100 kΩ	Set Input Voltage Threshold for Reset.	–	220 kΩ	$R1/R2 = \frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets Switching Frequency	1 kΩ	100 kΩ	
R4	10 kΩ	Pull-down Resistor		22 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency Compensation	10 kΩ		
R6		Collector Load For Reset Output	$\frac{V_o}{0.05\ A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to Set Output Voltage	– –	– 10 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R_{lim}	–	Sets Current Limit Level	7.5 kΩ		If R_{lim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 µF	Stability	2.2 µF		
C2	2.2 µF	Sets Reset Delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets Switching Frequency	1 nF	3.3 nF	
C4	2.2 µF	Soft Start	1 µF	–	Also determines average short circuit current.
C5	33 nF	Frequency Compensation			
C6	390 pF	High Frequency Compensation	–	–	Not required for 5 V operation.
C7, C8 L1	100 µF 300 µH	Output Filter	– 100 µH	–	
Q1		Crowbar Protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation Diode			7A Schottky or 35 ns t_{rr} Diode.

Figure 36 : A Minimal 5.1 V Fixed Regulator. Very Few Components are Required.

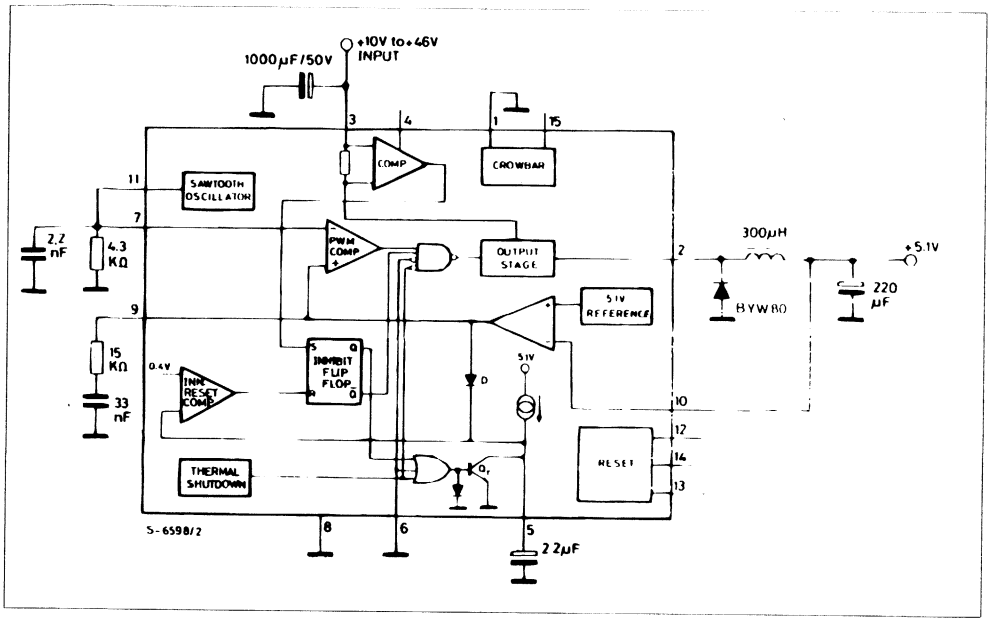


Figure 37 : 12 V/10 A Power Supply.

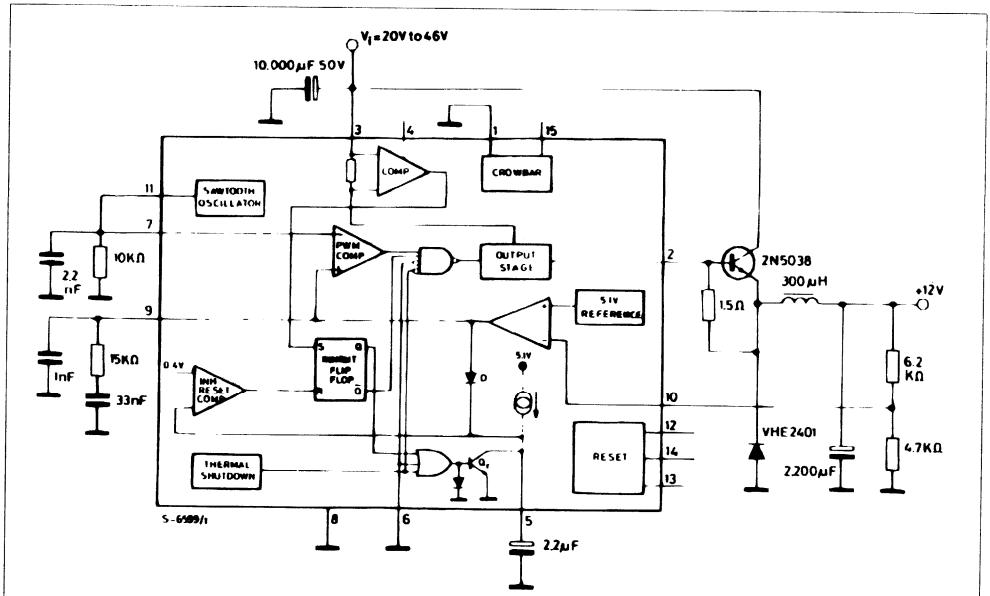
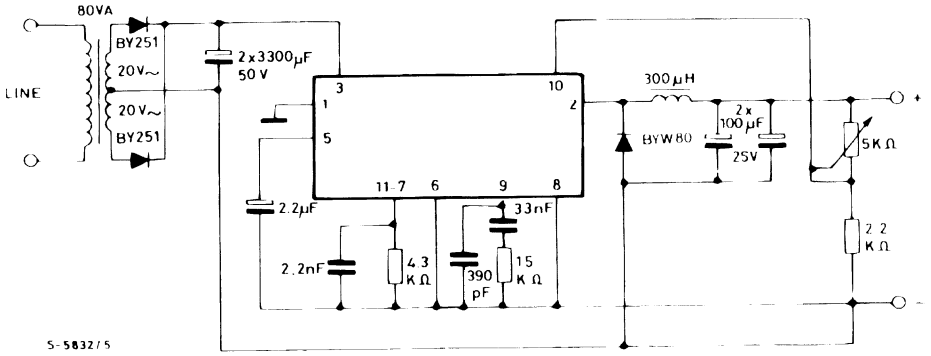
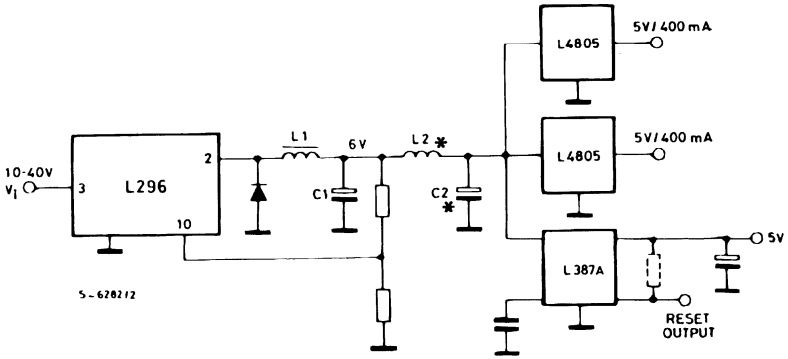


Figure 38 : Programmable Power Supply.



V_o ≅ 5.1 to 15 V
I_o = 4 A max. (min. load current = 100 mA)
ripple ≤ 20 mV
load regulation (1 A to 4 A) = 10 mV (V_o = 5.1 V)
line regulation (220 V ± 15 % and to I_o = 3 A) = 15 mV (V_o = 5.1 V)

Figure 39 : Preregulator for Distributed Supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Figure 40 : In Multiple Supplies Several L296s can be Synchronized As Shown.

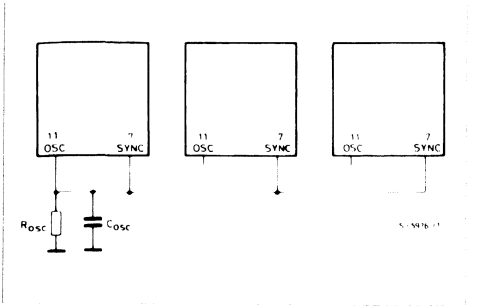


Figure 41 : Voltage Sensing for Remote Load.

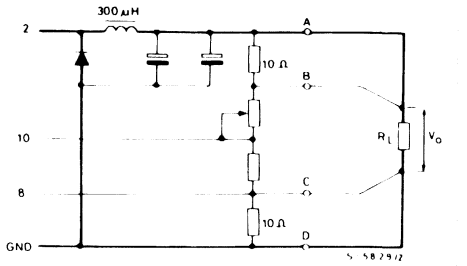


Figure 42 : A 5.1 V/15 V/24 V Multiple Supply. Note the Synchronization of the Three L296s.

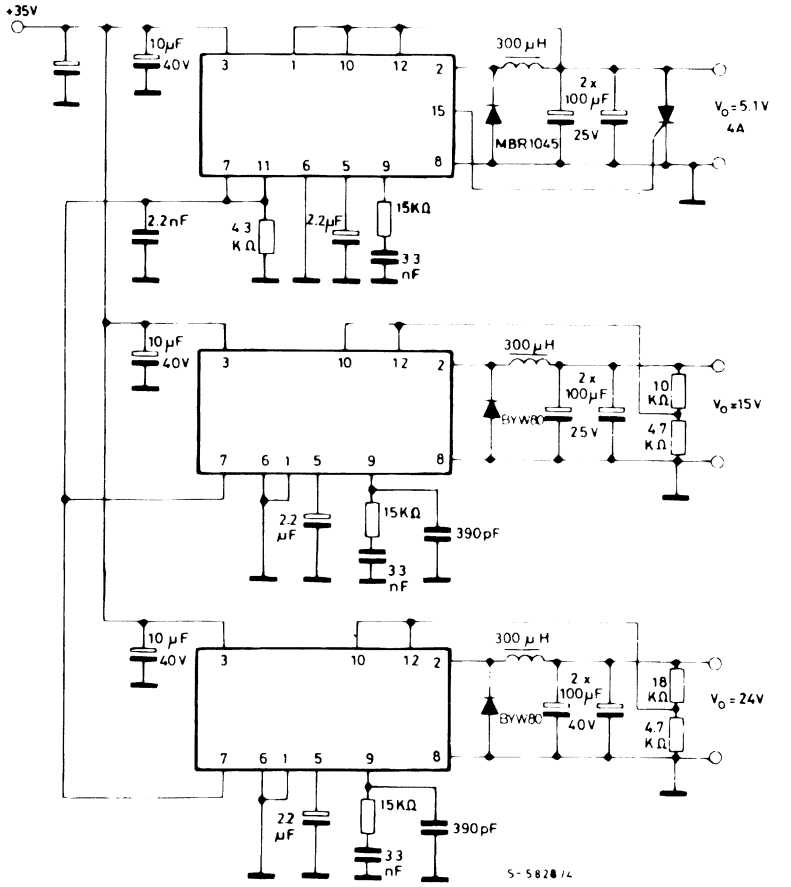
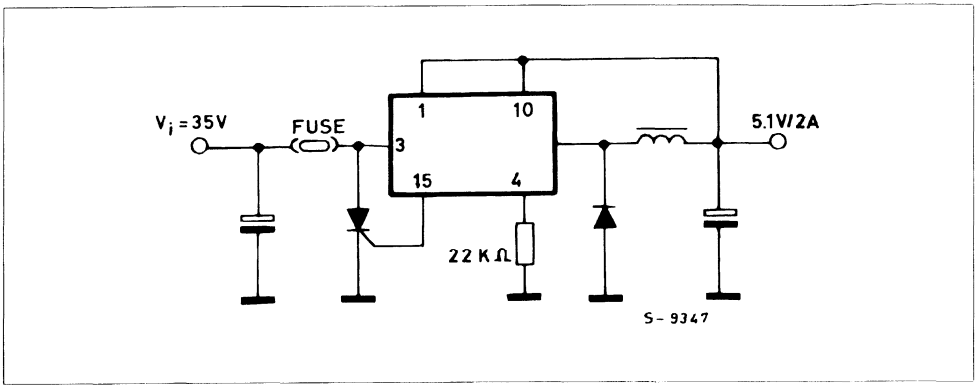


Figure 43 : 5.1 V/2 A Power Supply using External Limiting Current Resistor and Crowbar Protection on the Supply Voltage (L296P only).



SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Fig. 44.

In this circuit the divider R1, R2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS}.

The approximate discharge times obtained with this circuit are :

C_{SS}	t_{DIS}
2.2 µF	200 µs
4.7 µF	300 µs
10 µF	600 µs

If these times are still too long, an external PNP transistor may be added, as shown in Fig. 45 ; with this circuit discharge times of a few microseconds may be obtained.

Figure 44.

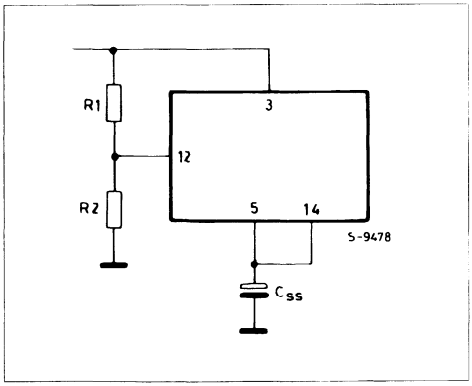
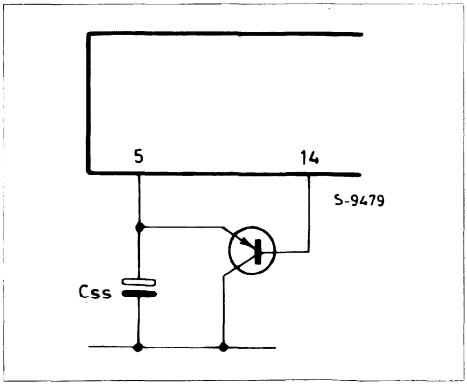


Figure 45.



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

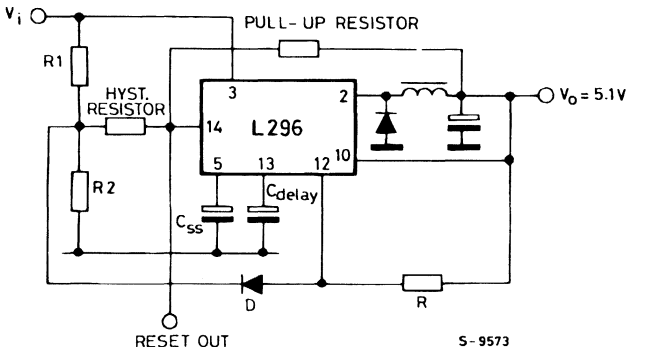
In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geq V_{REF}$ - 100 mV and the voltage across R2 is higher than 4.5 V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100 Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about 100 KΩ and the pull-up resistor of 1 to 2.2 KΩ.

Figure 46.



2.5A POWER SWITCHING REGULATOR

PRELIMINARY DATA

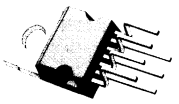
- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external componênts.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



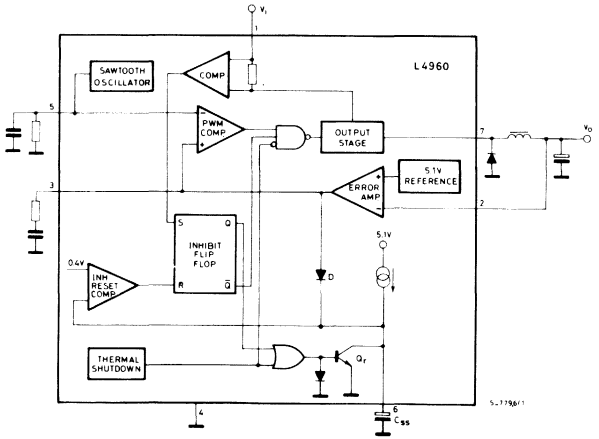
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

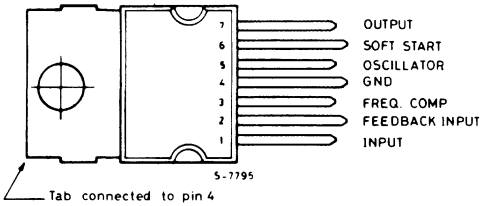
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_I = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	$V_I = 46V$ $I_o = 1A$	V_{ref}		40	V
V_I	Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 2.5A$	9		46	V
ΔV_o	Line regulation	$V_I = 10V$ to 40V $V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ $I_o = 0.5A$ to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	$V_I = 9V$ to 46V $I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$		0.4		mV/°C
V_d	Dropout voltage	$I_o = 2A$		1.4	3	V
I_{om}	Maximum operating load current	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V	2.5			A
I_{7L}	Current limiting threshold (pin 7)	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V	3		4.5	A
I_{SH}	Input average current	$V_i = 46V$; output short-circuit		30	60	mA
η	Efficiency	$f = 100KHz$ $V_o = V_{ref}$		75		%
		$I_o = 2A$ $V_o = 12V$		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$ $I_o = 1A$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	$V_I = 9V$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 2A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

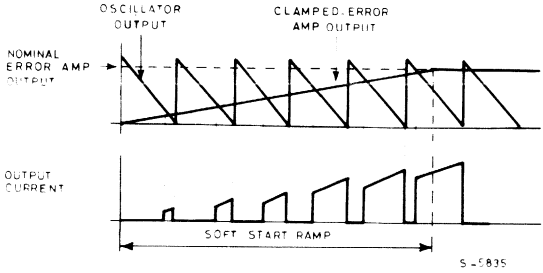


Fig. 2 - Current limiter waveforms

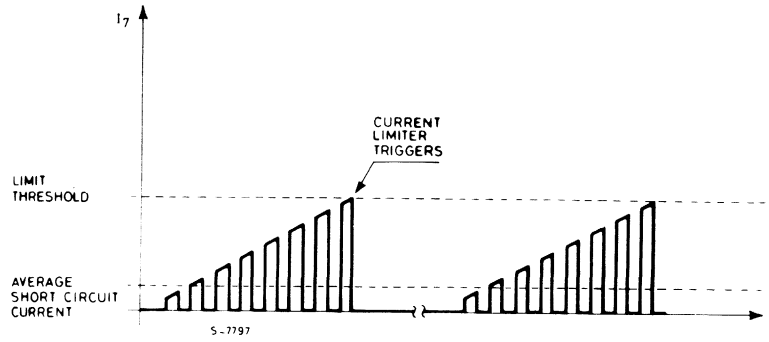
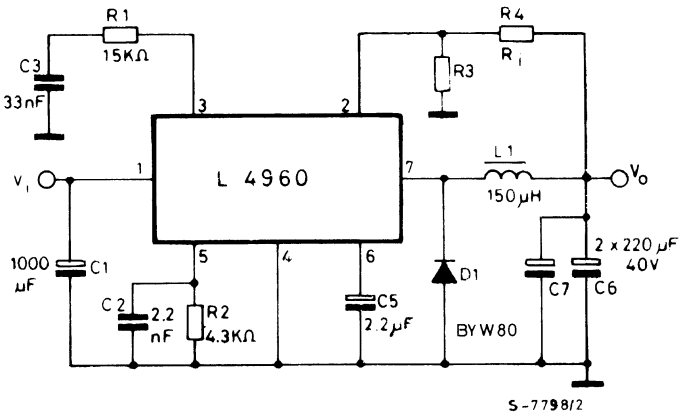


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150µH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

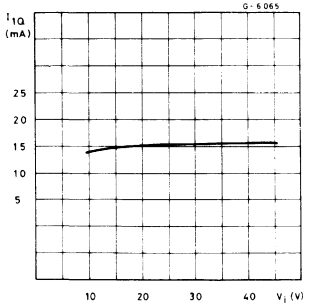


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

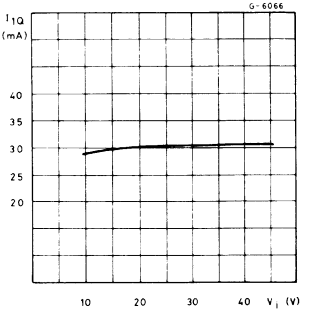


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

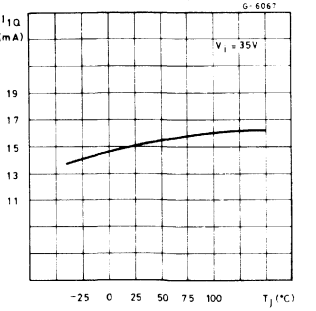


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

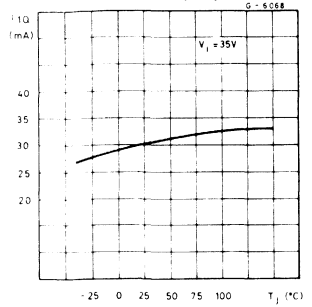


Fig. 8 - Reference voltage (pin 2) vs. V_I

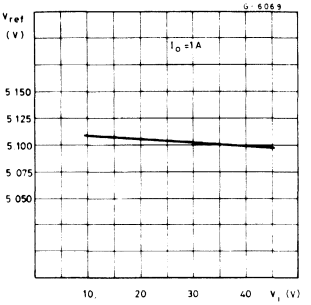


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

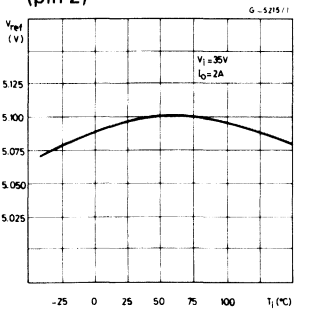


Fig. 10 - Open loop frequency and phase responde of error amplifier

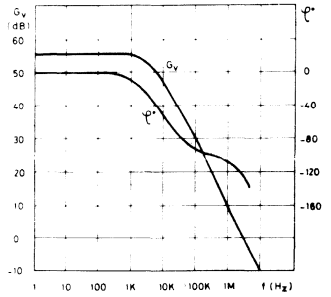


Fig. 11 - Switching frequency vs. input voltage

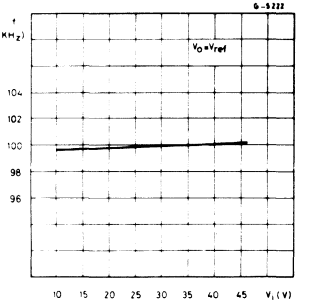


Fig. 12 - Switching frequency vs. junction temperature

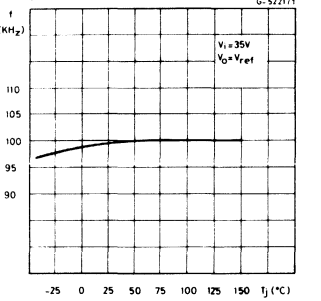


Fig. 13 - Switching frequency vs. R2 (see test circuit)

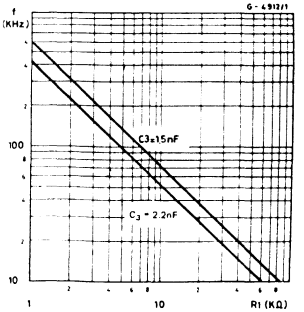


Fig. 14 - Line transient response

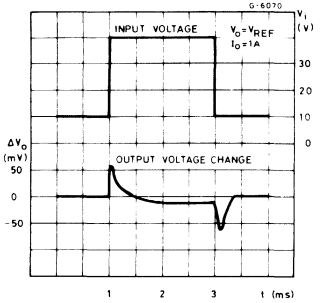


Fig. 15 - Load transient response

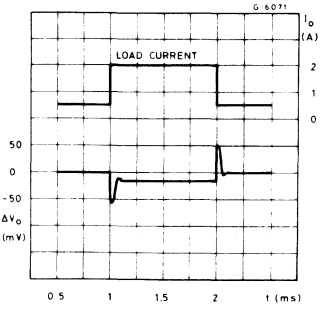


Fig. 16 - Supply voltage ripple rejection vs. frequency

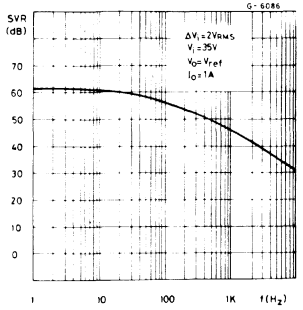


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

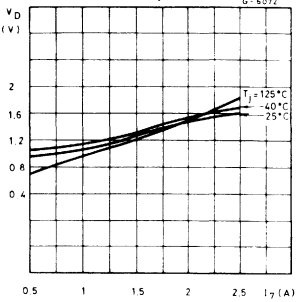


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

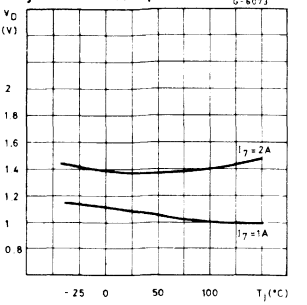


Fig. 19 - Power dissipation derating curve

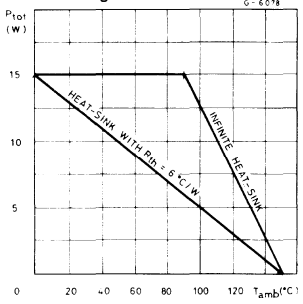


Fig. 20 - Efficiency vs. output current

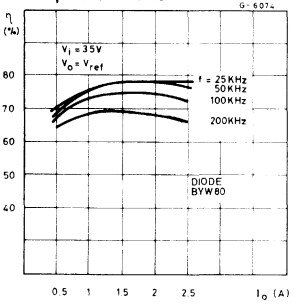


Fig. 21 - Efficiency vs. output current

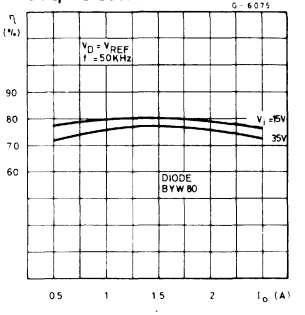


Fig. 22 - Efficiency vs. output current

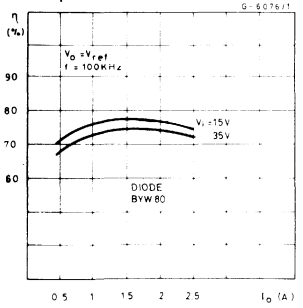
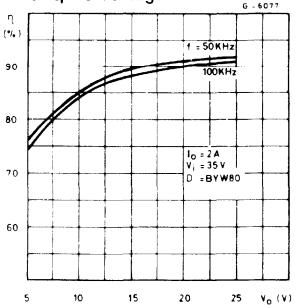
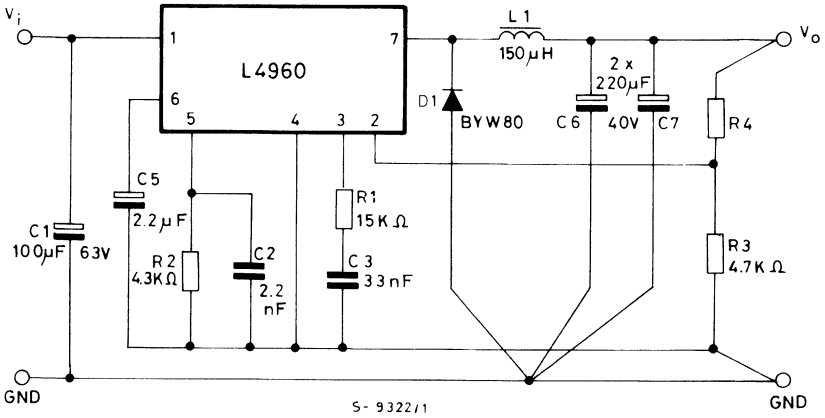


Fig. 23 - Efficiency vs. output voltage



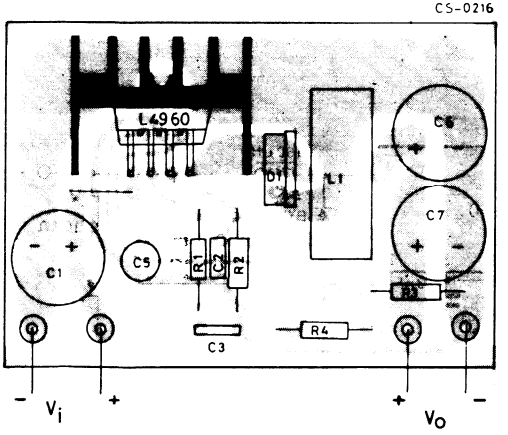
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required

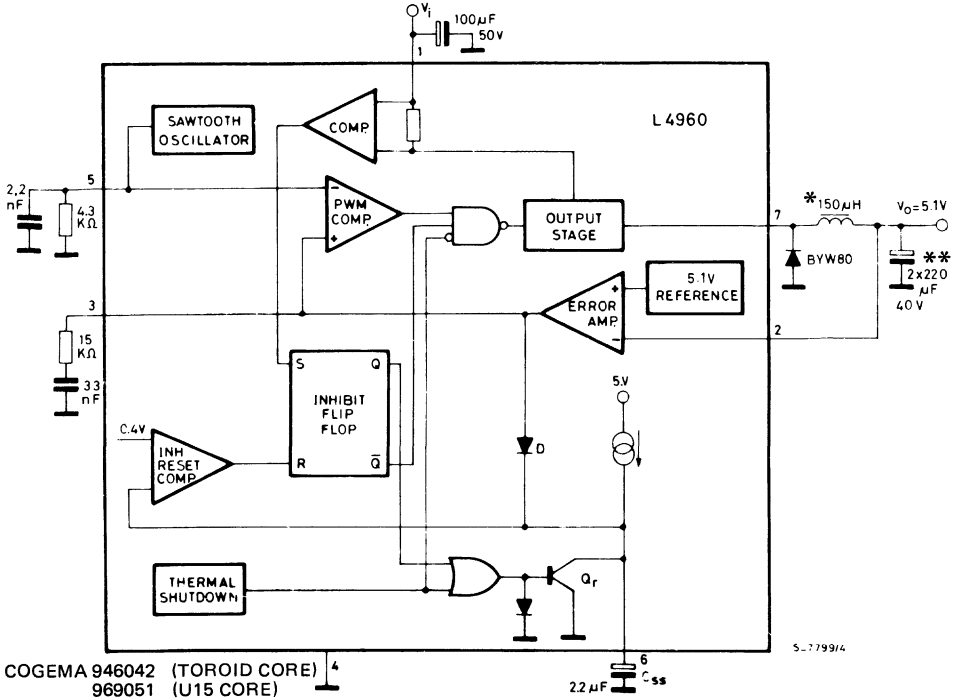
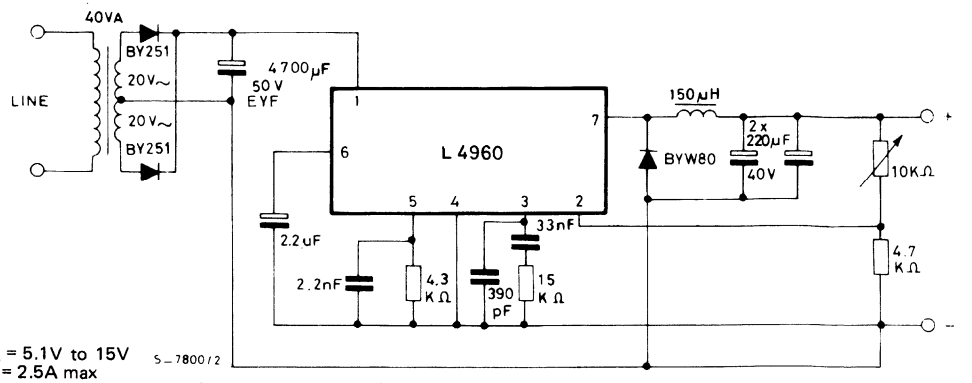


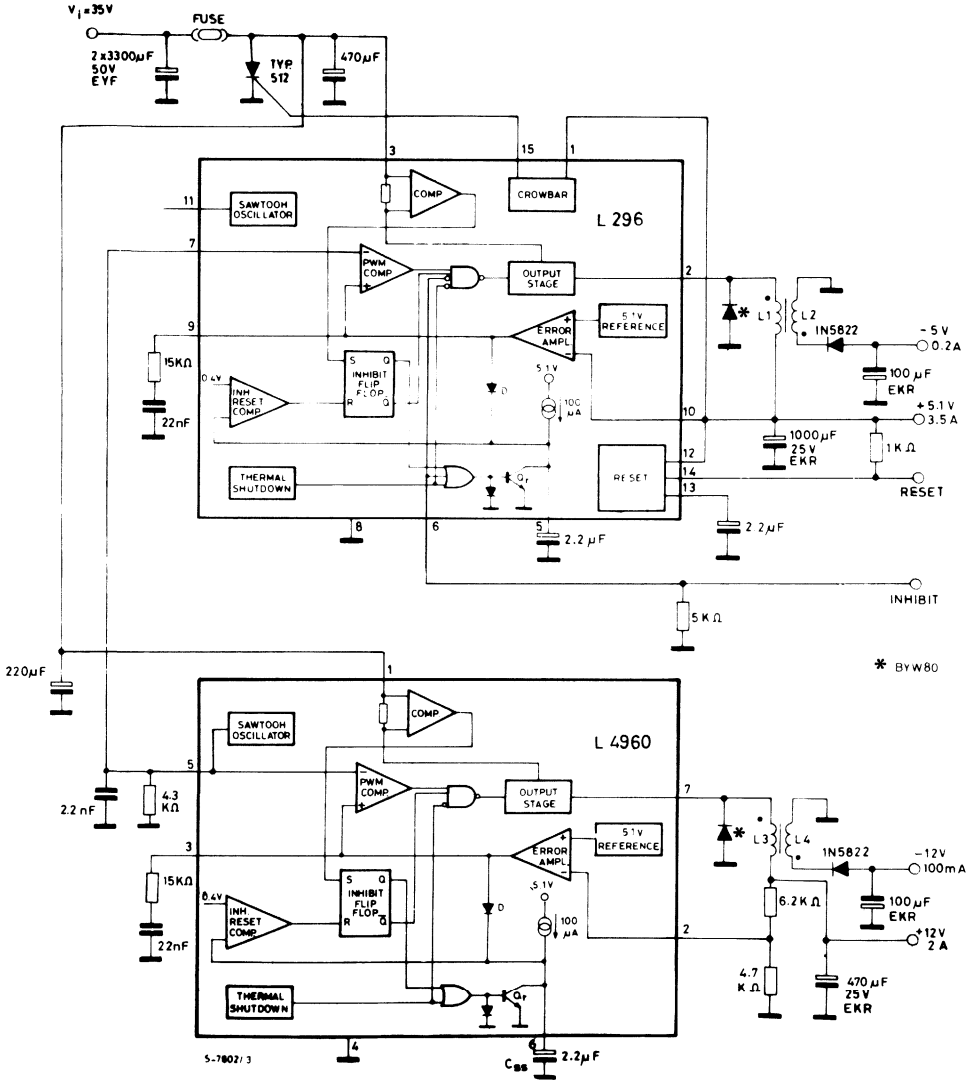
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

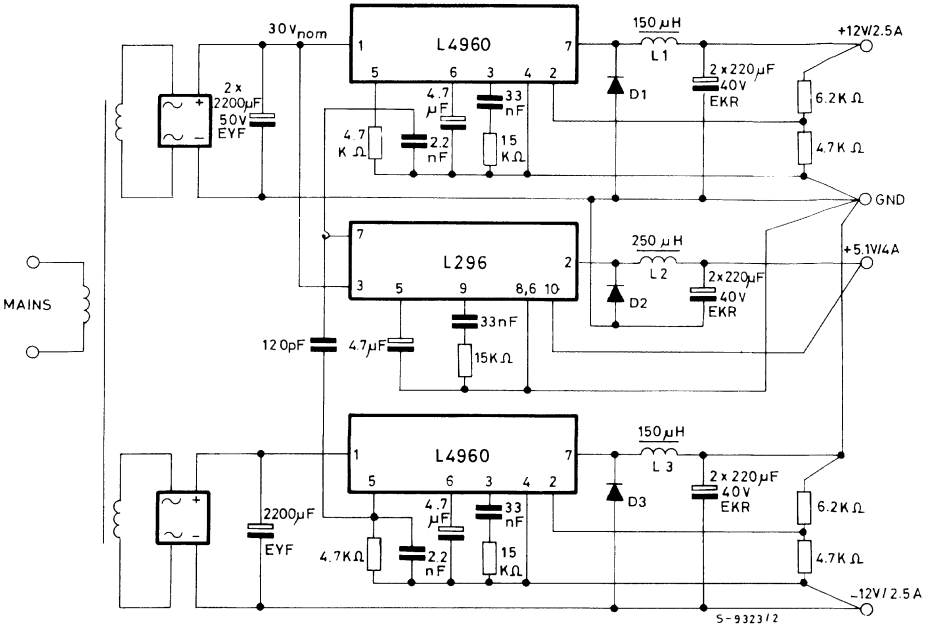
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, + 12V and -12V outputs



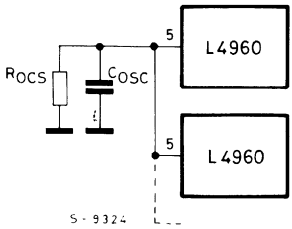
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



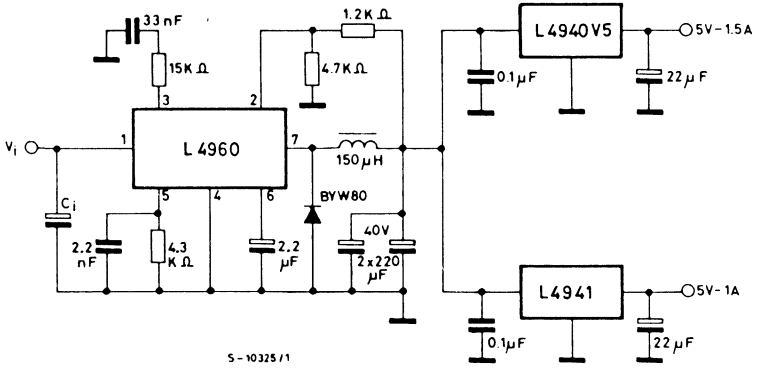
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D3 = BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

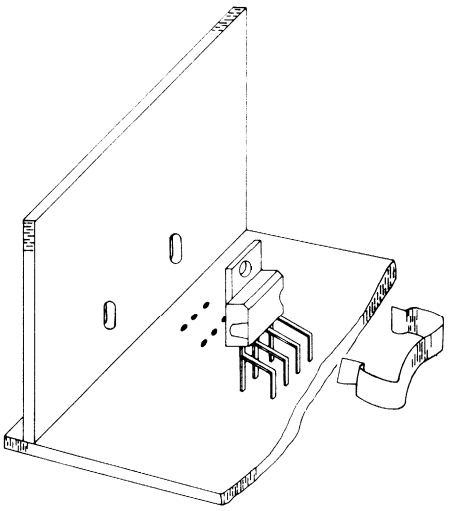
Fig. 31 - Regulator for distributed supplies



MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



1.5A POWER SWITHING REGULATOR

PRELIMINARY DATA

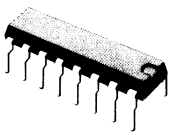
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

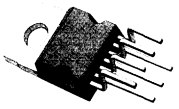
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

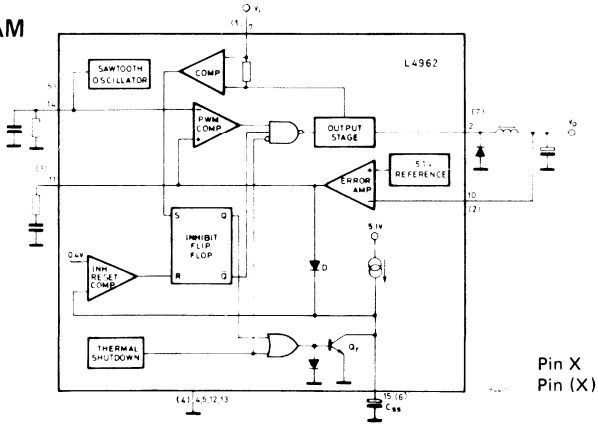
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leqslant 90°C$ (Powerdip)	4.3	W
	$T_{case} \leqslant 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

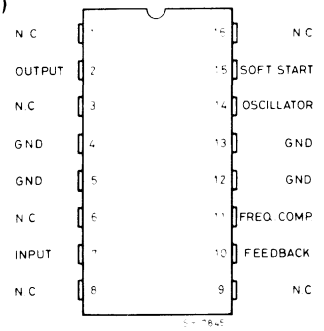
BLOCK DIAGRAM

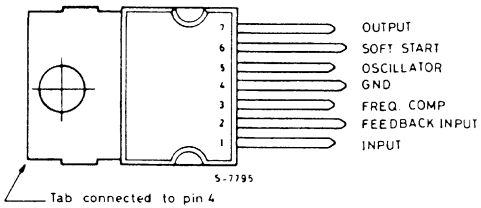


Pin X = Powerdip
Pin (X) = Heptawatt

CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	–
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	–	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	$V_i = 46V$ $I_o = 1A$	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 1.5A$	9		46	V
ΔV_o	Line regulation	$V_i = 10V$ to 40V $V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ $I_o = 0.5A$ to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	$V_i = 9V$ to 46V $I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$		0.4		mV/°C
V_d	Dropout voltage	$I_o = 1.5A$		1.5	2	V
I_{om}	Maximum operating load current	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V	1.5			A
I_{2L}	Current limiting threshold (pin 2)	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V	2		3.3	A
I_{SH}	Input average current	$V_i = 46V$; output short-circuit		15	30	mA
η	Efficiency	f = 100KHz $V_o = V_{ref}$		70		%
		$I_o = 1A$ $V_o = 12V$		80		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$ $I_o = 1A$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	$V_i = 9V$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 1A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

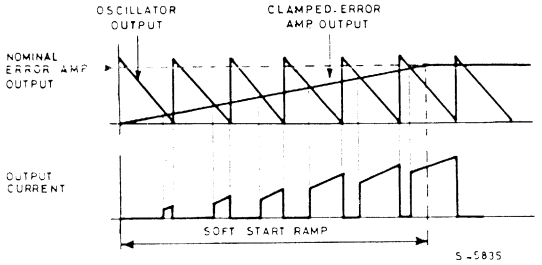


Fig. 2 - Current limiter waveforms

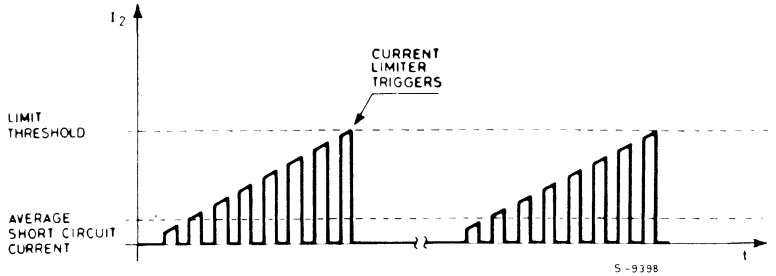
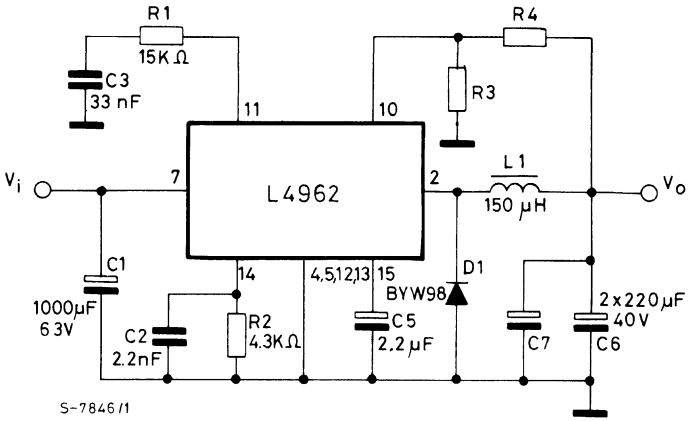


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

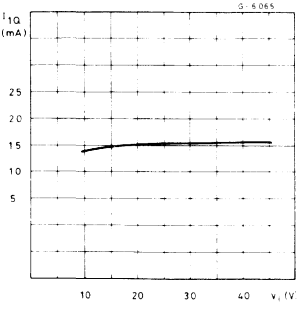


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

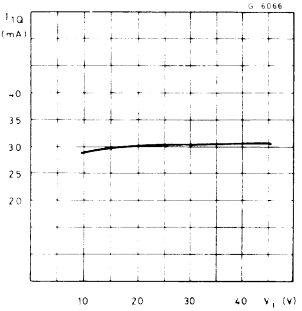


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

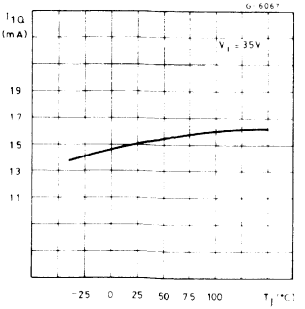


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

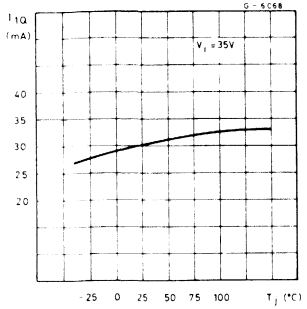


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

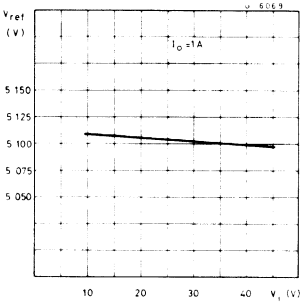


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

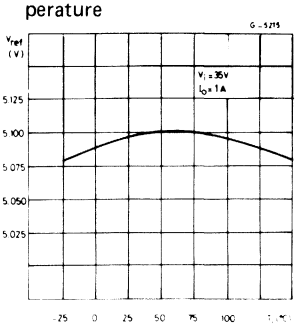


Fig. 10 - Open loop frequency and phase response of error amplifier

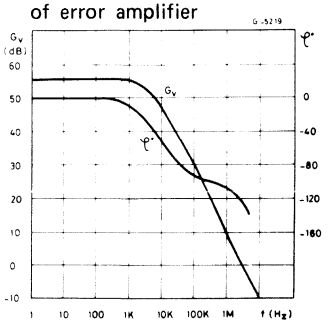


Fig. 11 - Switching frequency vs. input voltage

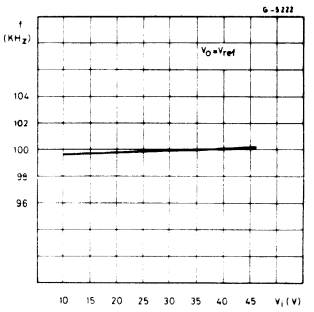


Fig. 12 - Switching frequency vs. junction temperature

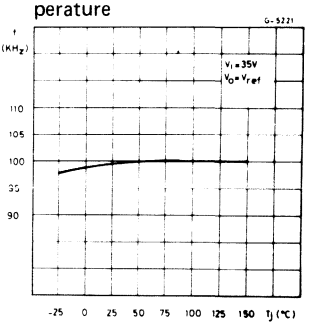


Fig. 13 - Switching frequency vs. R2 (see test circuit)

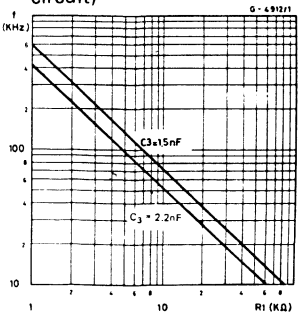


Fig. 14 - Line transient response

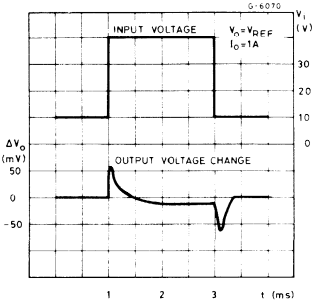


Fig. 15 - Load transient response

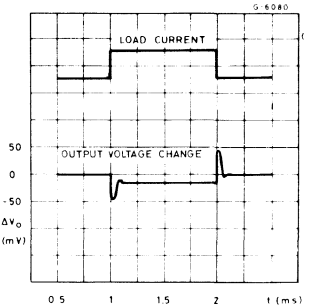


Fig. 16 - Supply voltage ripple rejection vs. frequency

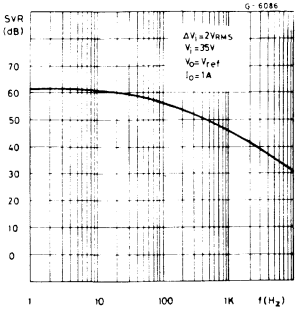


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

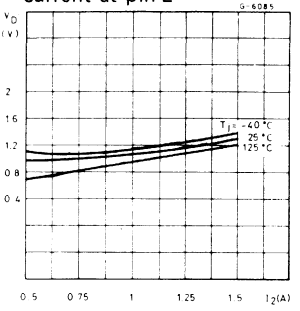


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

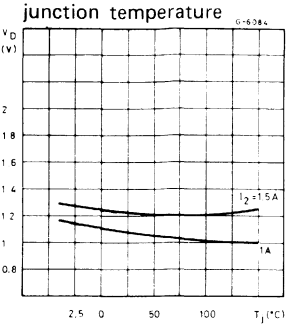


Fig. 19 - Efficiency vs. output current

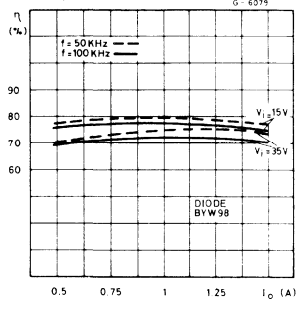


Fig. 20 - Efficiency vs. output current

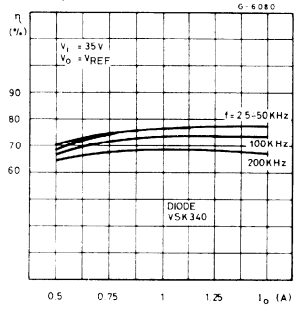


Fig. 21 - Efficiency vs. output current

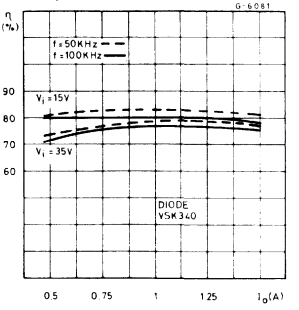


Fig. 22 - Efficiency vs. output voltage

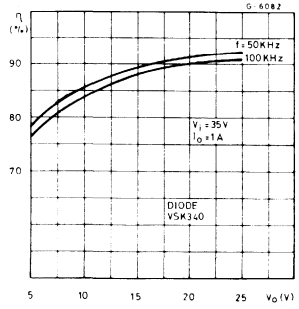


Fig. 23 - Efficiency vs. output voltage

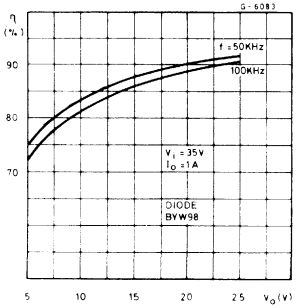
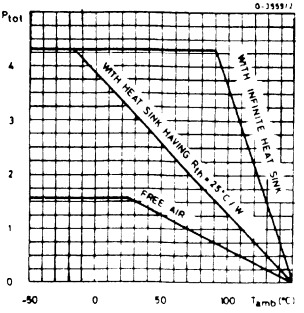
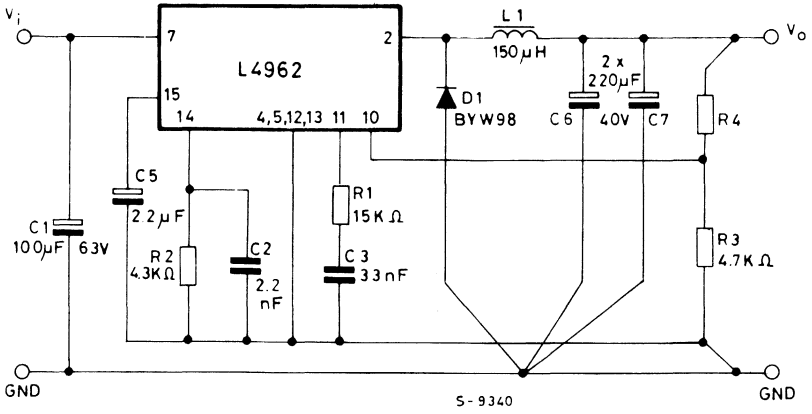


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



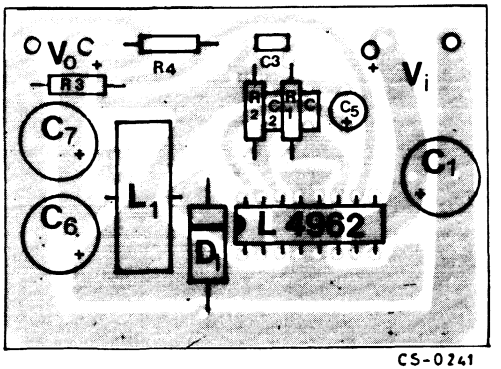
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

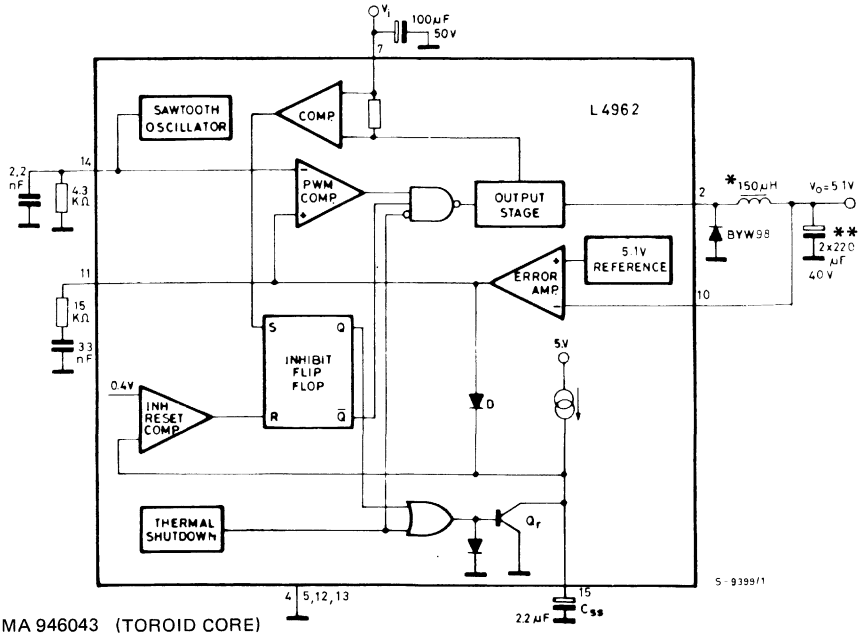
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

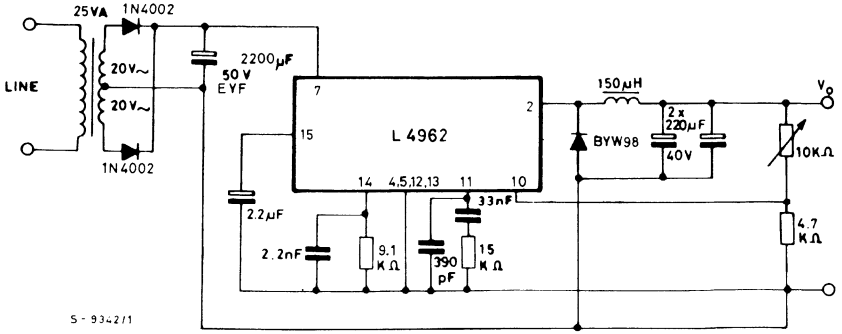
Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

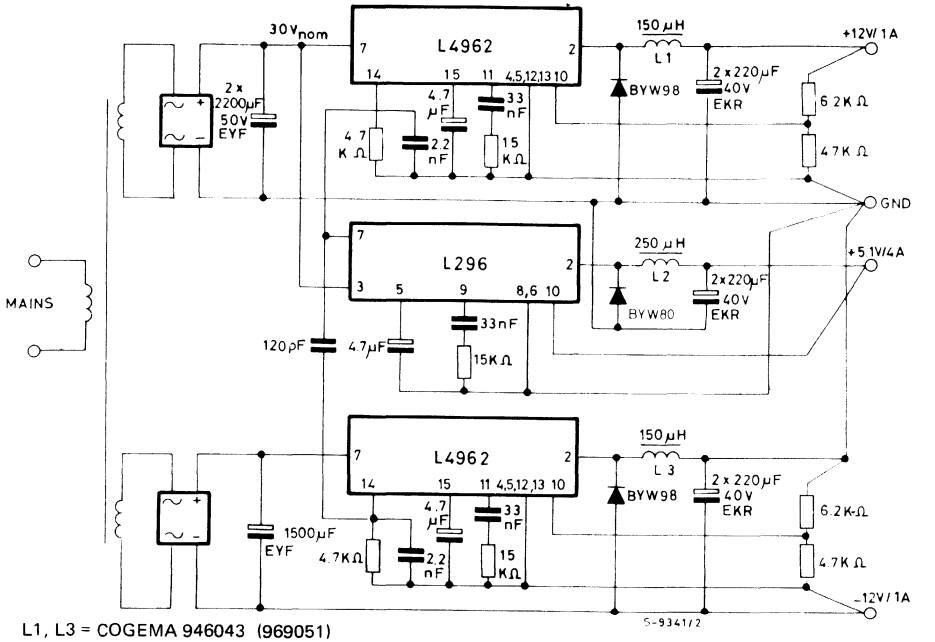
Fig. 28 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

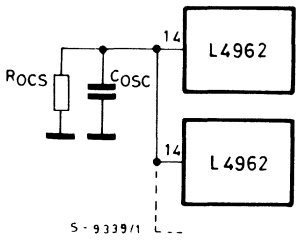
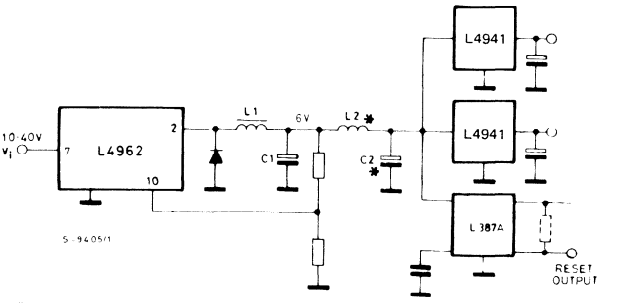


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

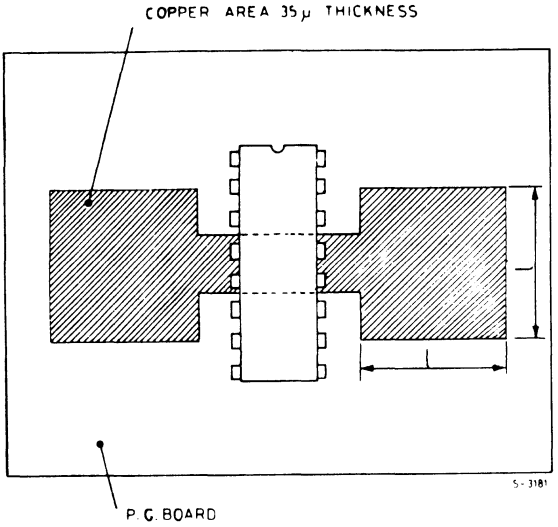
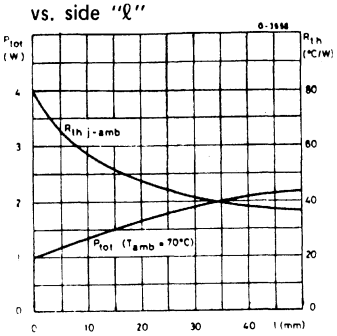
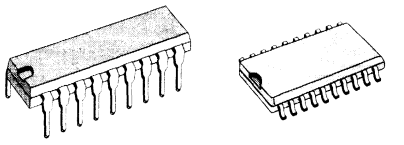


Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"



1.5A SWITCHING REGULATOR

- 1.5A OUTPUT LOAD CURRENT
- 5.1 TO 36V OUTPUT VOLTAGE RANGE
- DISCONTINUOUS VARIABLE FREQUENCY MODE
- PRECISE (+/–2%) ON CHIP REFERENCE
- VERY HIGH EFFICIENCY
- VERY FEW EXTERNAL COMPONENTS
- NO FREQ. COMPENSATION REQUIRED
- RESET AND POWER FAIL OUTPUT FOR MICROPROCESSOR
- INTERNAL CURRENT LIMITING
- THERMAL SHUTDOWN



Powerdip12+3+3 **SO20**

ORDERING NUMBERS:

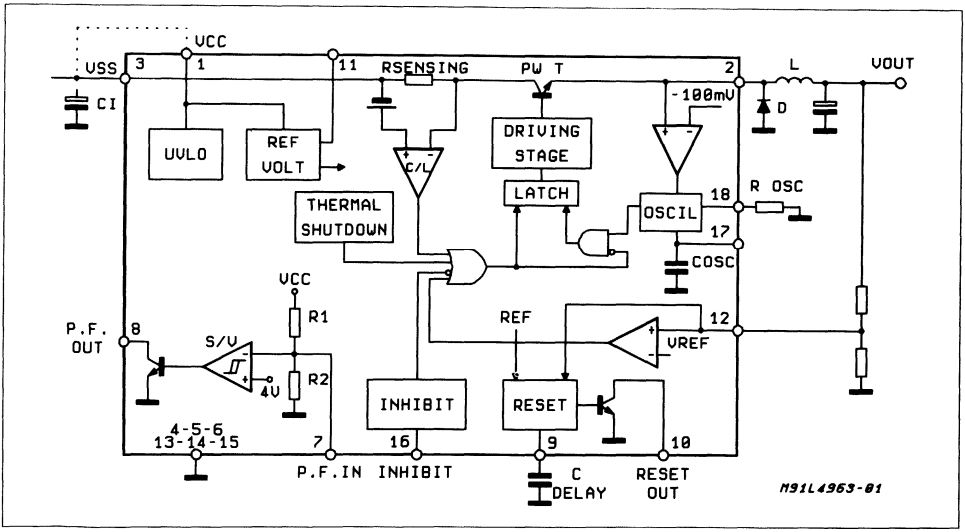
L4963W L4963D

DESCRIPTION

The L4963 is a monolithic power switching regulator delivering 1.5A at 5.1V. The output voltage is adjustable from 5.1V to 36V, working in discontinuous variable frequency mode. Features of the device include remote inhibit, internal current limiting and thermal protection, reset and power fail outputs for microprocessor.

The L4963 is mounted in a 12+3+3 lead Powerdip (L4963) and SO20 large (L4963D) plastic packages and requires very few external components.

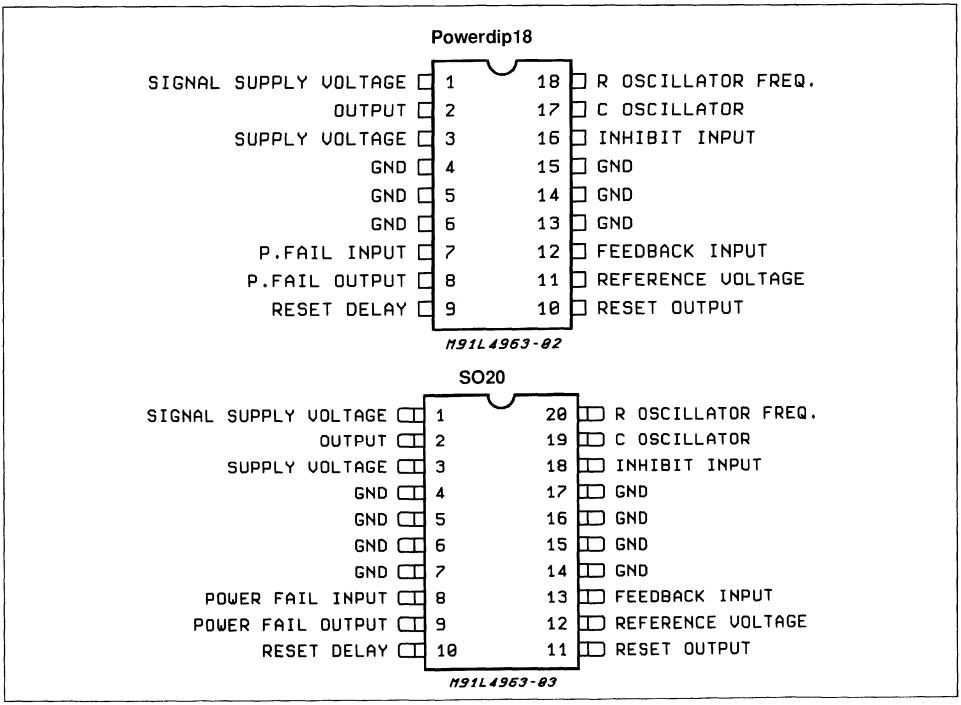
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
SO20	Powerdip			
V_i		Input Voltage (pin 1 and pin 3 connected togheter)	47	V
V_3–V_2		Input to Output Voltage Difference	47	V
V_2		Negative Output DC Voltage	–1	V
V_2		Negative Output Peak Voltage at t=0.2 µs, f=50kHz	–5	V
V_8	V_7	Power Fail Input	25	V
V_9, V_{11}	V_8, V_{10}	Reset and Power Fail Output	V_i	
V_{10}	V_9	Reset Delay Input	5.5	V
V_{13}, V_{18}	V_{12}, V_{16}	Feedback and Inhibit Inputs	7	V
V_{19}, V_{20}	V_{17}, V_{18}	Oscillator Inputs	5.5	V
P_{tot}		Total Power Dissipation Tpins ≤ 90°C (Power DIP) (T_{amb} = 70°C no copper area on PCB) (T_{amb} = 70°C, 4cm^2 copper area on PCB)	5 1.3 2	W W W
T_{stg}, T_j		Storage & Junction Temperature (Tamb = 70°C 6cm^2 copper area on PCB)	–40 to 150 1.45	°C W
P_{tot}		Total Power Dissipation Tpins ≤90°C (SO20L)	4	W

PIN CONNECTION (top view)



PIN FUNCTIONS

SO20L	Power DIP	Name	Description
1	1	SIGNAL SUPPLY VOLTAGE	Must be Connected to pin 3
2	2	OUTPUT	Regulator output
3	3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
4, 5, 6, 7 14, 15, 16, 17	4, 5, 6 13, 14, 15	GROUND	Common ground terminal
8	7	POWER FAIL INPUT	Input of the power fail circuit. The threshold can be modified introducing an external voltage divider between the Supply Voltage and GND.
9	8	POWER FAIL OUTPUT	Open collector power fail signal output. This output is high when the supply voltage is safe.
10	9	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
11	10	RESET OUTPUT	Open collector reset signal output. This output is high when the output voltage value is correct.
12	11	REFERENCE VOLTAGE	Reference voltage output.
13	12	FEEDBACK INPUT	Feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
18	16	INHIBIT INPUT	TTL level remote inhibit. A logic low level on this input disables the device.
19	17	C OSCILLATOR	Oscillator waveform. A capacitor connected between this terminal and ground modifies the maximum oscillator frequency.
20	18	R OSCILLATOR FREQ.	A resistor connected between this terminal and ground defines the maximum switching frequency.

THERMAL DATA

Symbol	Parameter		SO20	Powerdip	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction to Pins	max.	15	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient (*)	max.	85	80	°C/W

(*) See Fig. 28

CIRCUIT DESCRIPTION (Refer to Block Diagram)

The L4963 is a monolithic stepdown regulator providing 1.5A at 5.1V working in discontinuous variable frequency mode. In normal operation the device resonates at a frequency depending primarily on the inductance value, the input and output voltage and the load current. The maximum switching however can be limited by an internal oscillator, which can be programmed by only one external resistor.

The fondamental regulation loop consists of two comparators, a precision 5.1V on-chip reference and a drive latch. Briefly the operation is as follows: when the choke ends its discharge the catch freewheeling recirculation filter diode begins to come out of forward conduction so the output voltage of the device approaches ground. When the output voltage reaches –0.1V the internal comparator sets the latch and the power stage is turned on. Then the inductor current rises linearly until the voltage sensed at the feedback input reaches the 5.1V reference.

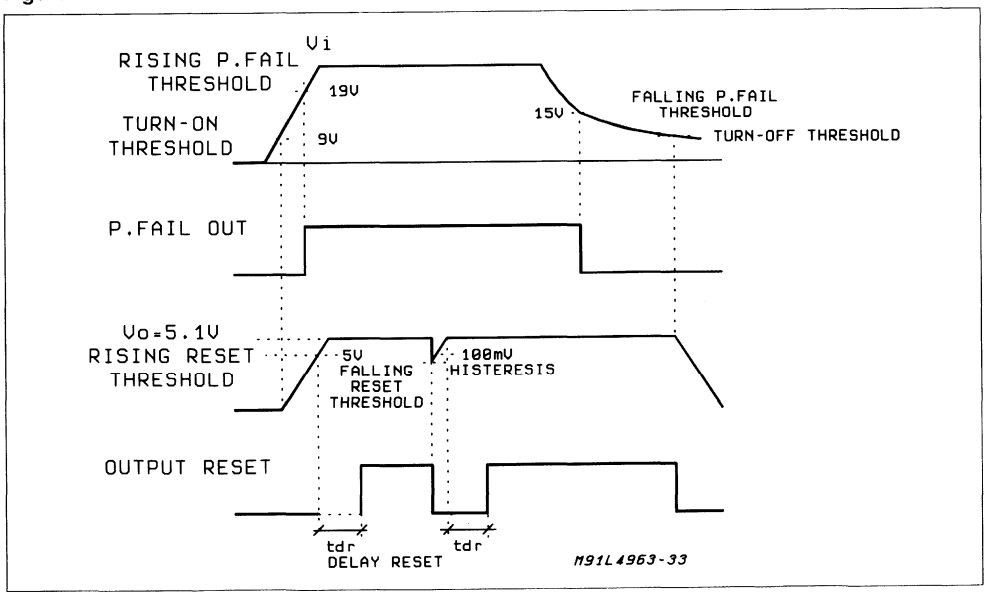
The second comparator then resets the latch and the output stage is turned off. The current in the choke falls linearly until it is fully discharged, then the cycle repeats. Closing the loop directly gives an output voltage of 5.1V. Higher output voltages are obtained by inserting a voltage divider and this method of control requires no frequency compensation network. At output voltages greater than 5.1V the available output current must be derated due to the increased power dissipation of the device.

Output overload protection is provided by an internal current limiter. The load current is sensed by a on-chip metal resistor connected to a comparator which resets the latch and turns off the power stage in overload condition. The reset circuits (see fig. 1) generates an output high signal when the output voltage value is correct. It has an open collector output and the output signal delay time can be programmed with an external capacitor. A power-fail circuit is also available and is used to monitor the supply voltage. Its output goes high when the supply voltage reaches a pre-programmed treshold set by a voltage divider to its input from the supply to ground. With the input left open the threshold is approximately equal to 5.1V. The output of the power fail is an open collector.

A TTL level inhibit is provided for applications such as remote on/off control. This input is activated by a low logic level and disables circuits operation.

The thermal overload circuit disables the device when the junction temperature is about 150°C and has hysteresis to prevent unstable conditions.

Figure 1: Reset and Power Fail Function



ELECTRICAL CHARACTERISTIC (Refer to the test circuit V_i = 30V T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS							
V_o	Output Voltage Range	V_i = 46V I_o = 0.5A	V_{ref}		36	V	2
V_i	Input Voltage Range	V_o = V_{ref} to 36V I_o = 0.5A	9		46	V	2
V_{12}	Feedback Voltage	V_i = 9 to 46V I_o = 0.5A	5	5.1	5.2	V	2
I_{12}	Input Bias Current	V_i = 15V V_{12} = 6V V_{17t} = 5V		5	20	µA	3a
V_{OS12}	Input Offset Voltage			5	10	mV	3a
ΔV_o	Line Regulation	V_i = 9 to 46V V_o = V_{ref} I_o = 0.5A		15	50	mV	2
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5 to 1.5A		15	45	mV	2
V_d	Dropout Voltage Between pin 3 and pin 2	I_2 = 3A V_i = 20V		1.5	2	V	2
I_{2L}	Current Limiting	V_i = 9 to 46V V_o = V_{ref} to 28V	3.5		6.5	A	2
I_o	Maximum Operating Load Current	V_i = 9 to 46V V_o = V_{ref}	1.5			A	2
SVR	Supply Voltage Ripple Rejection	V_i = 2Vrms V_o = V_{ref} fripple = 100Hz I_o = 1.5A	50	56		dB	2
V_{11}	Reference Voltage	V_i = 9 to 46V O < I_{11} < 5mA	5	5.1	5.2	V	3a
	Average Temperature Coefficient of Ref. Volt.	T_j = 0 to 125 °C		0.4		mV/°C	–
ΔV_{11}	V_{ref} Line Regulation	V_i = 9 to 46V		10	20	mV	3a
ΔV_{11}	V_{ref} Line Regulation	I_{ref} = 0 to 5mA V_i = 46V R_{osc} = 51KΩ	65 69	7	15	mV	3a
η	Efficiency	I_o = 1.5A V_o = V_{ref}	65	75		%	2
T_{sd}	Thermal Shutdown Junction Temperature		145	150		°C	–
	Hysteresis			30		°C	–
DC CHARACTERISTICS							
I_q	Quescent Drain Current	V_i = 46V I_o = 0mA; V_{16} = V_{12} = 0		14	20	mA	3a
		V_{16} = V_{ref} V_{12} = 5.3V		11	16	mA	3a
INHIBIT							
V_{16L}	Low Input Voltage	V_i = 9 to 46V	0.3		0.8	V	2
V_{16H}	High Input Voltage	V_i = 9 to 46V	2		5.5	V	2
I_{16L}	Input Current with Low Input Voltage	V_{16} = 0.8V		50	100	µA	2
I_{16L}	Input Current with High Input Voltage	V_{16} = 2V		10	20	µA	2

ELECTRICAL CHARACTERISTIC (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
RESET							
V_{12}	Rising Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –100	V_{ref} –50	mV	3b
V_{12}	Falling Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –200	V_{ref} –250	mV	3b
V_{9D}	Delay Rising Thereshold Voltage	V_7 = OPEN	4.3	4.5	4.7	V	3b
V_{9F}	Delay Falling Thereshold Voltage		1	1.5	2	V	3b
$-I_{9SO}$	Delay Source Current	V_9 = 4.7V V_{12} = 5.3V	70	110	140	µA	3b
I_{9SI}	Delay Sink Current	V_9 = 4.7V V_{12} = 4.7V	10			mA	3b
I_{10}	Output Leakage Current	V_i = 46V V_7 = 8.5V	50			µA	3b
V_{10}	Output Saturation Volt.	I_{10} = 15mA; V_I = 3 to 46V			0.4	V	3b
POWER FAIL							
V_R	Rising Threshold Voltage	Pin7 = open	17.5	19	20.5	V	3C
V_F	Falling Threshold Voltage	Pin7 = open	14.25	15	15.75	V	3c
V_7	Rising Threshold Voltage	V_i = 20V	4.14	4.5	4.86	V	–
V_7	Falling Threshold Voltage	V_i = 20V	3.325	3.5	3.675	V	–
V_s	Output Saturation Volt.	I_a = 5mA			0.4	V	3c
I_s	Output Leakage Current	V_i = 46V			50	µA	3c
OSCILLATOR							
f	Oscillator Frequency	R_T = 51KΩ	46	60	79	kHz	–
f	Oscillator Frequency	V_I = 9 to 46V T_j = 0 to 125°C R_T = 51KΩ	42		83	kHz	–

Figure 2: Test Circuit

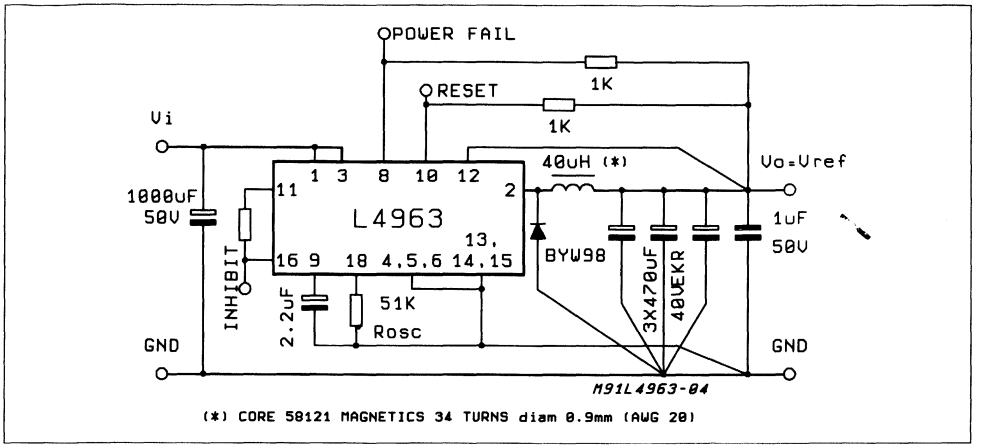


Figure 3: DC Test Circuit

Figure 3a

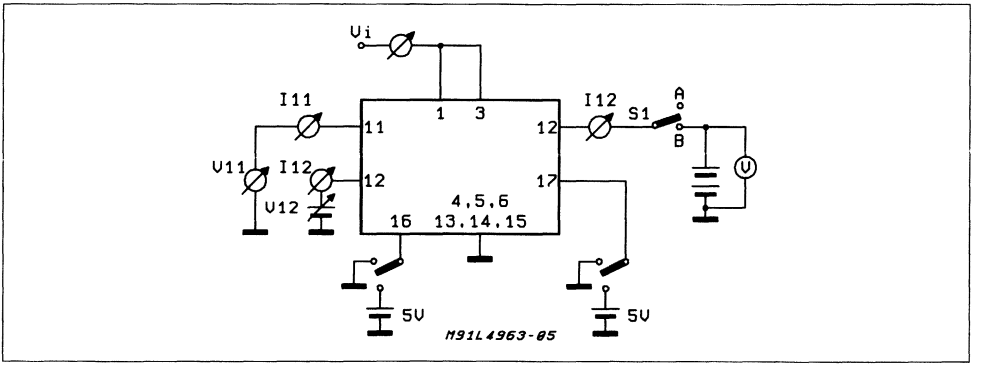


Figure 3b

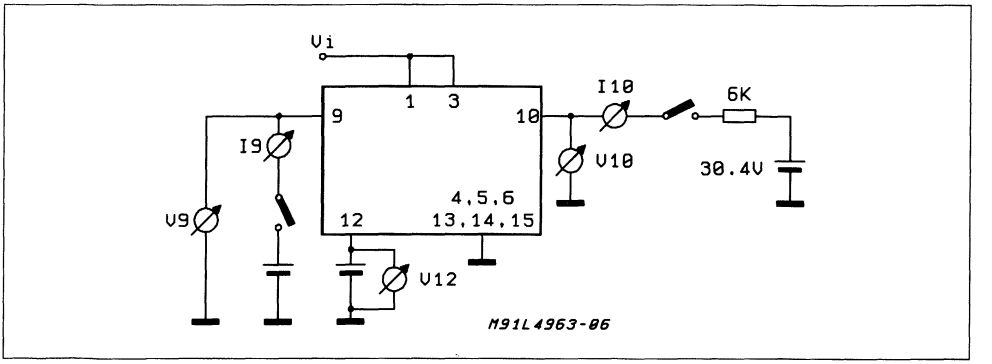


Figure 3c

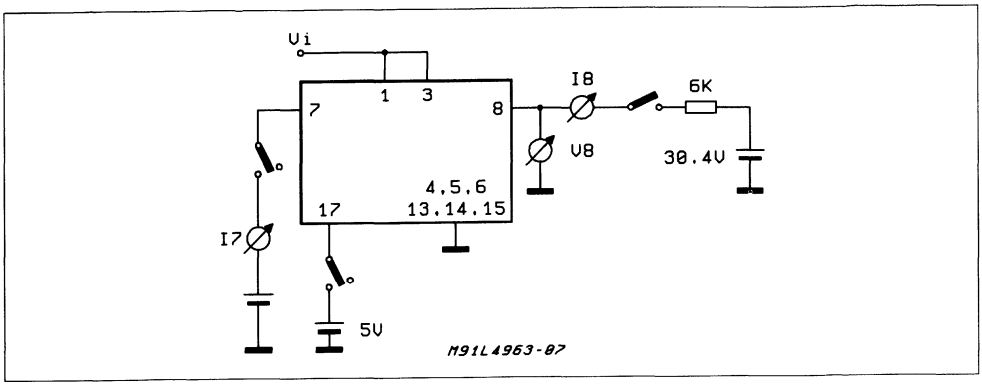


Figure 4: Quiescent Drain Current vs. Supply Voltage (0% Duty Cycle)

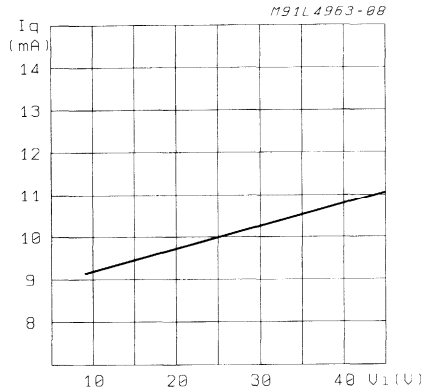


Figure 5: Quiescent Drain Current vs. Supply Voltage (100% Duty Cycle)

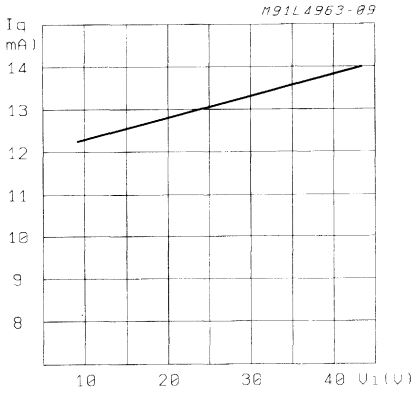


Figure 6: Quiescent Drain Current vs. Junction Temperature (0% Duty Cycle)

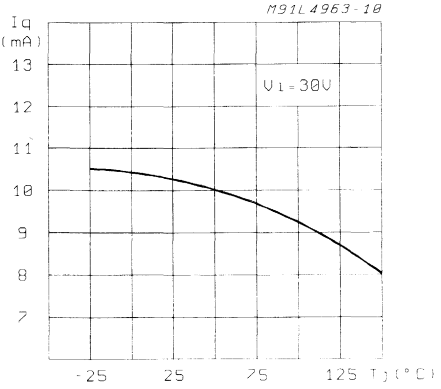


Figure 7: Quiescent Drain Current vs. Junction Temperature (100% Duty Cycle)

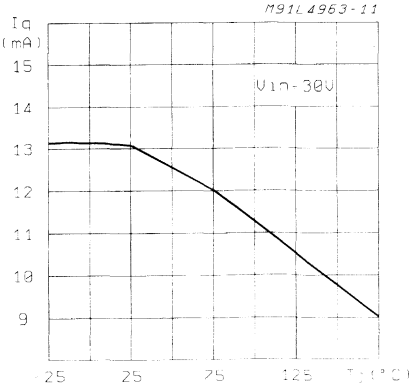


Figure 8: Reference Voltage vs. V_i

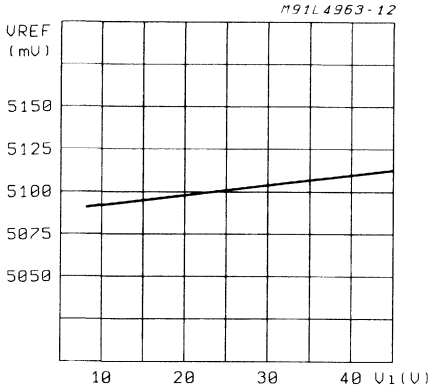


Figure 9: Reference Voltage vs. T_j

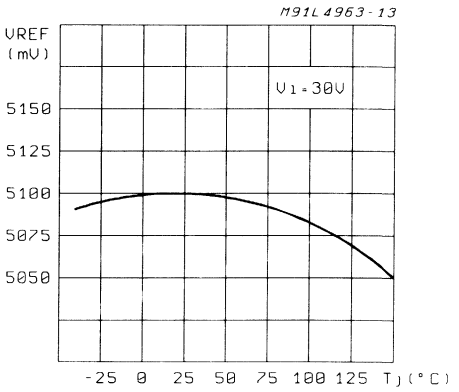


Figure 10: Line Transient Response

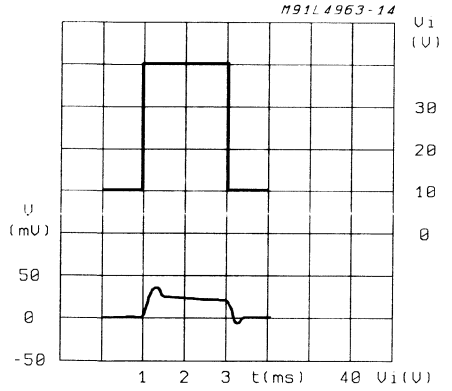


Figure 11: Load Transient

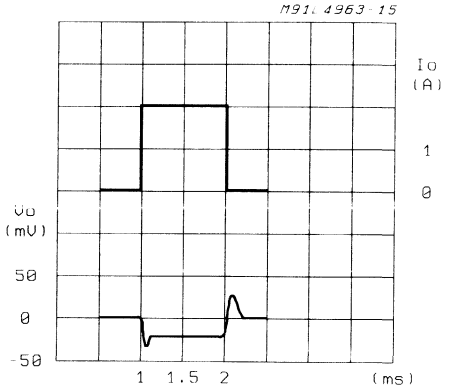


Figure 12: Supply Voltage Ripple Rejection vs. Frequency

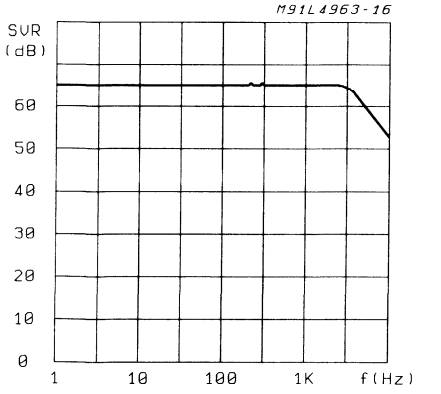


Figure 13: Dropout Voltage Between pi3 and 2 vs. Current at pin2

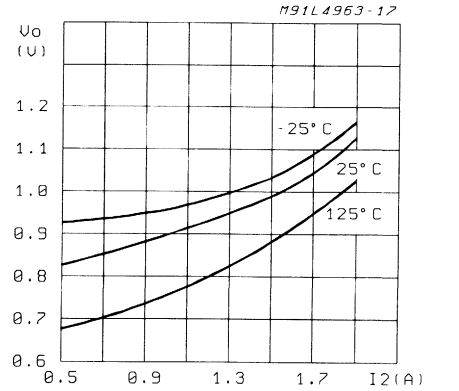


Figure 14: Dropout Voltage Between pin3 and 2 vs. Junction Temperature

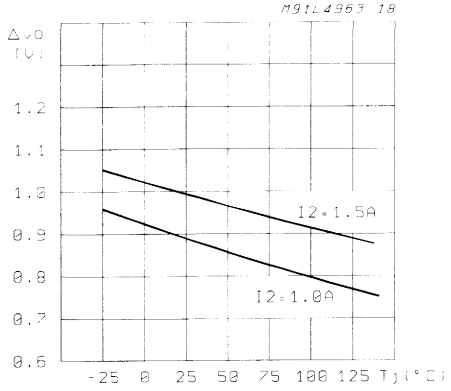


Figure 15: Maximum Allowable PowerDissipation vs. Ambient Temperature (Powerdip Package Only)

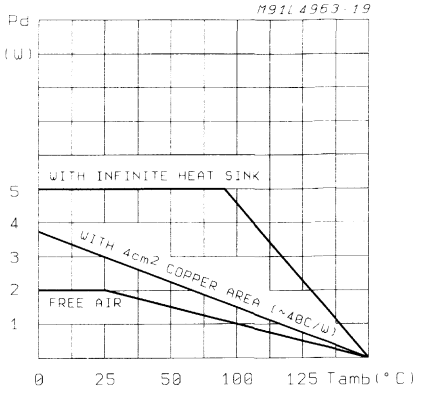


Figure 16: Power Dissipation (device only) vs. Input Voltage (Powerdip Package Only)

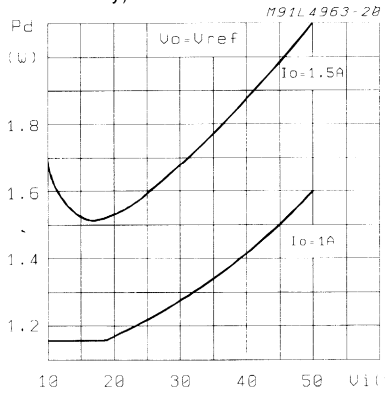


Figure 17: Power Dissipation (device only) vs. Output Voltage (Powerdip Package Only)

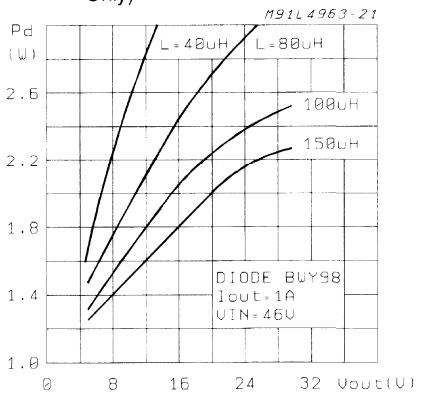


Figure 18: Voltage and Current Waveform at pin2

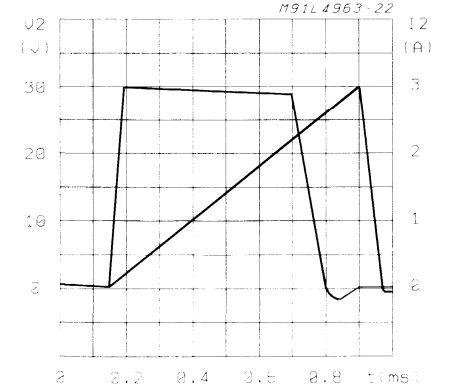


Figure 19: Efficiency vs. Output Current (Powerdip Package Only)

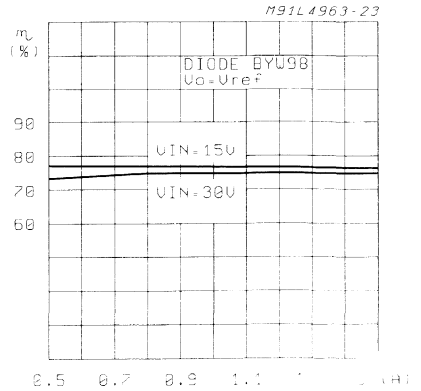


Figure 20: Efficiency vs. Output Voltage (Power-dip Package Only)

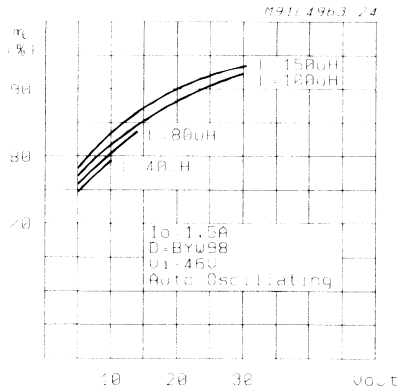


Figure 21: Current Limit vs. Junction Temperature V_I = 30V

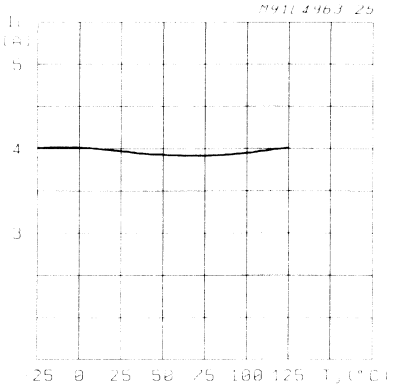


Figure 22: Current Limit vs. Input Voltage

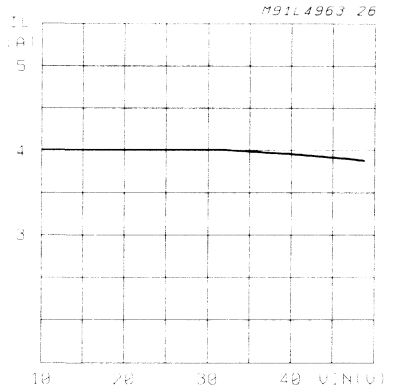


Figure 23: Oscillator Frequency vs. R2 (see fig. 26)

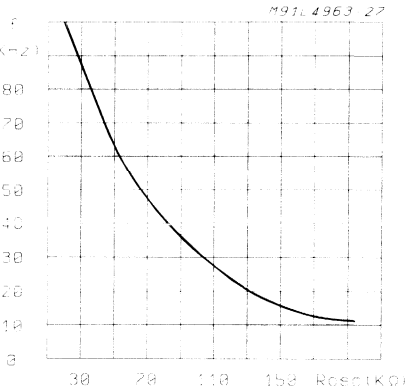


Figure 24: Oscillator Frequency vs. Junction Temperature

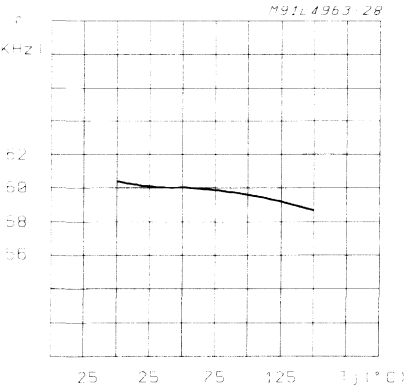


Figure 25: Oscillator Frequency vs. Input Voltage

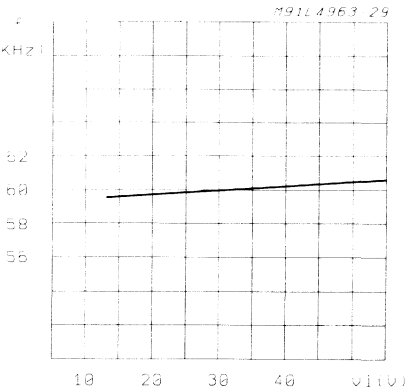
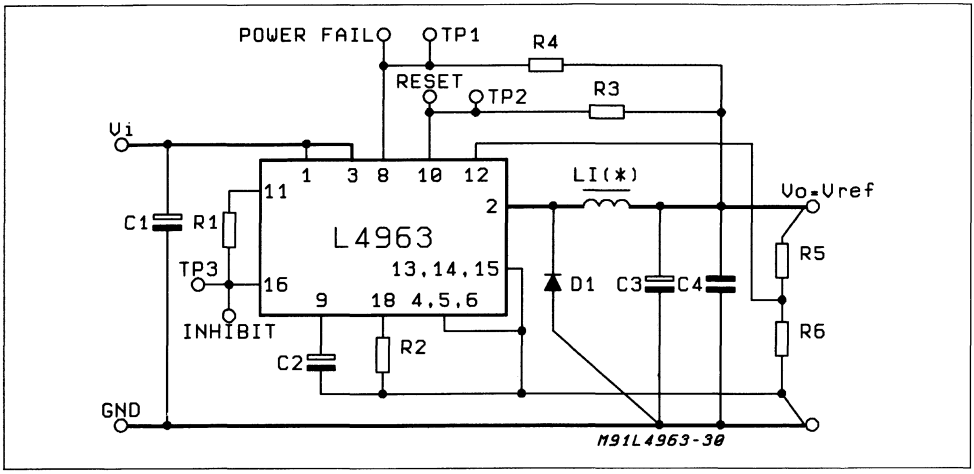


Figure 26: Evaluation Board Circuit



PART LIST

CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2mF 16V
C3	1000µF 40V with low ESR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
V_O	R6	R5
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP 34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 27: P.C. Board and Component Layout of the Circuit of fig. 26 (Powerdip Package) (1:1 scale).

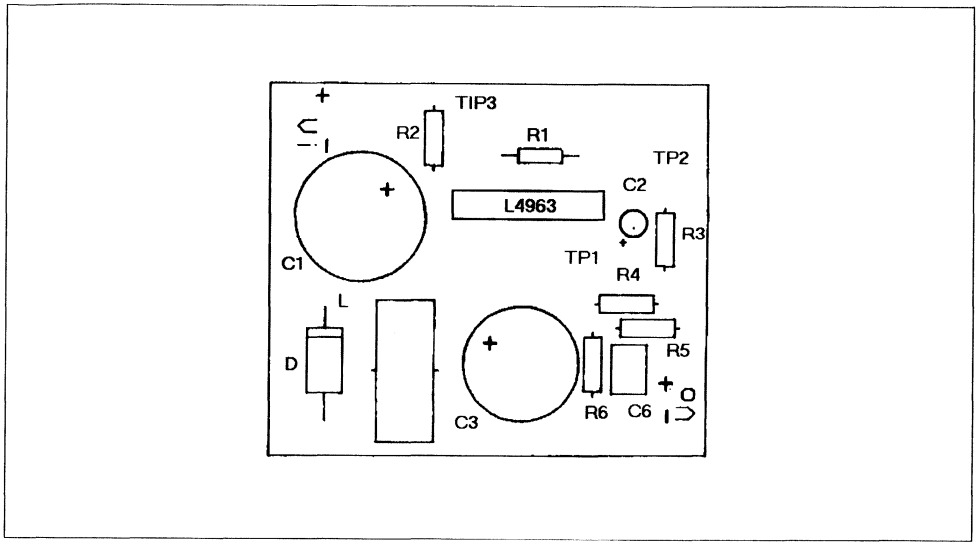


Figure 28: Thermal Characteristics

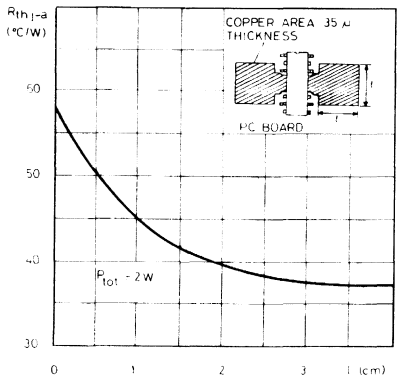


Figure 29: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

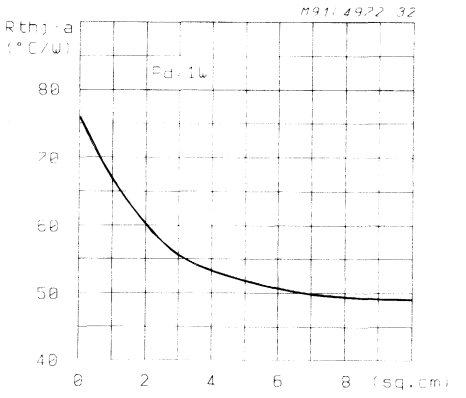


Figure 30: A Minimal 5.1 Fixed Regulator — Very Few Components are Required

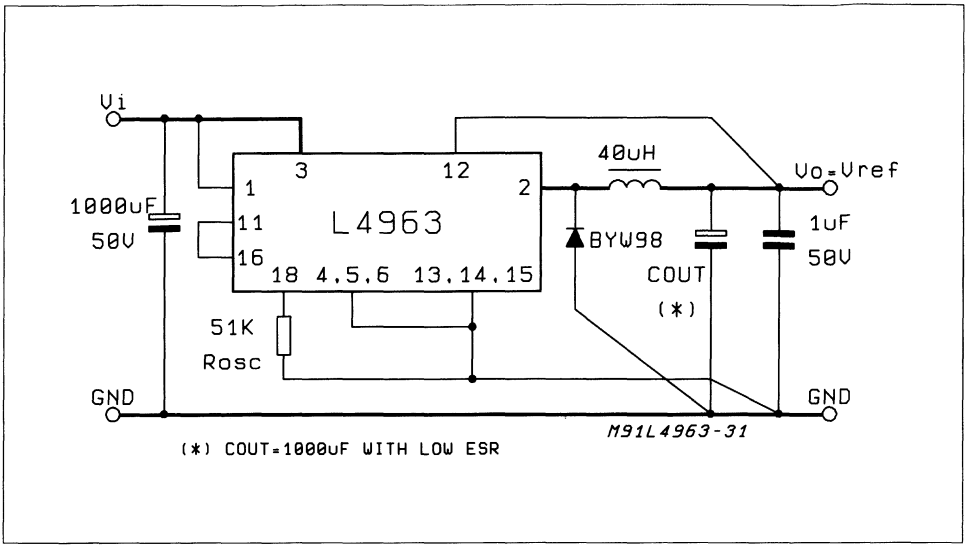
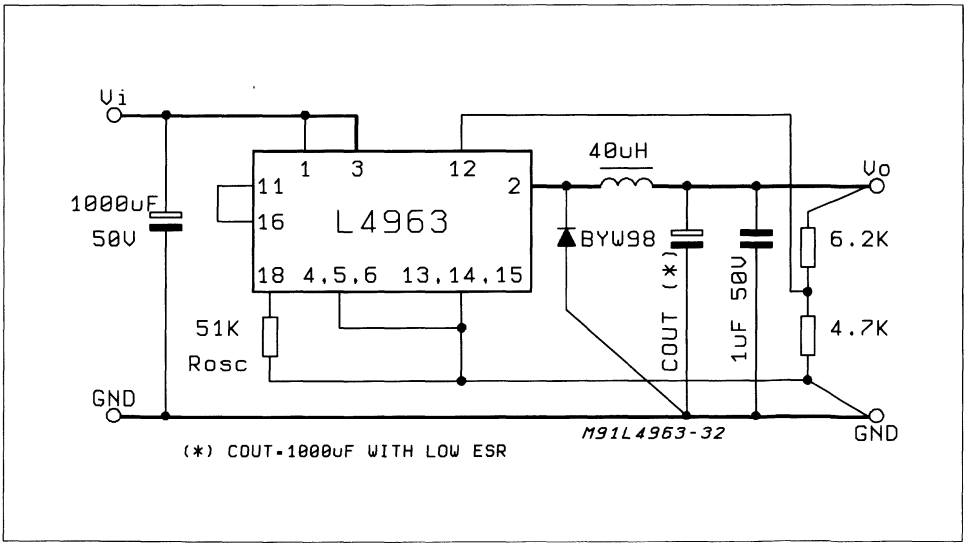


Figure 31: A Minimal Components count for V_O = 12V



HIGH CURRENT SWITCHING REGULATOR

- 4 A OUTPUT CURRENT
- 5.1 V TO 28 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (± 3 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 120 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- CURRENT LIMITING
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

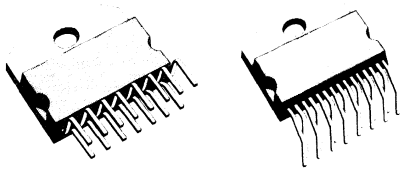
The L4964 is a stepdown power switching regulator delivering 4 A at a voltage variable from 5.1 V to 28 V.

Features of the device include overload protection, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L4964 is mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

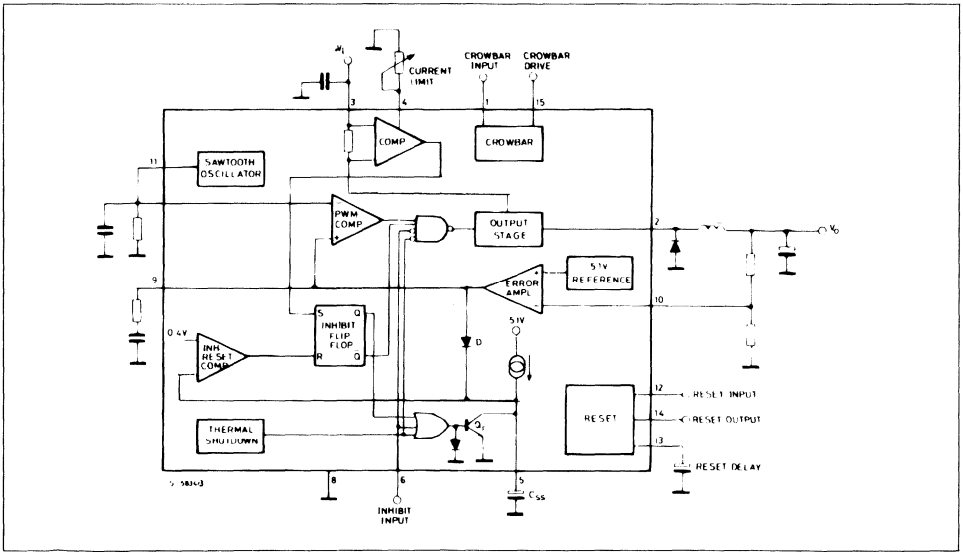
Efficient operation at switching frequencies up to 120 KHz allows a reduction in the size and cost of external filter components.

Multiwatt
(15-lead)



ORDER CODES : L4964
L4964HT

BLOCK DIAGRAM



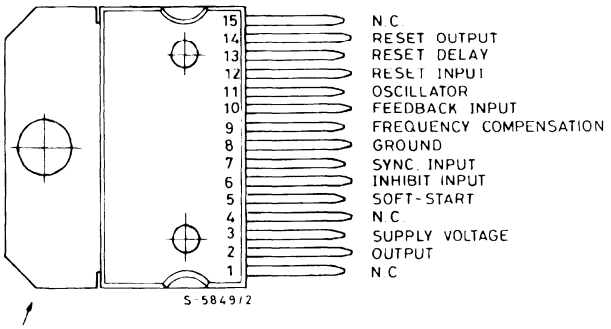
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage (pin 3)	36	V
$V_i - V_2$	Input to Output Voltage Difference	38	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 100 kHz	−1 −7	V V
V_{12}	Voltage at Pin 12	10	V
V_5, V_7, V_9	Voltage at Pins 5, 7 and 9	5.5	V
V_{10}, V_6, V_{13}	Voltage at Pins 10, 6 and 13	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	− 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

CONNECTION DIAGRAM (top view)



Note : Pins 1, 4, 15 must not be connected. Leave open circuit.

PIN FUNCTIONS

N°	Name	Function
1	N.C.	Must not be connected. Leave open circuit.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unregulated Voltage Input. An internal regulator powers the L4964's internal logic.
4	N.C.	Must not be connected. Leave open circuit.
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL - Level Remote Inhibit. A logic high level on this input disables the L4964.
7	SYNC INPUT	Multiple L4964's are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. The pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the beedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open Collector Reset Signal Output. This output is high when the supply is safe.
15	N.C.	Must not be connected. Leave open circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L4964 is a monolithic stepdown switching regulator providing output voltages from 5.1 V to 28 V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 3 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be ajusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enable and the output voltage rises under contro of the soft start network. If the overload condition is still present the limiter will trigger again when the thershold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

A TTL - level input is provided for applications such as remote on/off control. This input is activated by high level and disables circuit operation. After an inhibit the L4964 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.

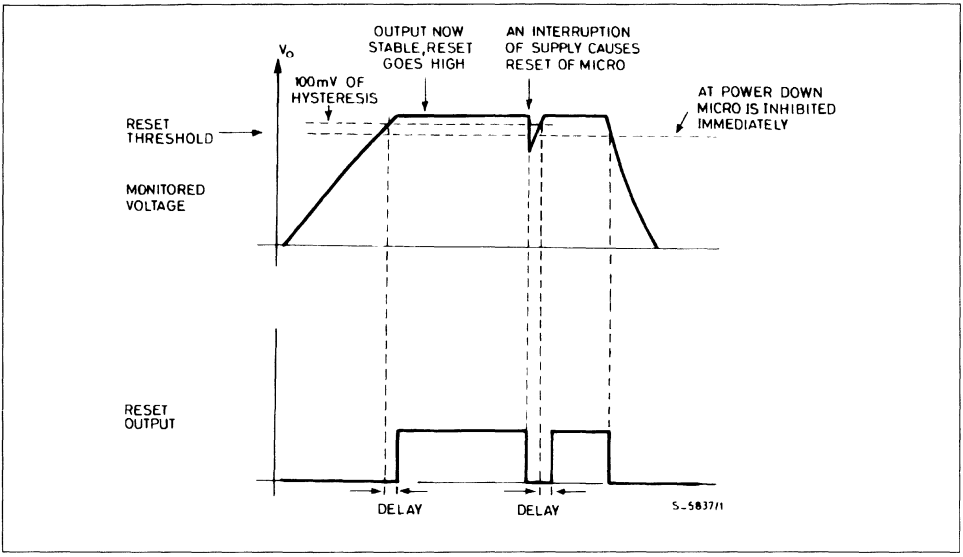


Figure 2 : Soft Start Waveforms.

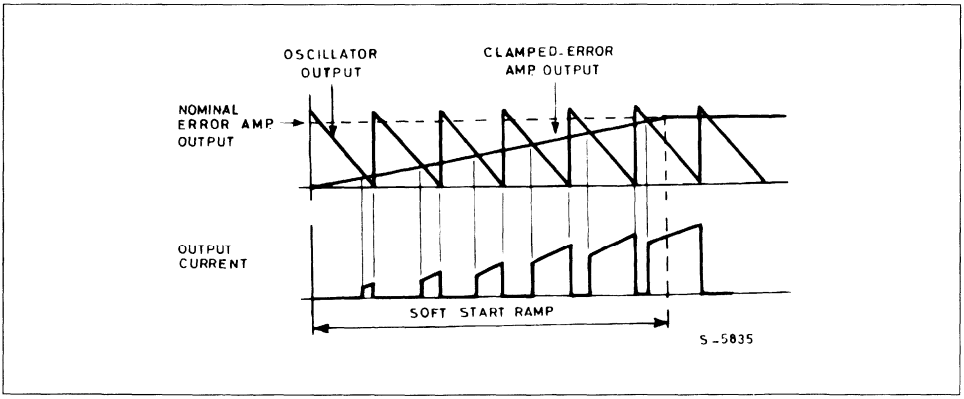
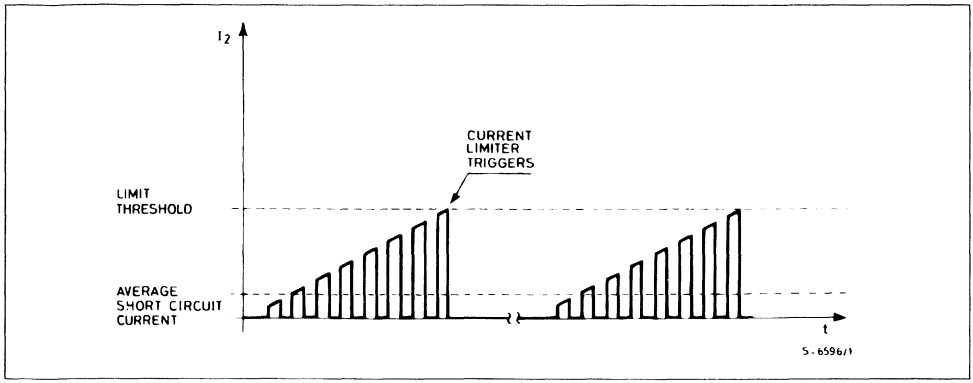


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 25 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)

V_o	Output Voltage Range	V_i = 36 V I_o = 1 A	V_{ref}		28	V	4
V_i	Input Voltage Range	V_o = V_{ref} to 28 V I_o = 3 A	9		36	V	4
ΔV_o	Line Regulation	V_i – 10 V to 30 V, V_o – V_{ref}, I_o = 2 A		15	70	mV	4
ΔV_o	Load Regulation	I_o = 1 A to 2 A		10	30	mV	4
		V_o = V_{ref} I_o = 0.5 A to 3 A		15	50	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 36 V I_o = 2 A	4.95	5.1	5.25	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/°C	
V_d	Dropout Voltage between Pin 2 and Pin 3	I_o = 3 A		2	3.2	V	4
		I_o = 2 A		1.5	2.4	V	4
Io_m	Maximum Operating Load Current	V_i = 9 V to 36 V, V_o = V_{ref} to 28 V	4			A	4
I_{2L}	Current Limiting Threshold (pin 2)	V_i = 9 V to 36 V V_o = V_{ref} to 28 V	4.5		8	A	4
I_{SH}	Input Average Current	V_i = 36 V ; Output Short-circuited		80	140	mA	4

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (continued)

η	Effiency	I_o = 3 A	$V_o = V_{ref}$		75		%	4
			V_o = 12 V		85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_I = 2 V_{rms} $V_o = V_{ref}$	f_{ripple} = 100 Hz I_o = 2 A	46	56	–	dB	4
f	Switching Frequency			40	50	60	kHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9 V to 36 V			0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0 °C to 125 °C			1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$ I_o = 1 A		120			kHz	–
T_{sd}	Thermal Shutdown Junction Temperature			135	145		°C	–

DC CHARACTERISTICS

I_{3Q}	Quiescent Drain Current	V_i = 36 V V_7 = 0 V S1 : B S2 : B	V_6 = 0		66	100	mA	6a
			V_6 = 3 V		30	50	mA	6a
$-I_{2L}$	Output Leakage Current	V_i = 36 V, V6 = 3 V, S1 : B, S2 : A, V_7 = 0 V				2	mA	6a

SOFT START

I_{5so}	Source Current	V_6 = 0 V,	V_5 = 3 V	80	130	180	µA	6b
I_{5si}	Sink Current	V_6 = 3 V,	V_5 = 3 V	40	70	140	µA	6b

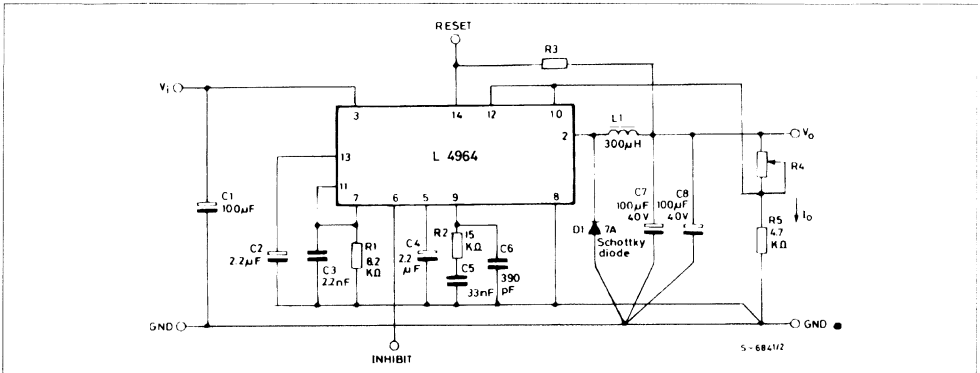
INHIBIT

V_{6L}	Low Input Voltage	V_i = 9 V to 36 V V_7 = 0 V	S1 : B S2 : B	– 0.3		0.8	V	6a
V_{6H}	High Input Voltage			2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	V_i = 9 V to 36 V V_7 = 0 V	V_6 = 0.8 V			20	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	S1 : B S2 : B	V_6 = 2 V			10	µA	6a

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
ERROR AMPLIFIER							
V_{9H}	High Level Output Voltage	V_{10} = 4.7 V, I_9 = 100 µA, S1 : A, S2 : A	3.4			V	6c
V_{9L}	Low Level Output Voltage	V_{10} = 5.3 V, I_9 = 100 µA, S1 : A, S2 : E			0.6	V	6c
$I_{9\,si}$	Sink Output Current	V_{10} = 5.3 V, S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	V_{10} = 4.7 V, S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	V_{10} = 5.2 V S1 : B		2	20	µA	6c
G_v	DC Open Loop Gain	V_9 = 1 V to 3 V, S1 : A, S2 : C	40	55		dB	6c
OSCILLATOR AND PWM COMPARATOR							
$-I_7$	Input Bias Current of PWM Comparator	V_7 = 0.5 V to 3.5 V			10	µA	6a
$-I_{11}$	Oscillator Source Current	V_{11} = 2 V, S1 : A, S2 : B	4		–	mA	6a
RESET							
V_{12R}	Rising Threshold Voltage	V_i = 9 V to 36 V, S1 : B, S2 : B,	V_{ref} −150mV	V_{ref} −100mV	V_{ref} −50mV	V	6d
V_{12F}	Falling Threshold Voltage		4.75	V_{ref} −150mV	V_{ref} −100mV	V	6d
V_{13D}	Delay Threshold Voltage	V_{12} = 5.3 V, S1 : A, S2 : B	4.3	4.5	4.7	V	6d
V_{13H}	Delay Threshold Voltage Hysteresis			100		mV	6d
V_{14S}	Output Saturation Volt.	I_{14} = 5 mA ; V_{12} = 4.7 V ; S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	V_{12} = 0 V to V_{ref}, S1 : B, S2 : B		1	10	µA	6d
$-I_{13\,so}$	Delay Source Current	V_{13} = 3 V, S1 : A, S2 : B; V_{12} = 5.3 V	60	110	150	µA	6d
$I_{13\,si}$	Delay Sink Current	V_{13} = 3 V, S1 : A, S2 : B; V_{12} = 4.7 V	8			mA	6d
I_{14}	Output Leakage Current	V_i = 36 V, V_{12} = 5.3 V, S1 : B, S2 : A			100	µA	6d

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A
R = 500 mΩ

Core type : MAGNETICS 58930 - A2 MPP
N turns : 43 Wire Gauge : 1 mm (18 AWG)

Figure 5 : PC. Board and Component Layout of the Circuit of Fig. 4 (1:1 scale).

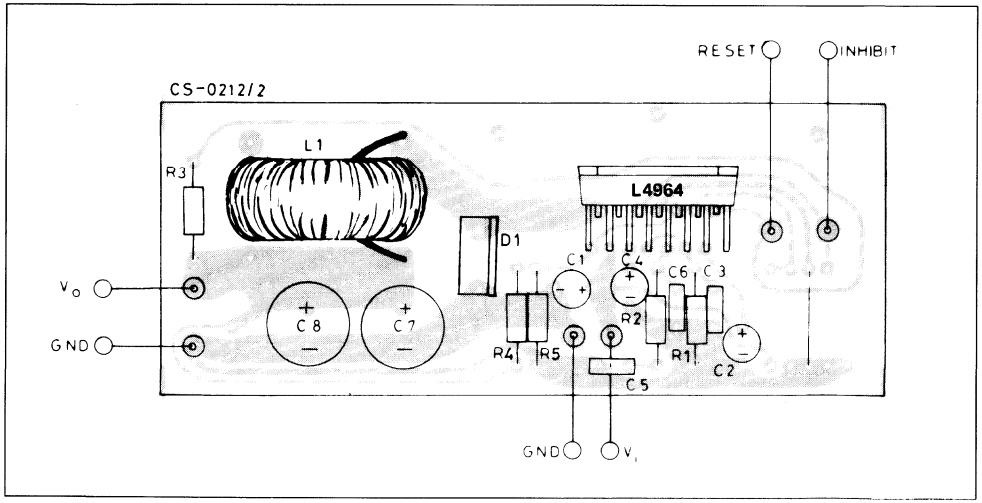


Figure 6 : DC Test Circuits.

Figure 6a.

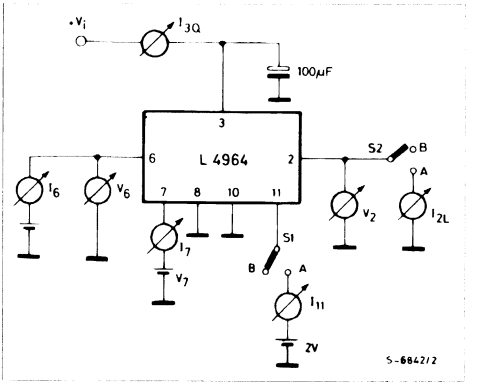


Figure 6b.

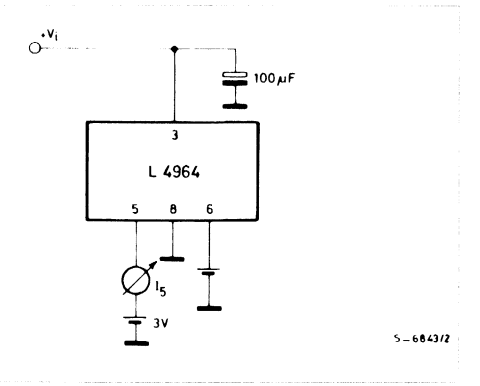
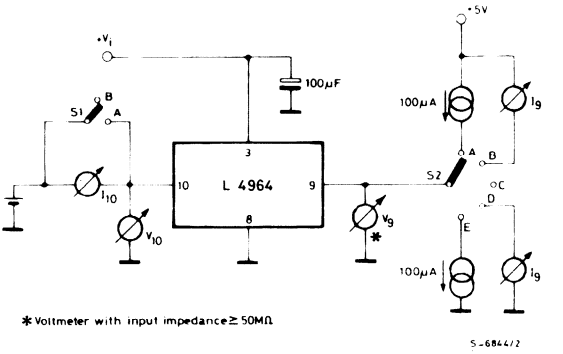


Figure 6c.



1 - Set V_{10} FOR V_9 = 1 V

2 - Change V_{10} to obtain V_9 = 3 V

3 - $G_V = \frac{DV_9}{\Delta V_{10}} = \frac{2\ V}{\Delta V_{10}}$

* Voltmeter with input impedance ≥ 50MΩ

Figure 6d.

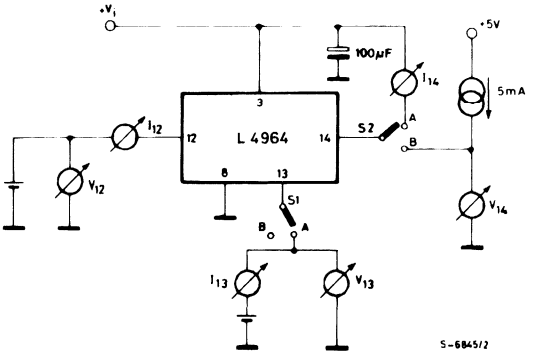


Figure 7 : Switching Frequency vs. R1 (see fig. 4).

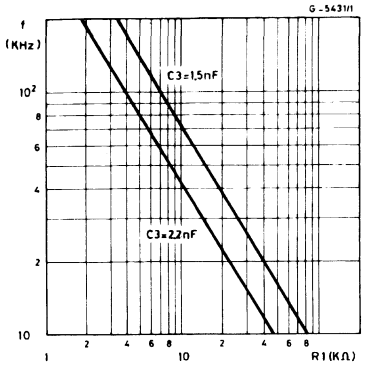


Figure 8 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

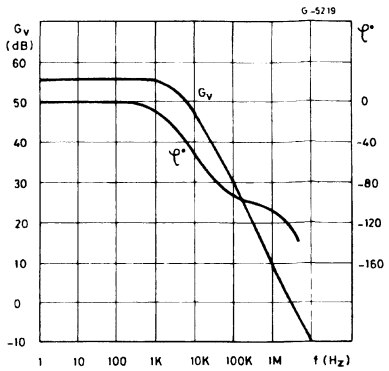


Figure 9 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

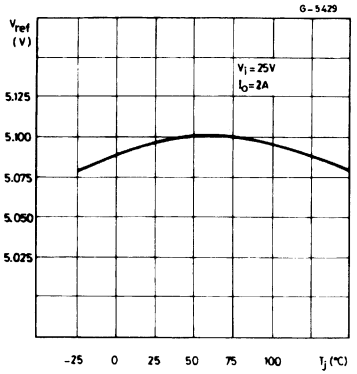


Figure 10 : Power Dissipation (L4964 only) vs. Input Voltage.

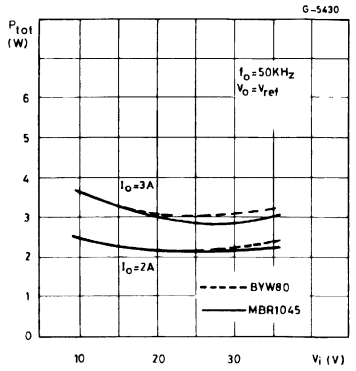


Figure 11 : Efficiency vs. Output Voltage.

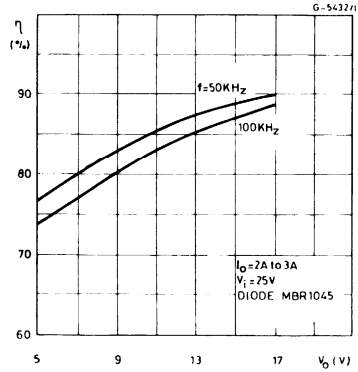
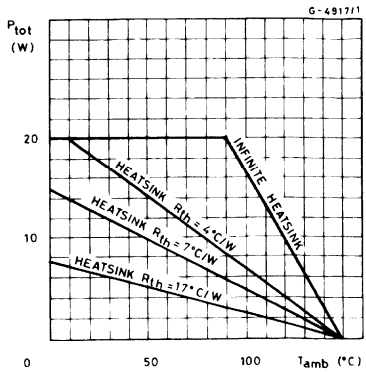


Figure 12 : Power Dissipation Derrating Curve.



APPLICATION INFORMATION

CHOOSING THE INDUCTOR AND CAPACITOR

The input and output capacitors of the L4964 must have a low ESR and low inductance at high current ripple.

Preferably, the inductor should be a toroidal type or wound on a Moly-Permalloy nucleus.Saturation must not occur at current levels below 1.5 times the current limiter level. MPP nuclei have very soft saturation characteristics.

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

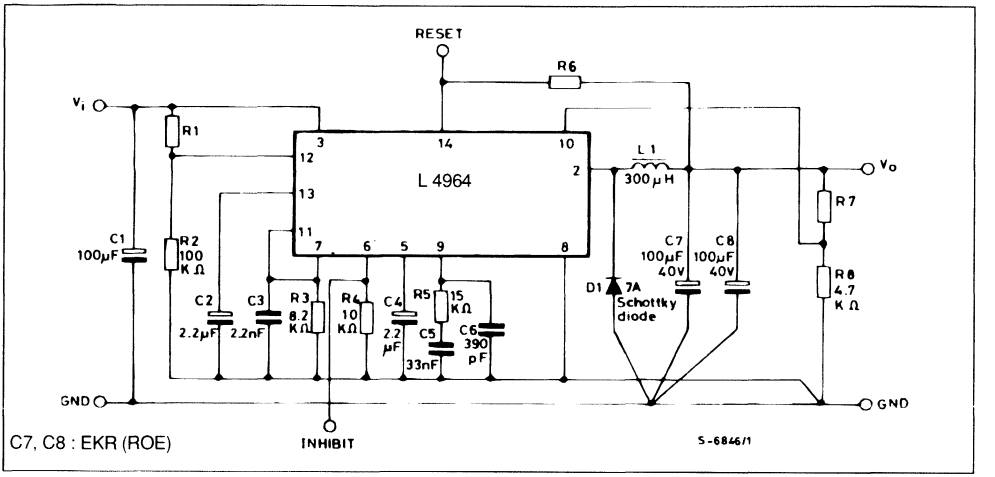
$$C = \frac{(V_i - V_o)\, V_o}{8L\, f^2\, \Delta V_o}$$

F = frequency

ΔI_L = Inductance current ripple

ΔV_o = Output ripple voltage

Figure 13 : Typical Application Circuit.

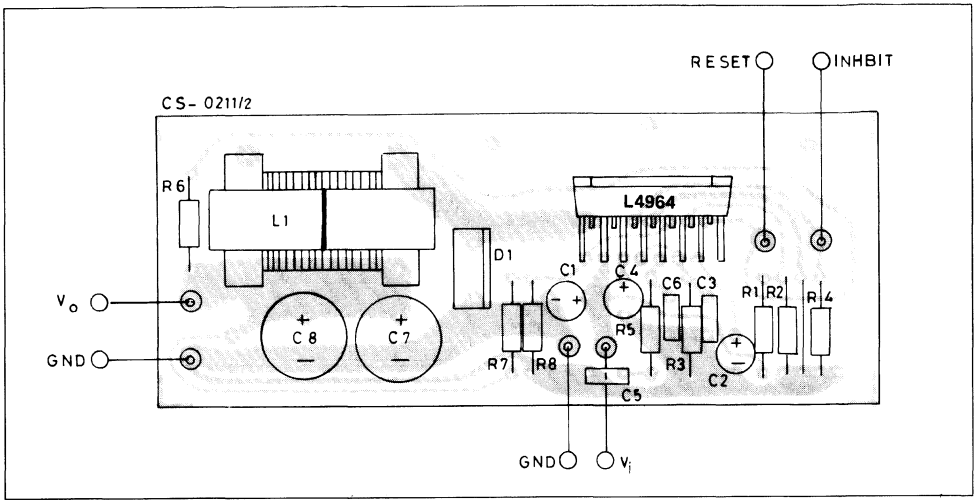


SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	50	0.8 mm	0.7 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages		
V_O	R8	R7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ

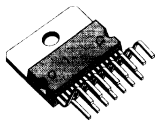
Figure 14 : P.C. Board and Component Layout of the Circuit of Fig. 13 (1:1 scale).



10A SWITCHING REGULATOR

- 10A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



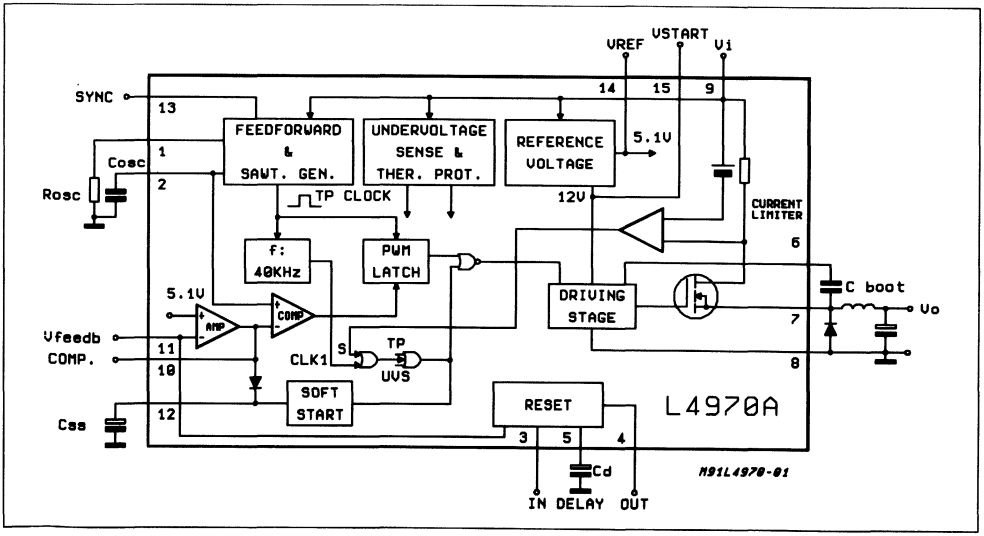
Multiwatt15V
ORDERING NUMBER: L4970A

DESCRIPTION

The L4970A is a stepdown monolithic power switching regulator delivering 10A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

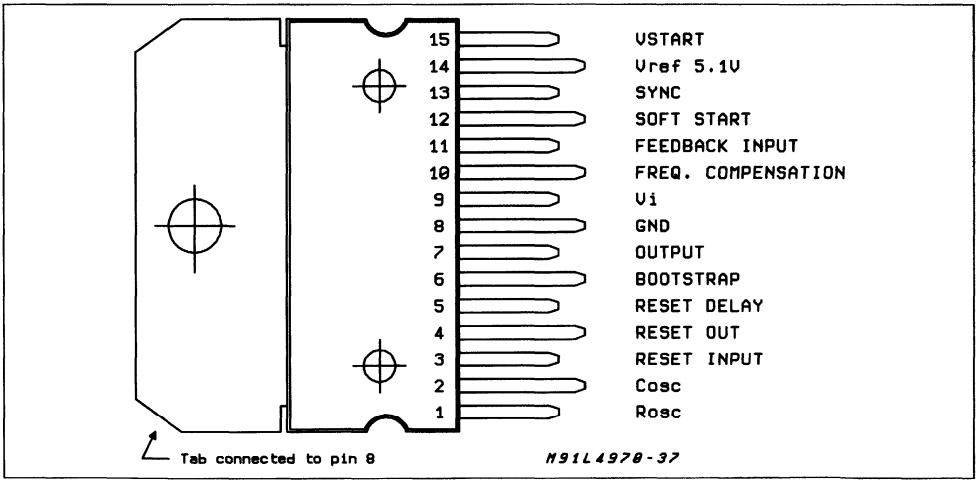
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4970A are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4970A is a 10A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 10A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

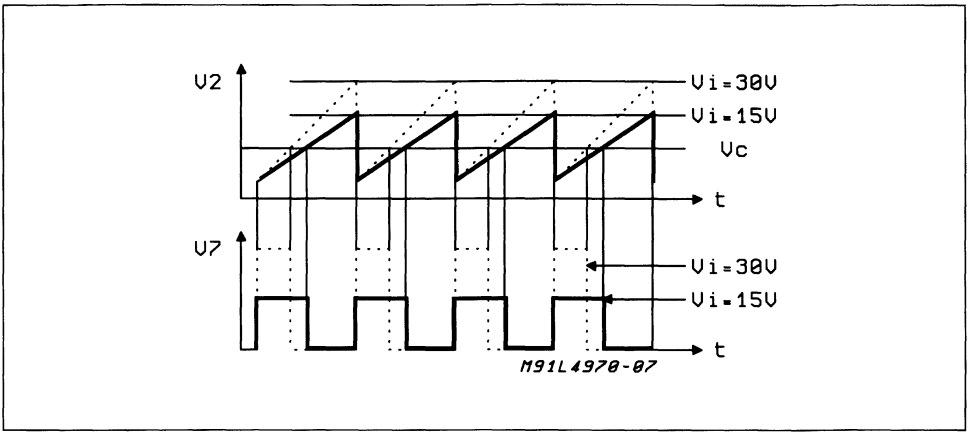


Figure 2: Soft Start Function

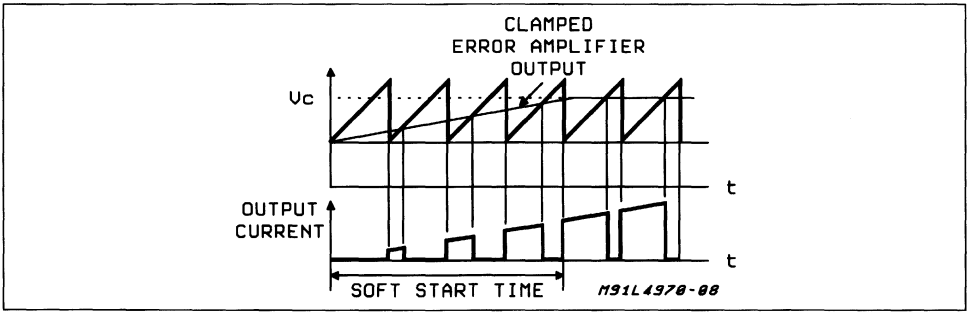
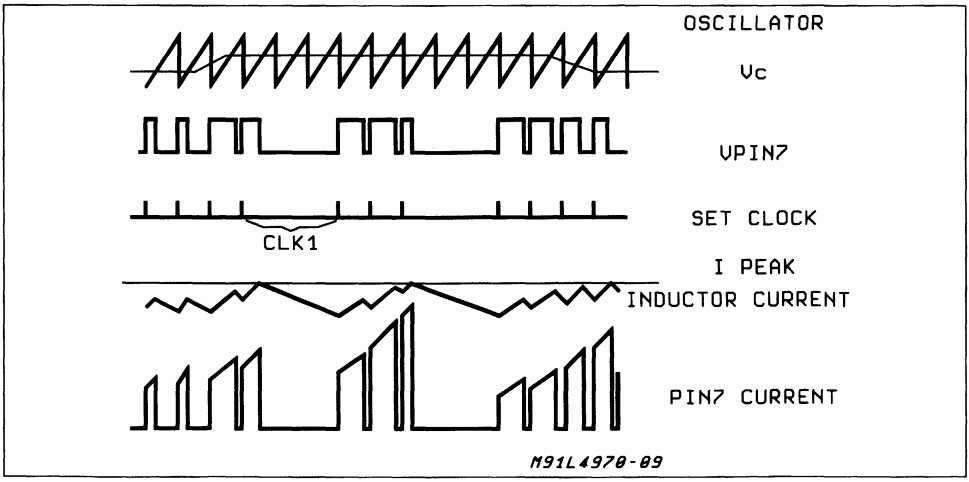


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

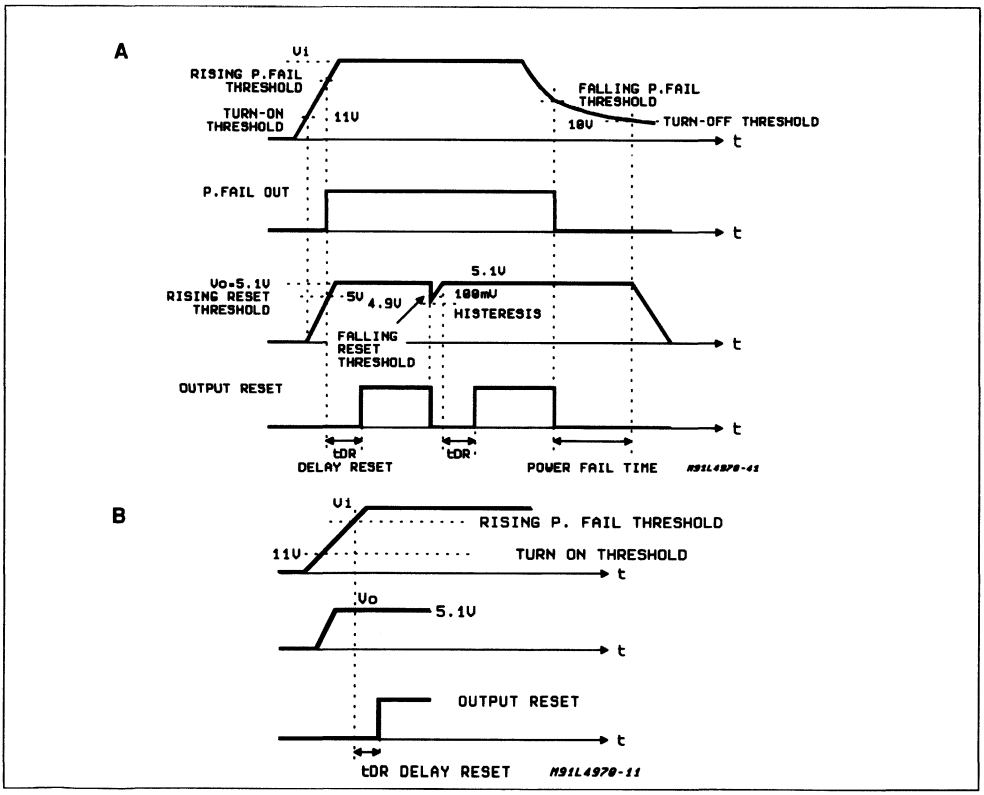
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	$V_o = V_{ref}$ to 40V I_o = 10A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 5A; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 5A; $V_o = V_{ref}$		12	30	mV	5
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 3A to 6A I_o = 2A to 10A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 5A I_o = 10A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V	11	13	15	A	5
η	Efficiency	I_o = 5A $V_o = V_{ref}$ V_o = 12V	80	85 92		% %	5
		I_o = 10A $V_o = V_{ref}$ V_o = 12V	75	80 87		% %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 5A f = 100Hz; $V_o = V_{ref}$	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; R_4 = 10KΩ I_o = 10A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B	1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C; V_i = 15V		2.5		V	7A
		S2 = B; V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA		270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA	2.4	2.7		mA	7A

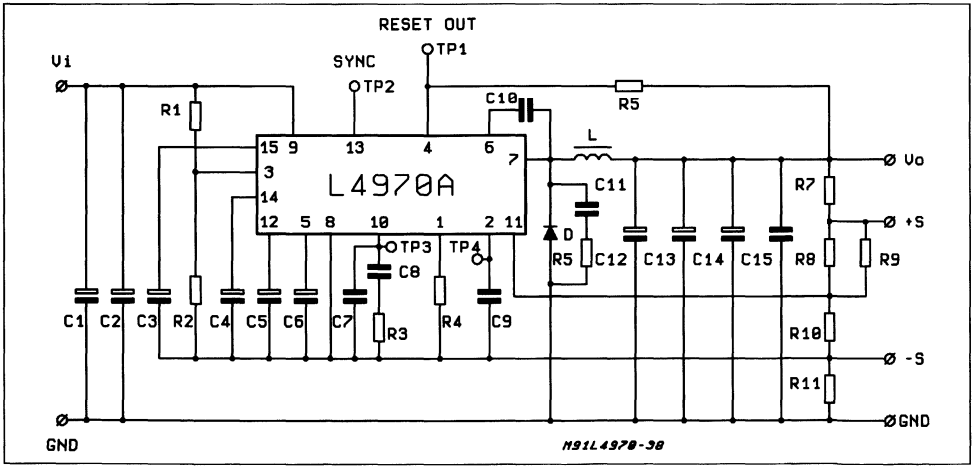
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_{13} = V_2 = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
tw	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

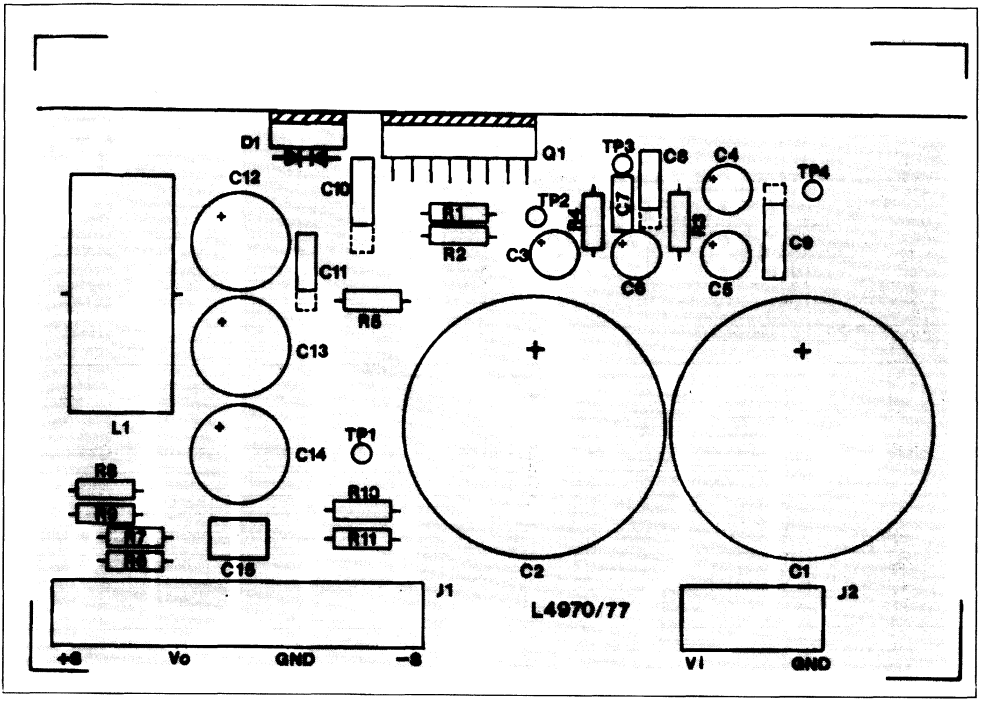
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{14} = V_{11} V_3 = 5.3V	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{14} = V_{11} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 10A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

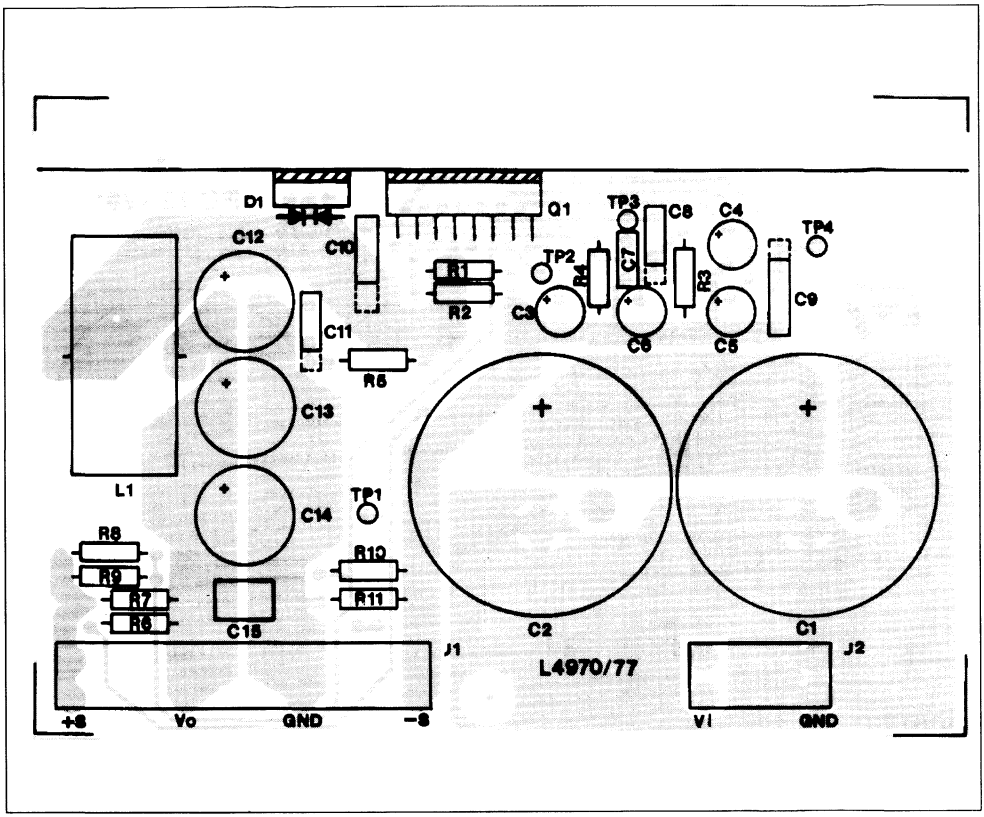


Figure 7: DC Test Circuits

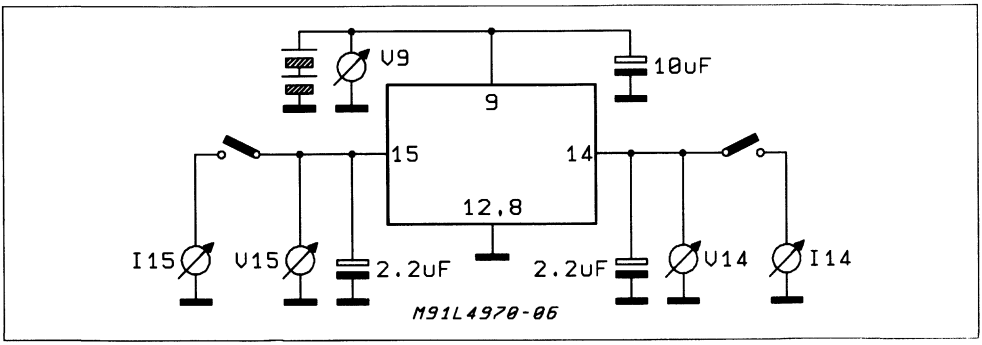


Figure 7A

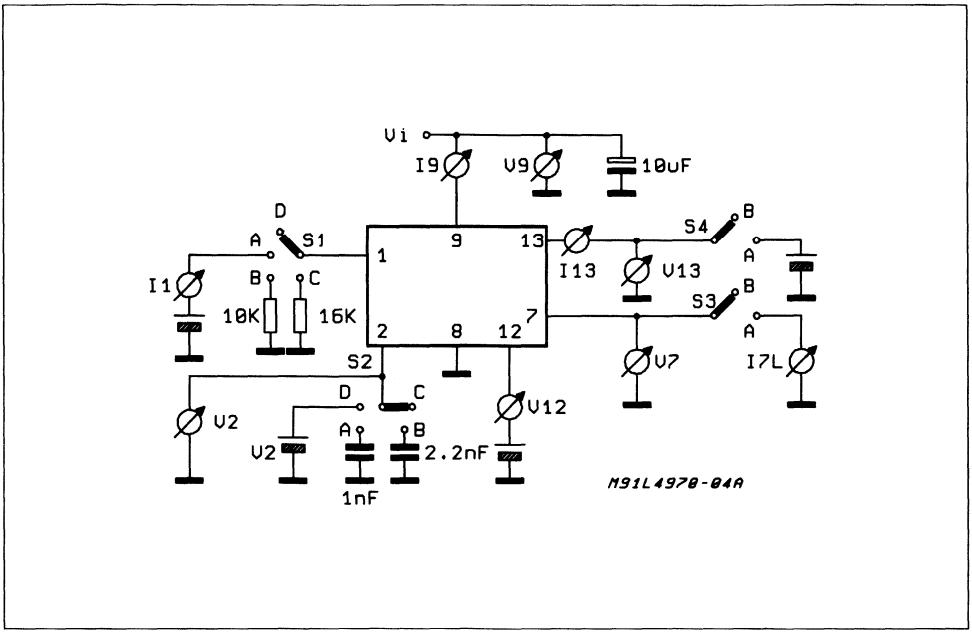


Figure 7B

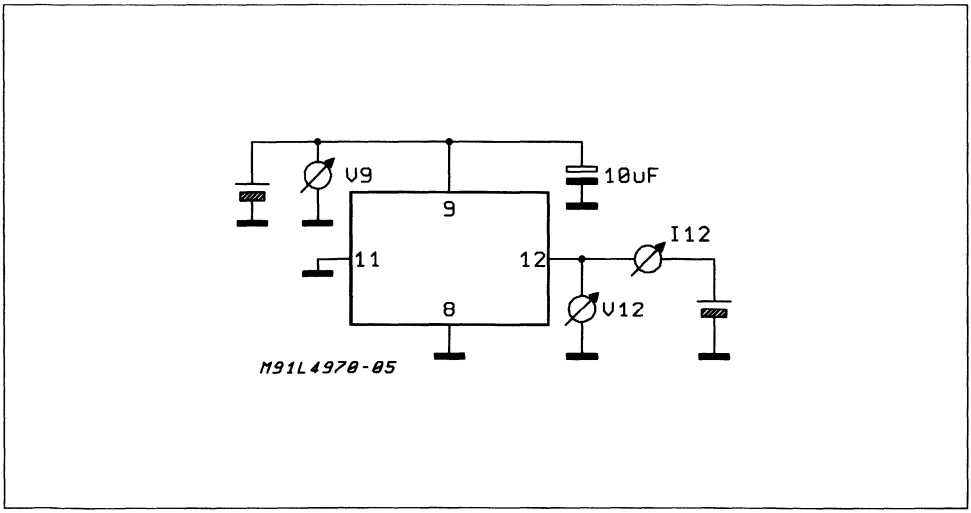


Figure 7D

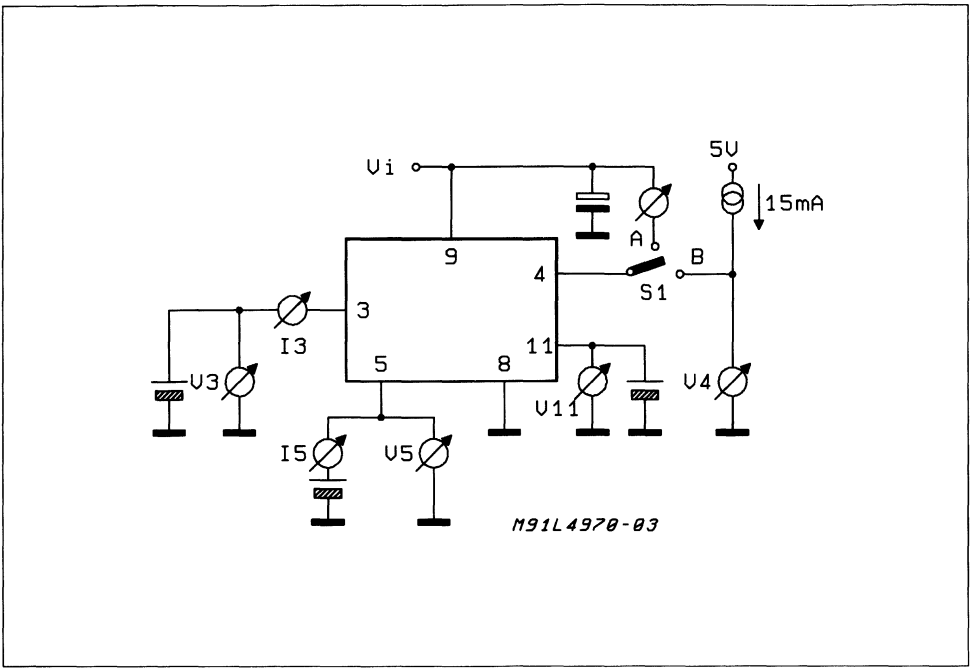


Figure 7C

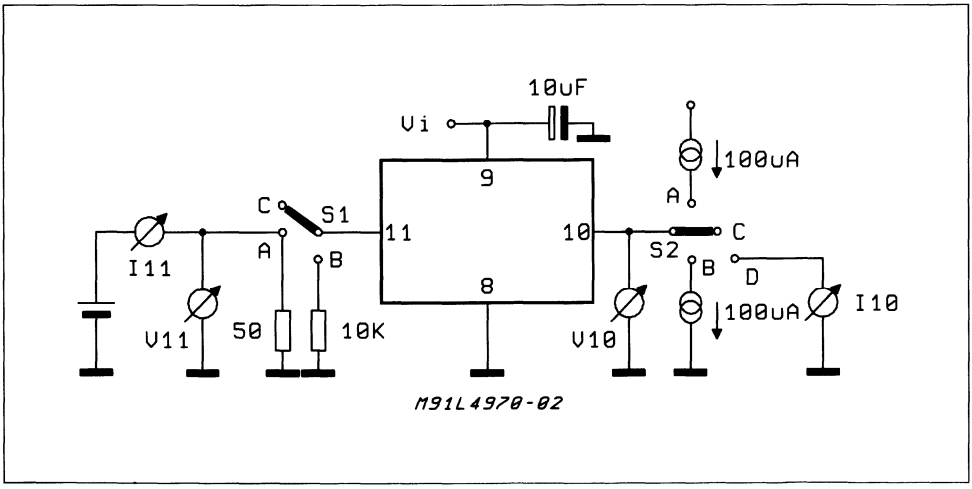


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

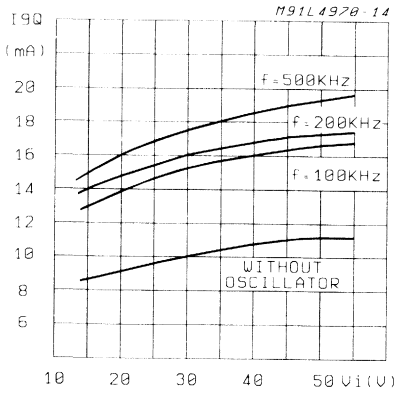


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

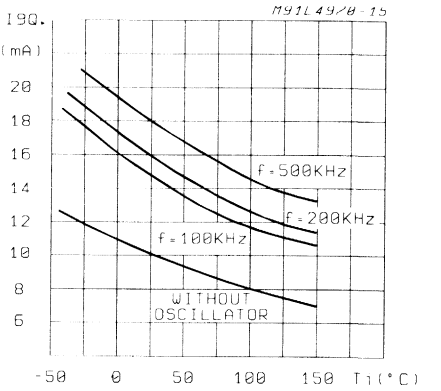


Figure 10: Quiescent Drain Current vs. Duty Cycle

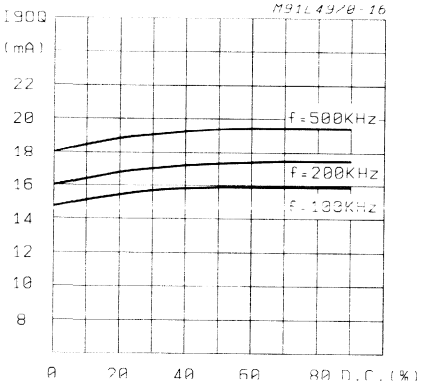


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

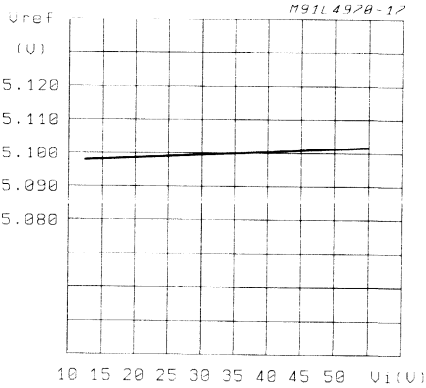


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

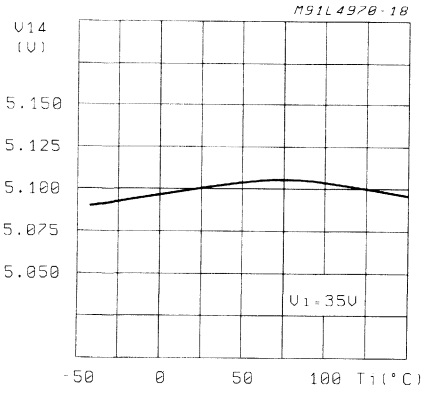


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

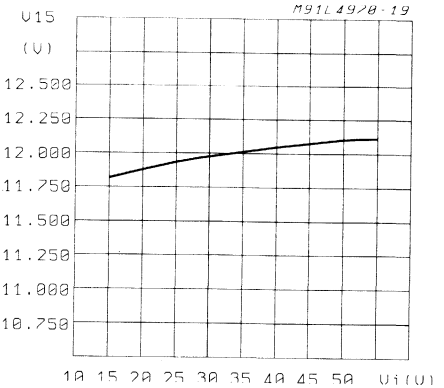


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

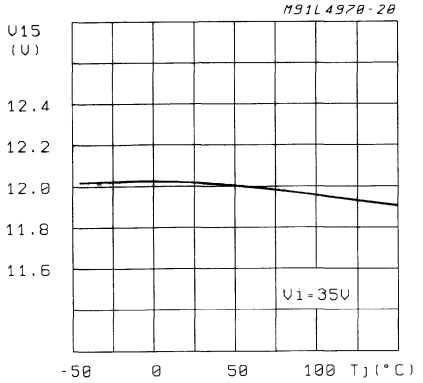


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

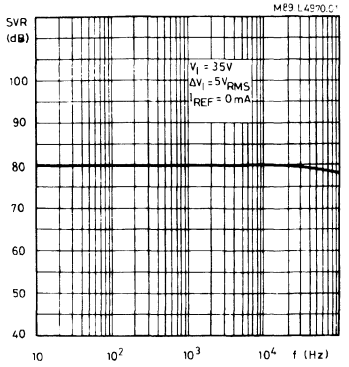


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

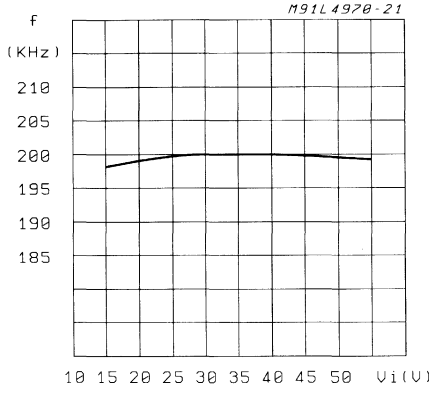


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

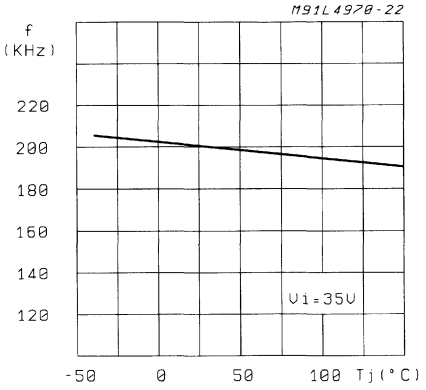


Figure 18: Switching Frequency vs. R4 (see fig. 5)

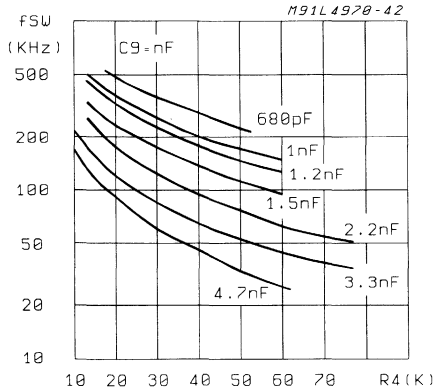


Figure 19: Max. Duty Cycle vs. Frequency

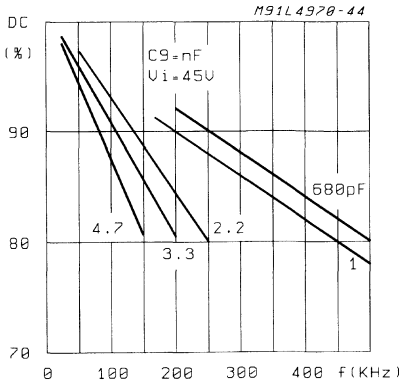


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

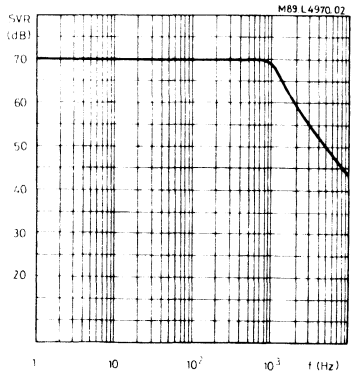


Figure 21: Line Transient Response (see fig. 5)

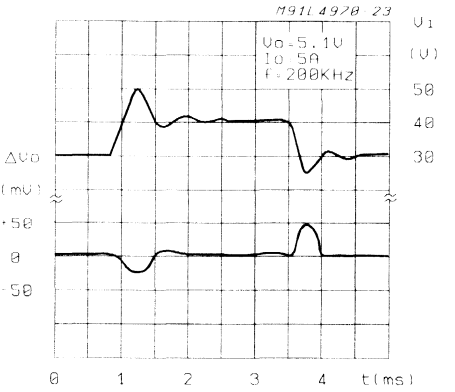


Figure 22: Load Transient Response (see fig. 5)

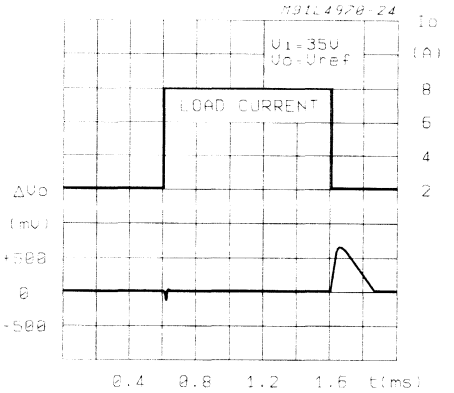


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

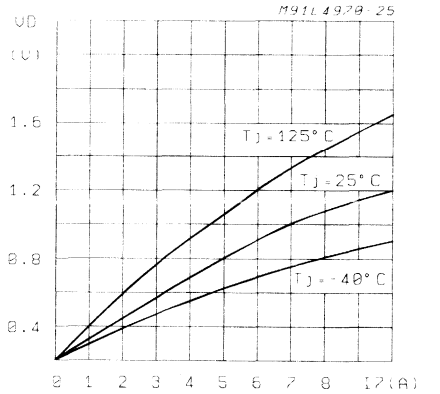


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

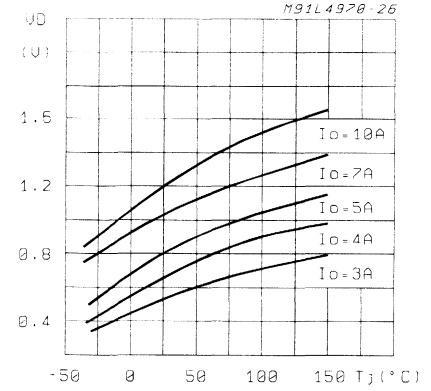


Figure 25: Power Dissipation (device only) vs. Input Voltage

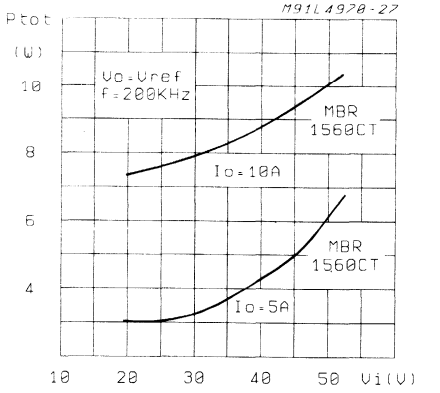


Figure 26: Power Dissipation (device only) vs. Output Voltage

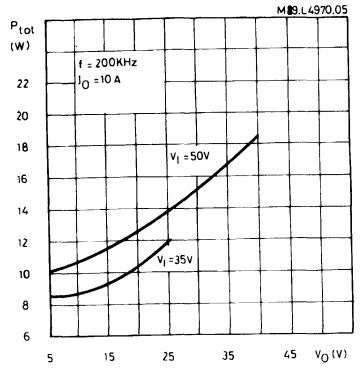


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th} \text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

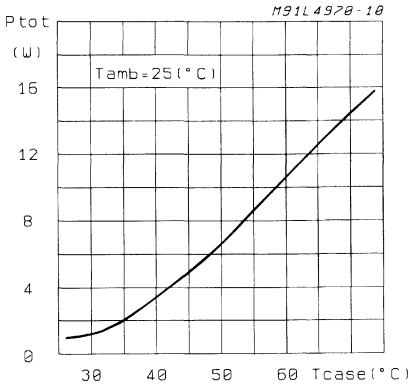


Figure 28: Efficiency vs. Output Current

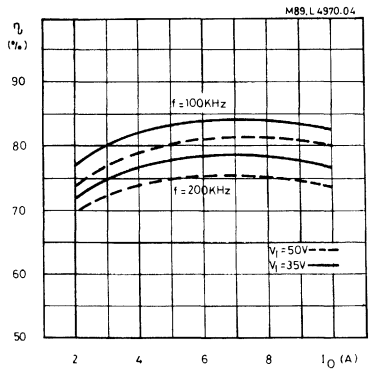


Figure 29: Efficiency vs. Output Voltage

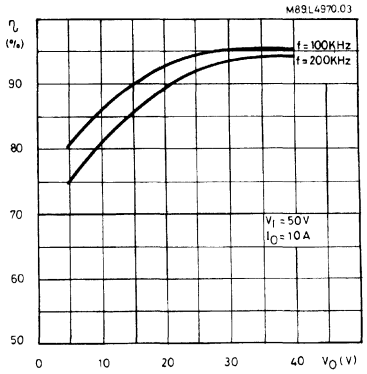


Figure 30: Efficiency vs. Output Voltage

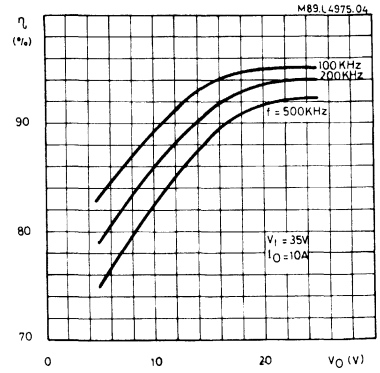


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

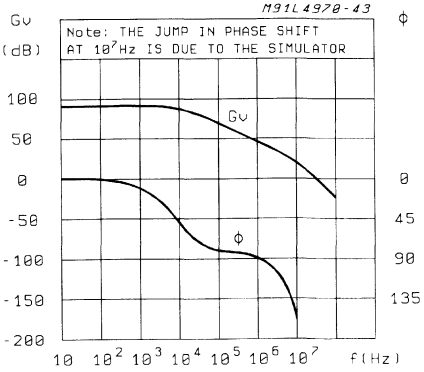


Figure 32: Power Dissipation Derating Curve

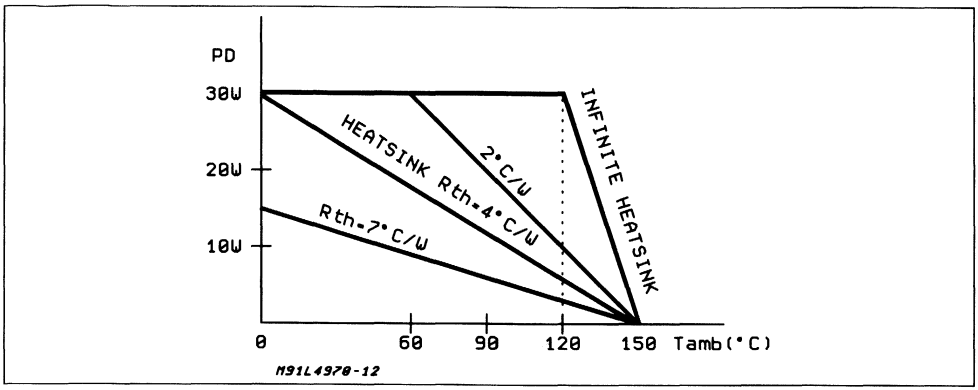


Figure 33: A5.1V/12V Multiple Supply. Note the Synchronization between the L4970A and the L4974A

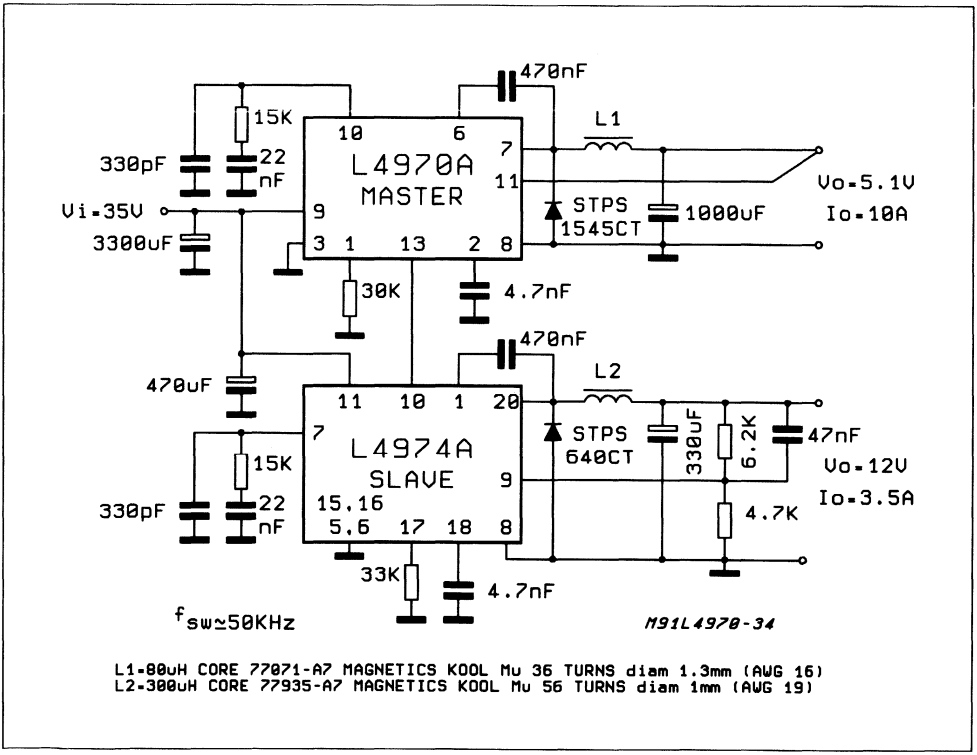


Figure 34: 5.1V / 10A Low Cost Application

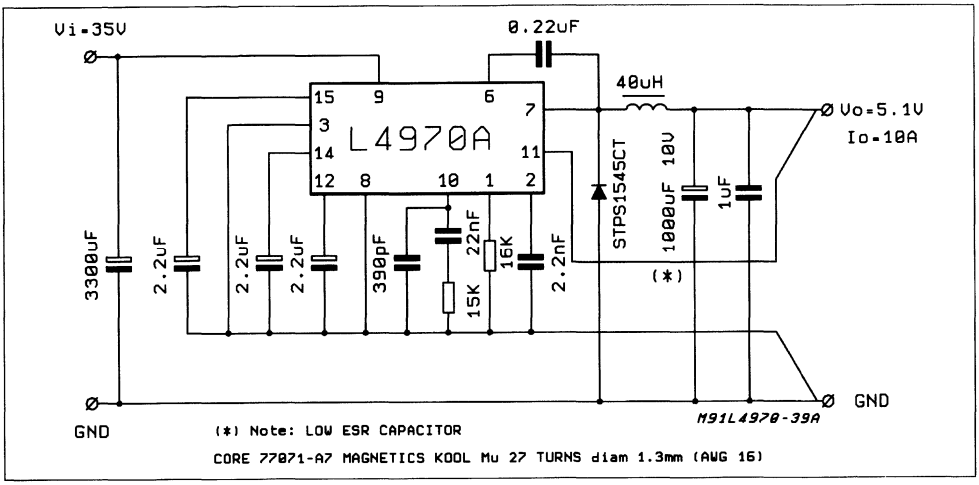


Figure 35: 10A Switching Regulator, Adjustable from 0V to 25V.

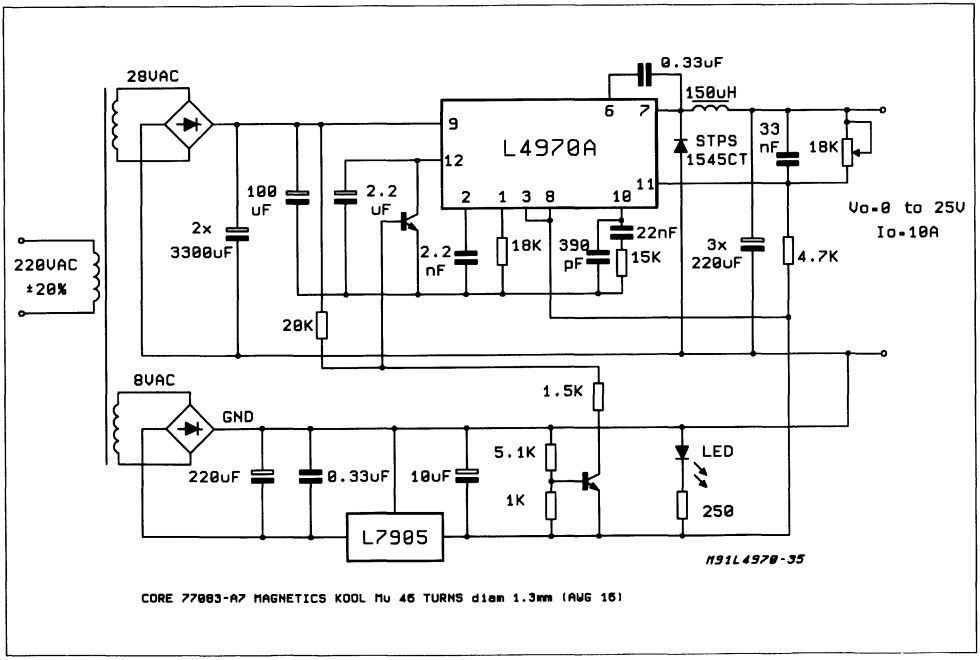
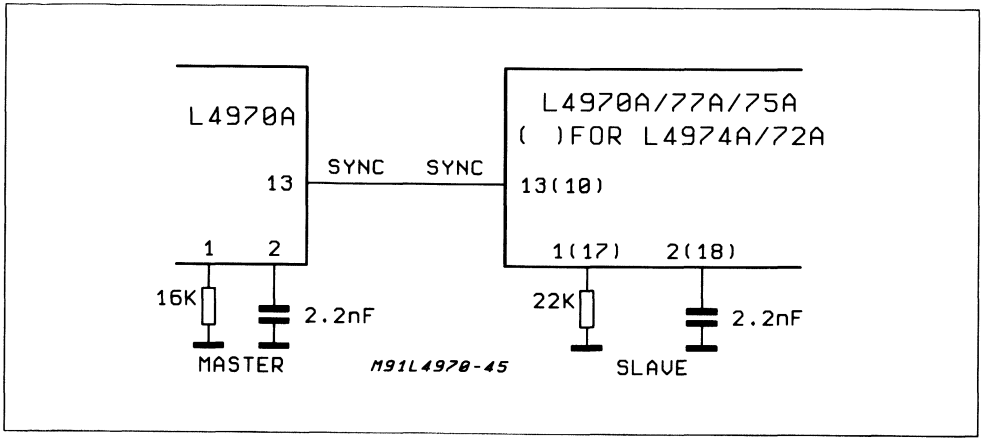


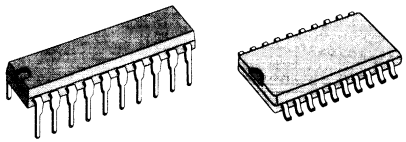
Figure 36: L4970A's Sync. Example



2A SWITCHING REGULATOR

- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

SO20

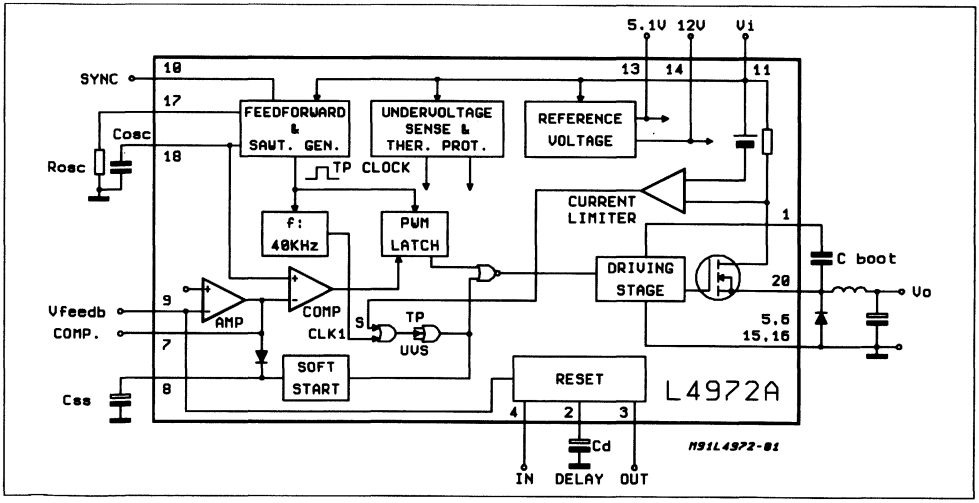
ORDERING NUMBERS : L4972A (Powerdip)
L4972AD (SO20)

DESCRIPTION

The L4972A is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

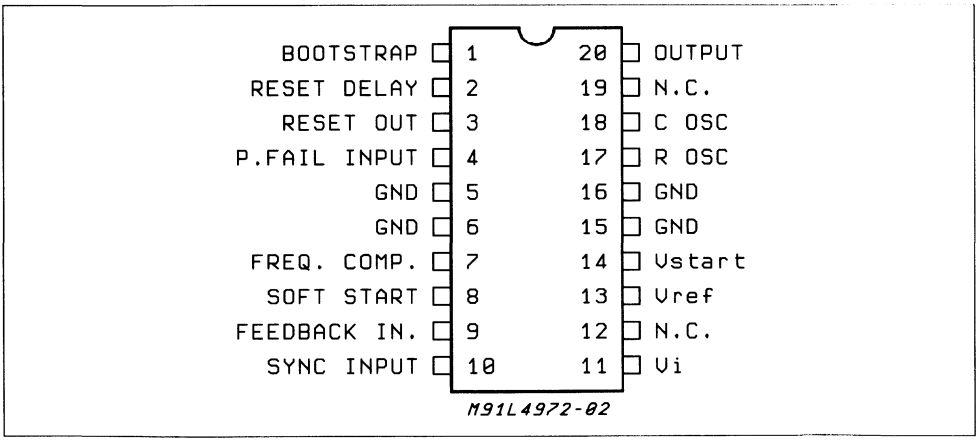


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at $T_{PINS} \leq 90°C$ at T_{amb} = 70°C (No copper area on PCB)	5 / 3.75(*) 1.3/1 (*)	W W
T_J, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

(*) SO-20

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Powerdip	SO-20
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12°C/W	16°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60°C/W	80°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4972A's are synchronized by connecting pin 10 inputs togheter or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	V_{ref}	5.1 V_{ref} Device Reference Voltage
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output

CIRCUIT OPERATION

The L4972A is a 2A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 2A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

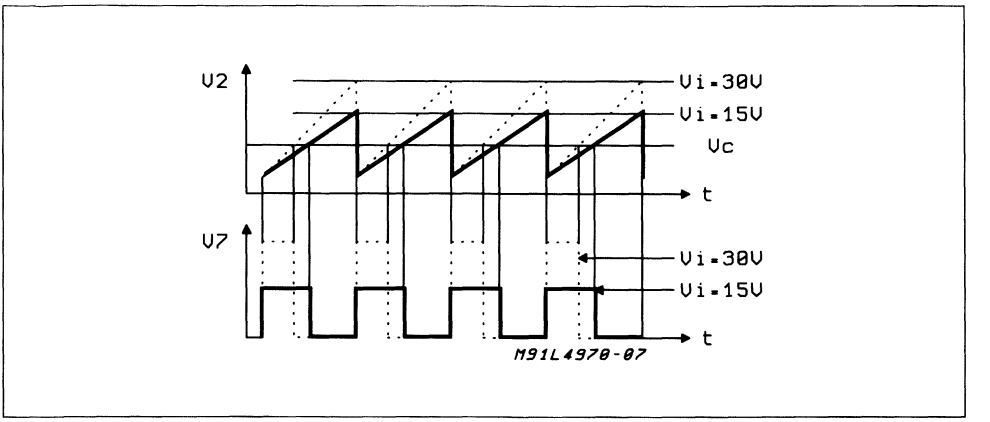


Figure 2 : Soft Start Function.

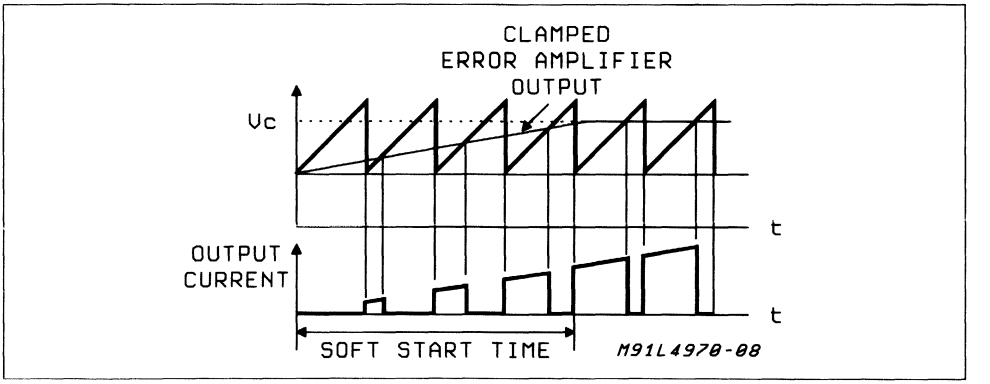


Figure 3 : Limiting Current Function.

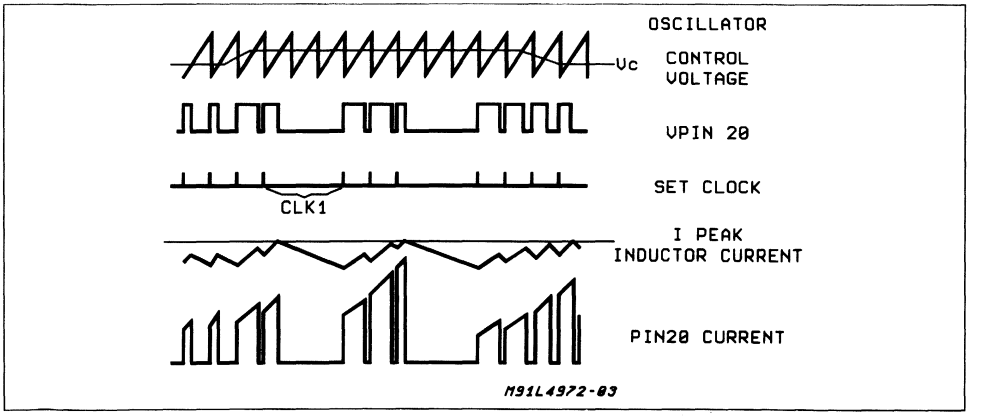
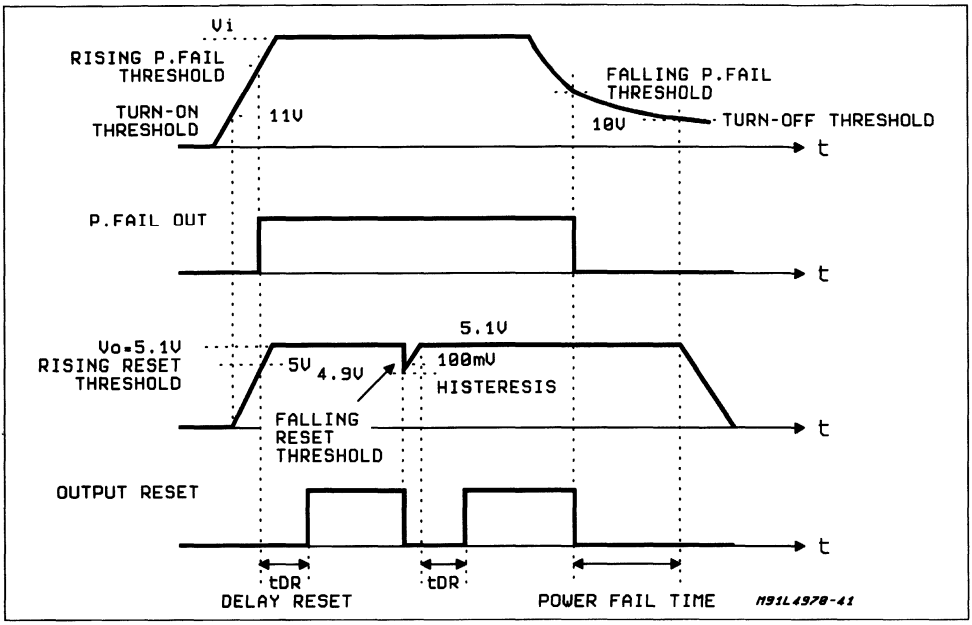
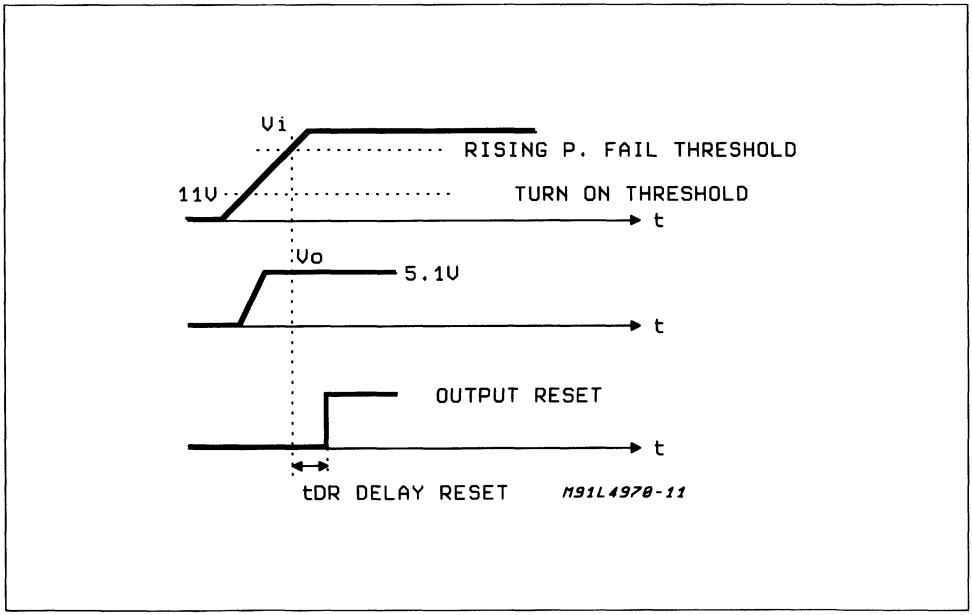


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 2A (**)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 1A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 0.5A; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5A to 2A		7	20	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A		0.25	0.4	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	2.5	2.8	3.5	A	
η	Efficiency (*)	I_o = 2A, f = 100KHz V_o = V_{ref} V_o = 12V	75	85 90		% %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 1A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta Vi$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref} R_4 = 15KΩ I_o = 2A C_9 = 2.2nF	200			KHz	5

(*) Only for DIP version (**) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\ short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\,Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	70	100	130	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200µA$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B		1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100µA$			270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$		2.4	2.7		mA	7A

SYNC FUNCTION (pin 10)

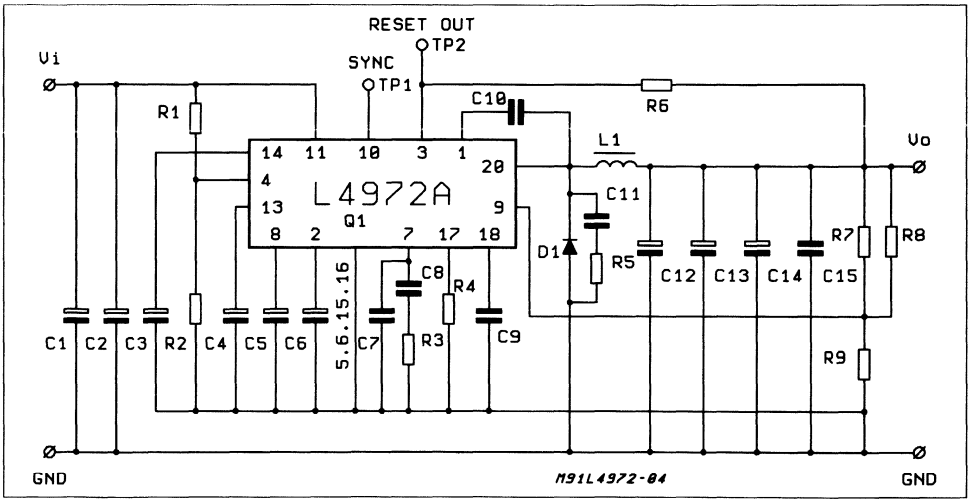
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	V8 = 0; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
I_{10L}	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
I_{10H}	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
tw	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -120	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	40	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3 = 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.95	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 2A ; f_{sw} = 100KHz)

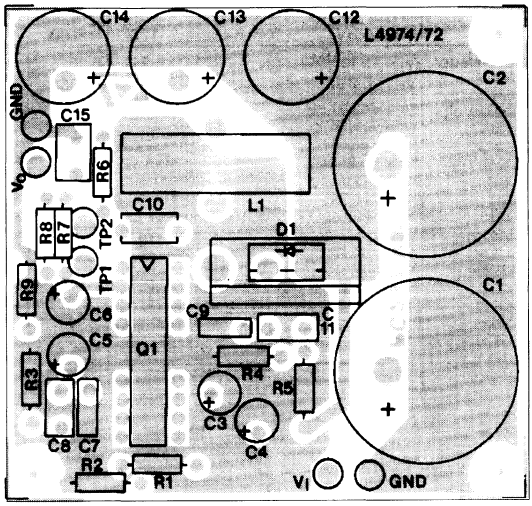
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 7mV (I_o = 0.5 to 2A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available (only for DIP version)



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A.

V_0	R_9	R_7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

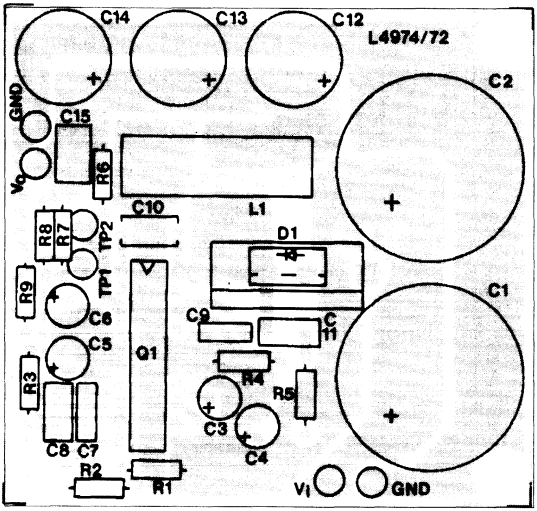


Figure 7 : DC Test Circuits.

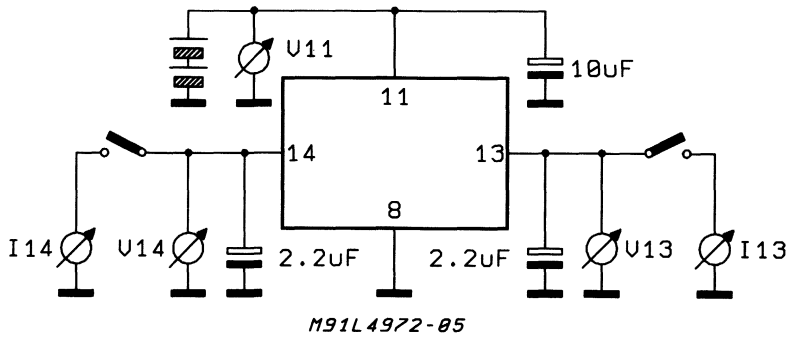


Figure 7A.

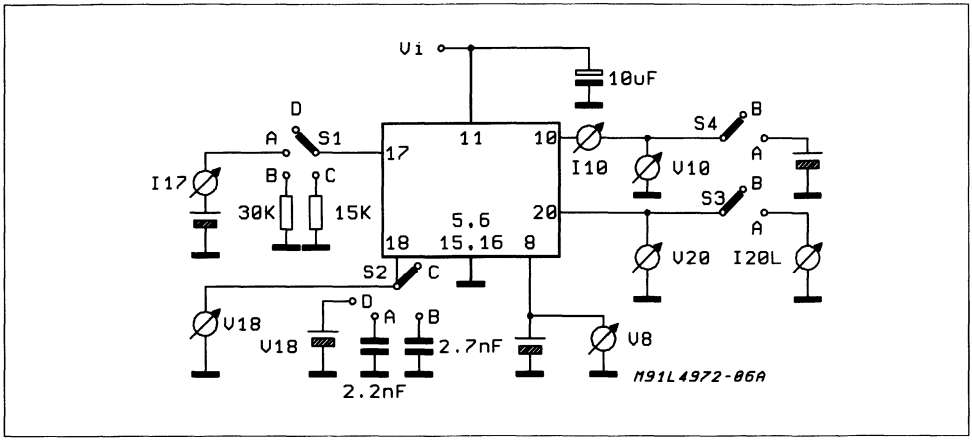


Figure 7B.

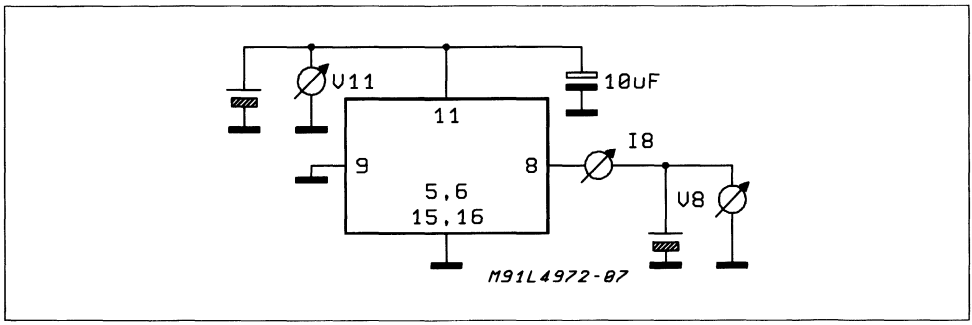


Figure 7C.

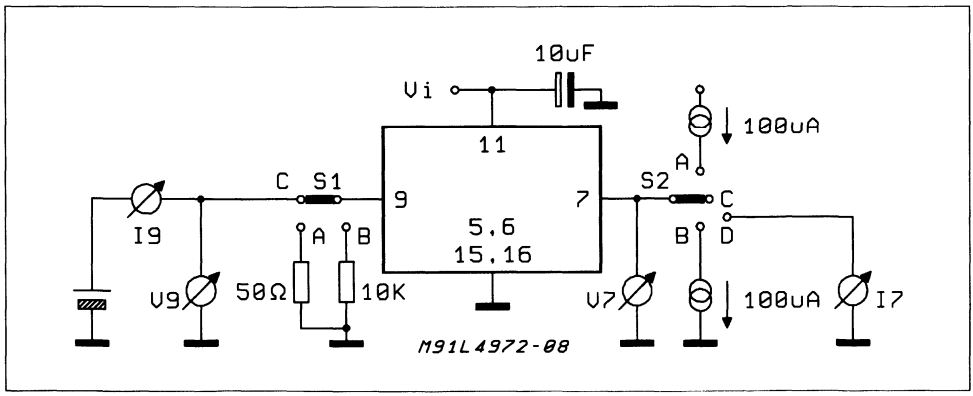


Figure 7D.

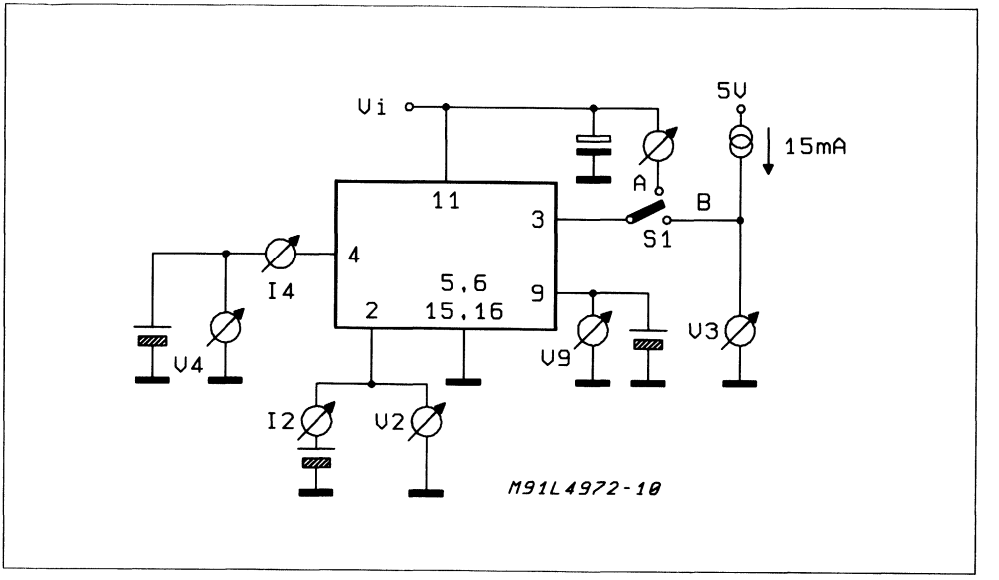


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

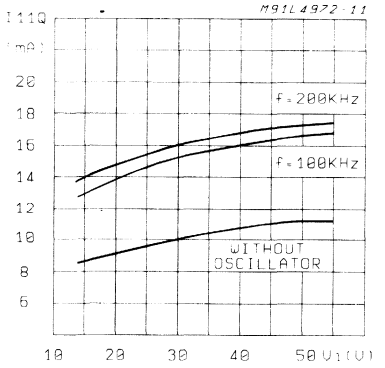


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

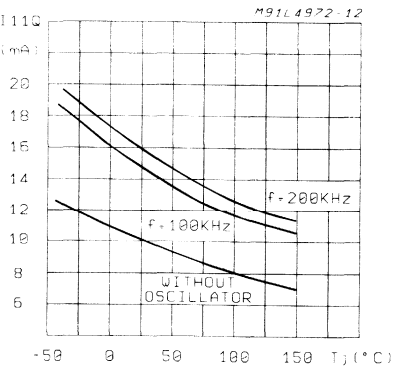


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

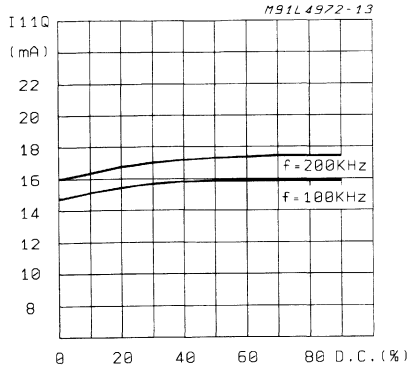


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

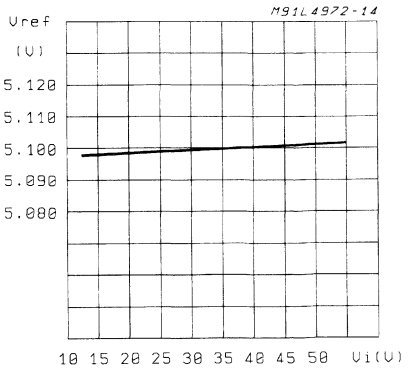


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

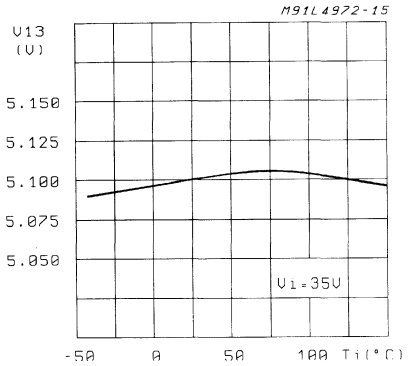


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

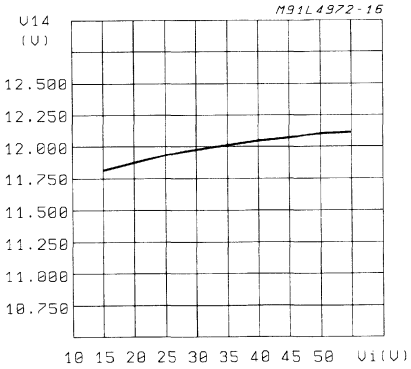


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

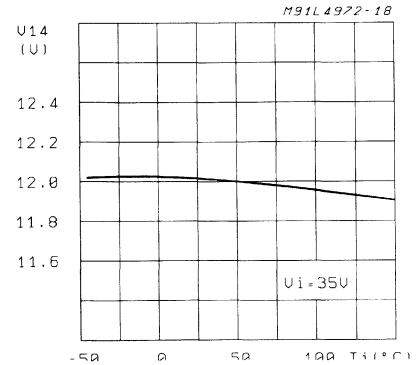
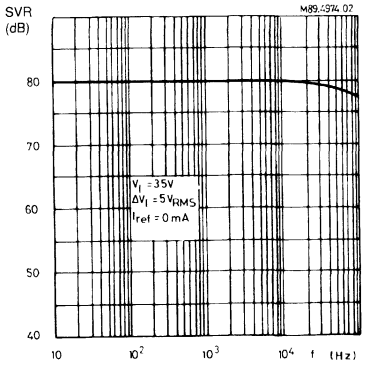


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-



Fi . e 16 : Switching Frequency vs. Input Voltage (see fig. 5).

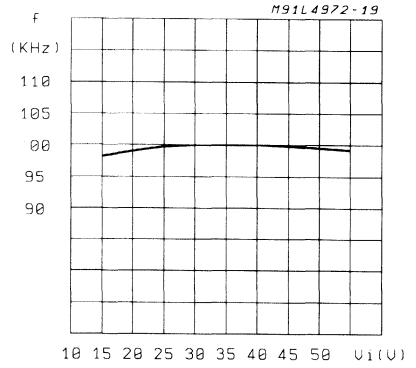


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

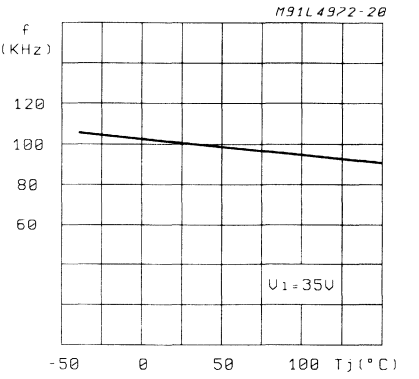


Figure 18 : Switching Frequency vs. R4 (see fig.5).

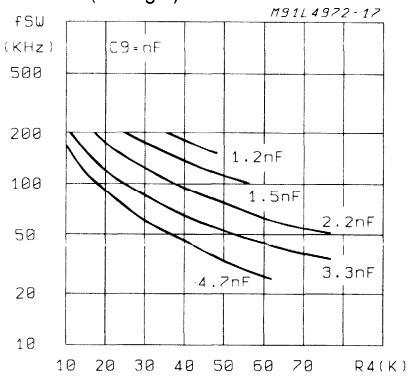


Figure 19 : Maximum Duty Cycle vs. Frequency.

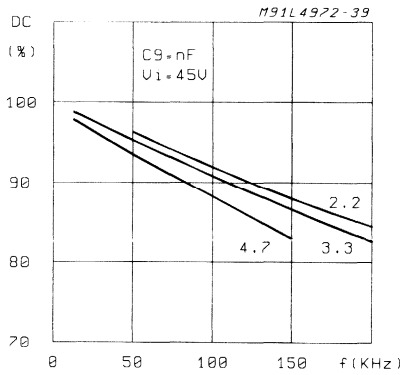


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

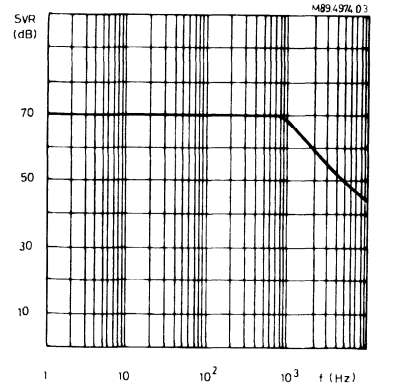


Figure 21 : Efficiency vs. Output Voltage.

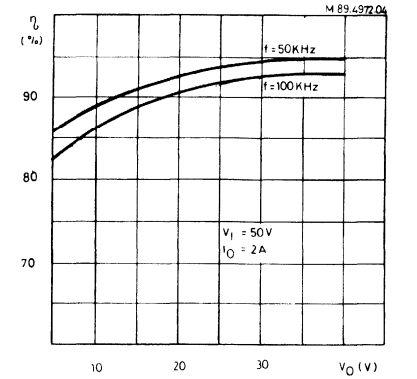


Figure 22 : Line Transient Response (see fig. 5).

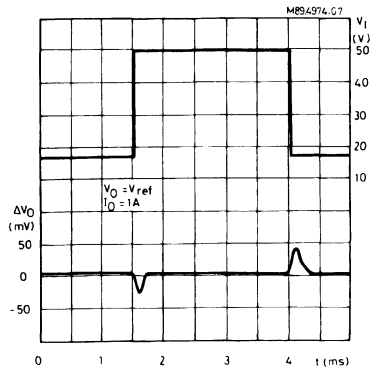


Figure 23 : Load Transient Response (see fig. 5).

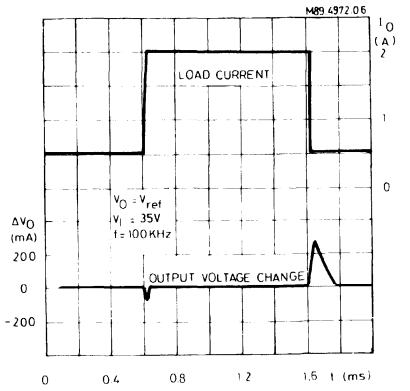


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

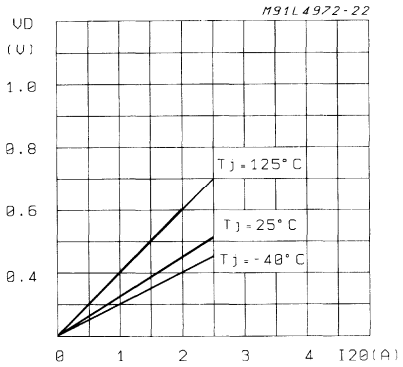


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

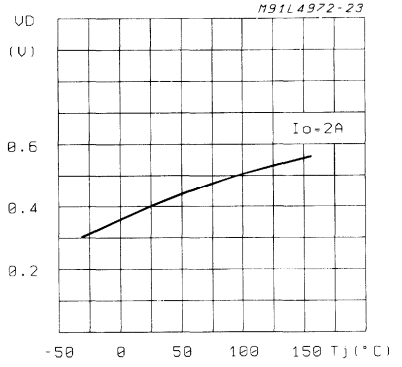


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

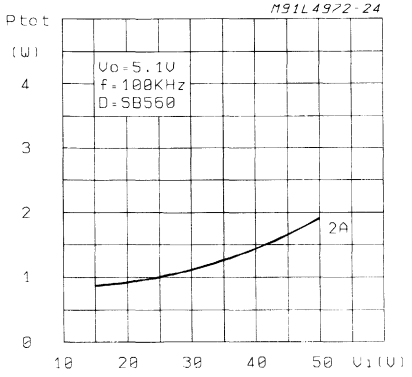


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

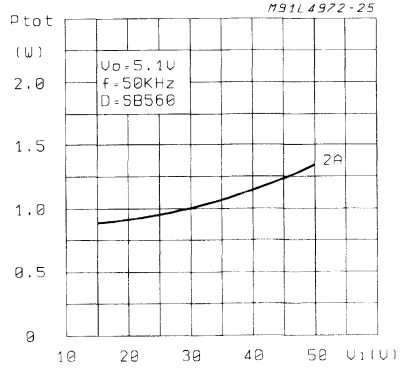


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

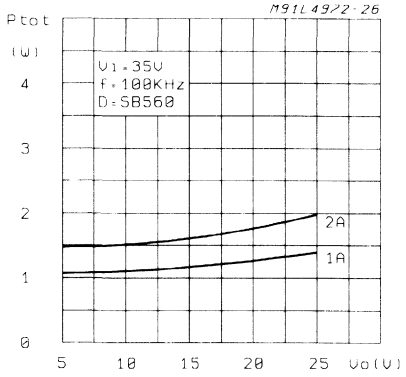


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

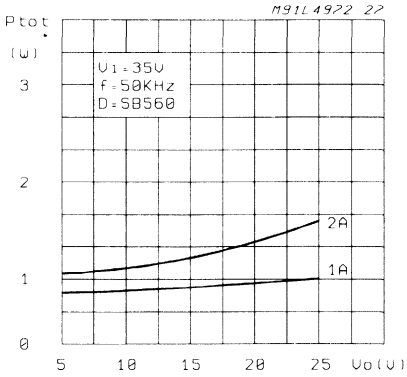


Figure 30 : Power Dissipation (device only) vs. Output Current.

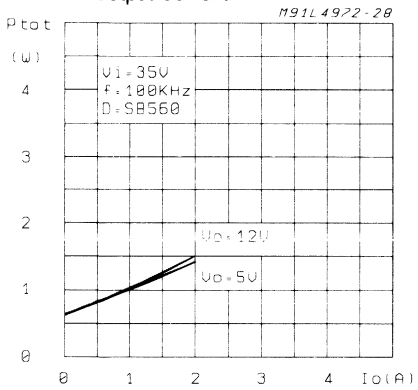


Figure 31 : Power Dissipation (device only) vs. Output Current.

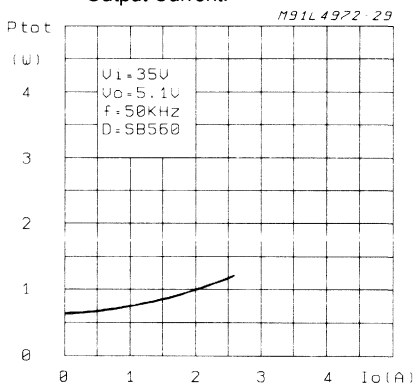


Figure 32 : Efficiency vs. Output Current.

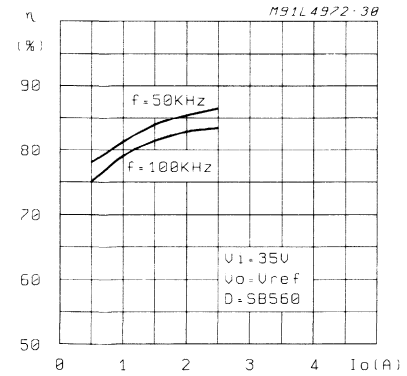


Figure 33 : Test PCB Thermal Characteristic.

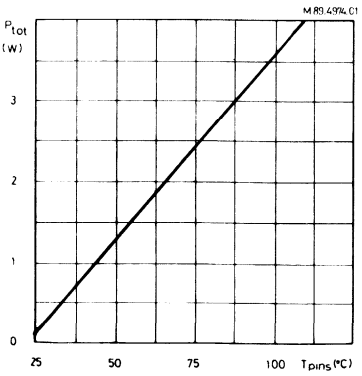


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

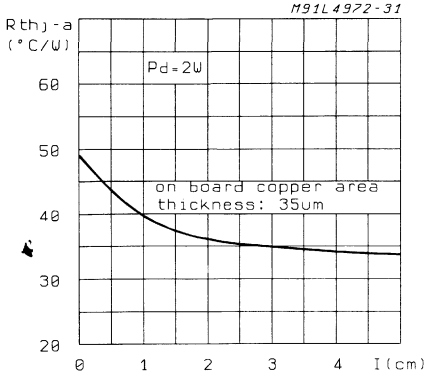


Figure 35: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

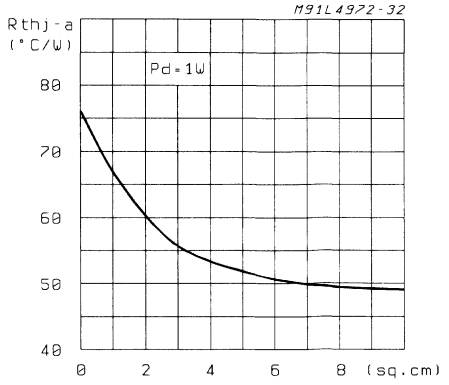


Figure 36: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

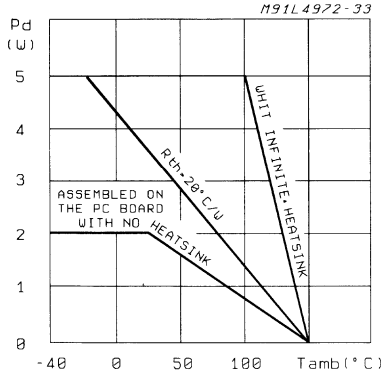


Figure 37: Maximum Allowable Power Dissipation vs. Ambient Temperature (SO20)

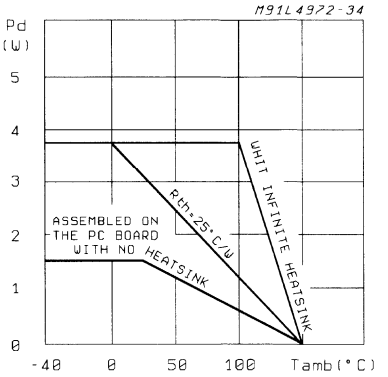


Figure 38: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

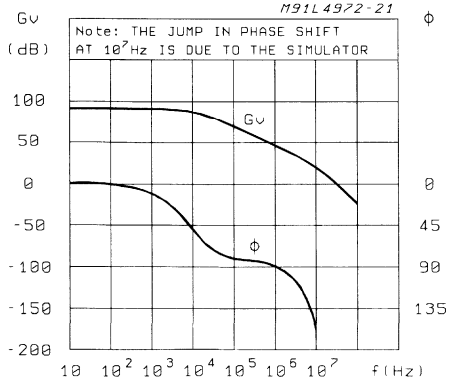


Figure 39 : 2A – 5.1V Low Cost Application Circuit.

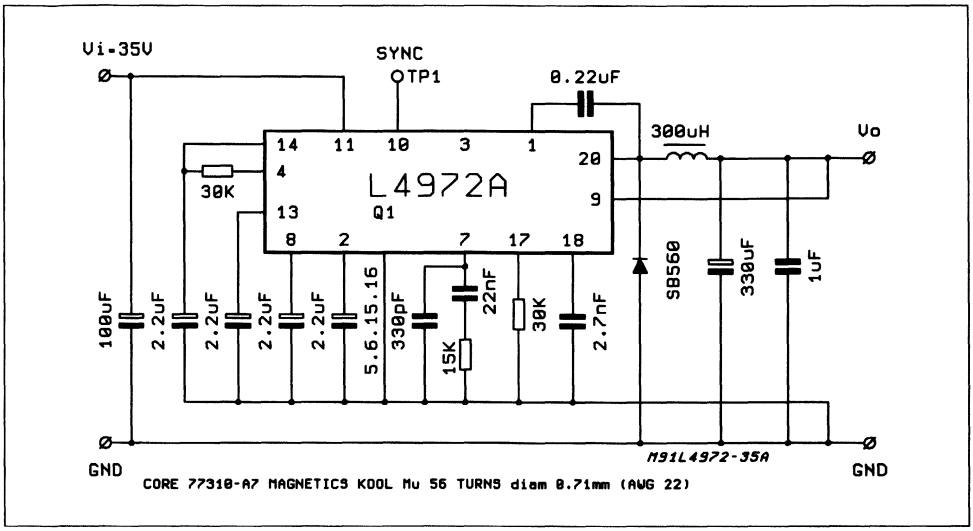


Figure 40 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4972A and L4970A.

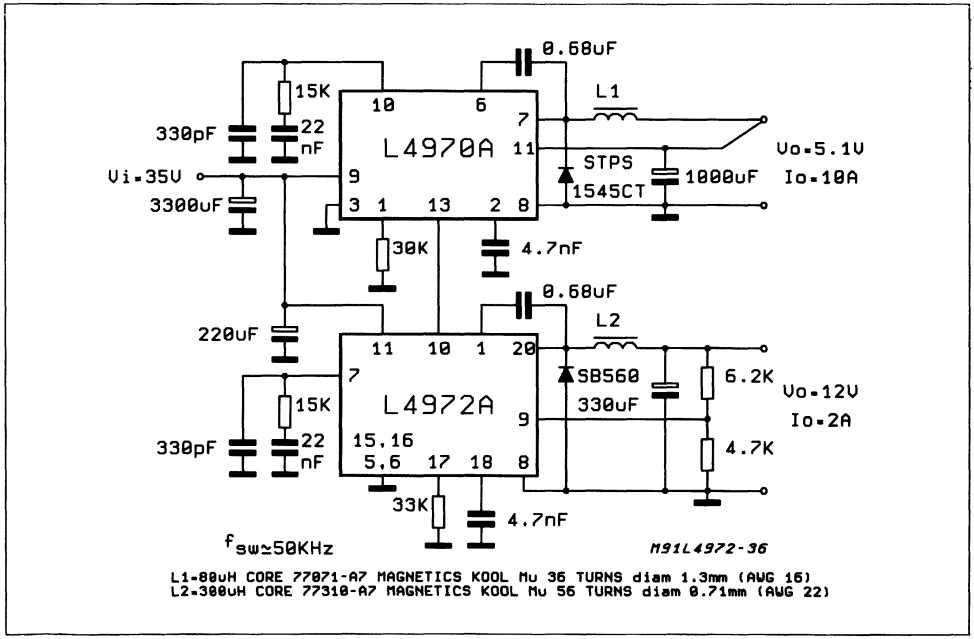


Figure 41 : L4972A's Sync. Example.

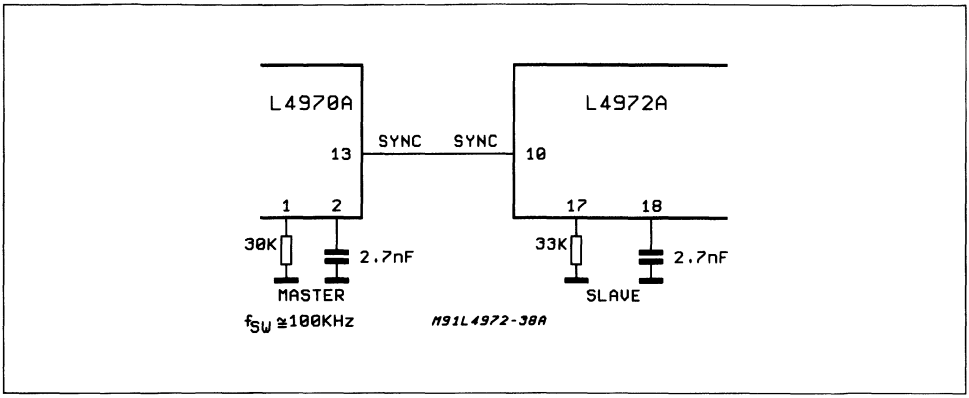
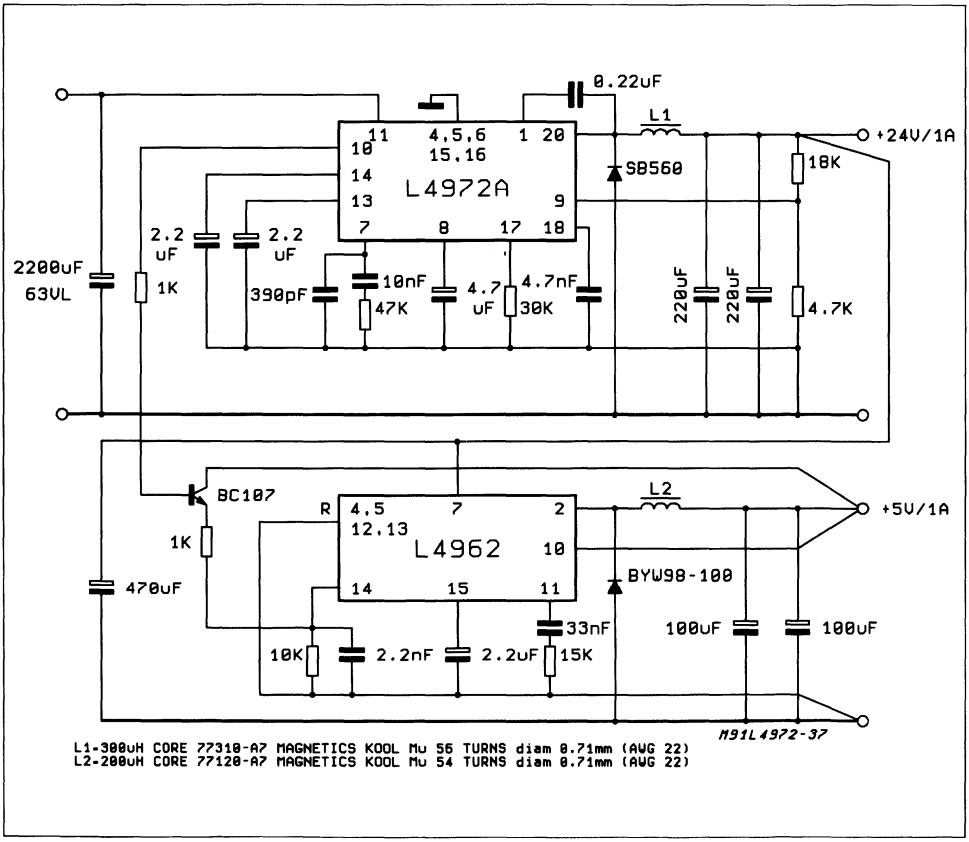


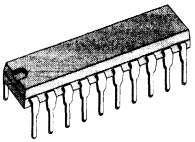
Figure 42: 1A/24V Multiple Supply. Note the synchronization between the L4972A and L4962



3.5A SWITCHING REGULATOR

- 3.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

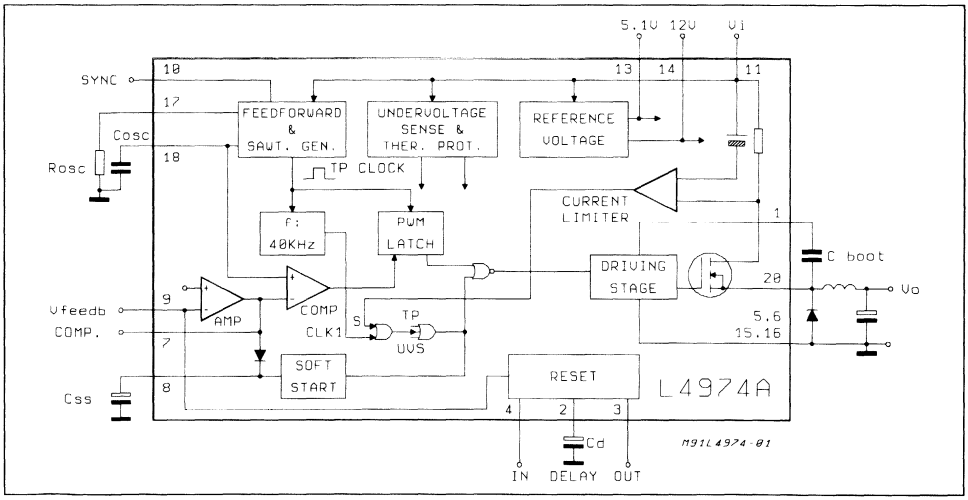
ORDERING NUMBER : L4974A

DESCRIPTION

The L4974A is a stepdown monolithic power switching regulator delivering 3.5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4974A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 plastic package and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

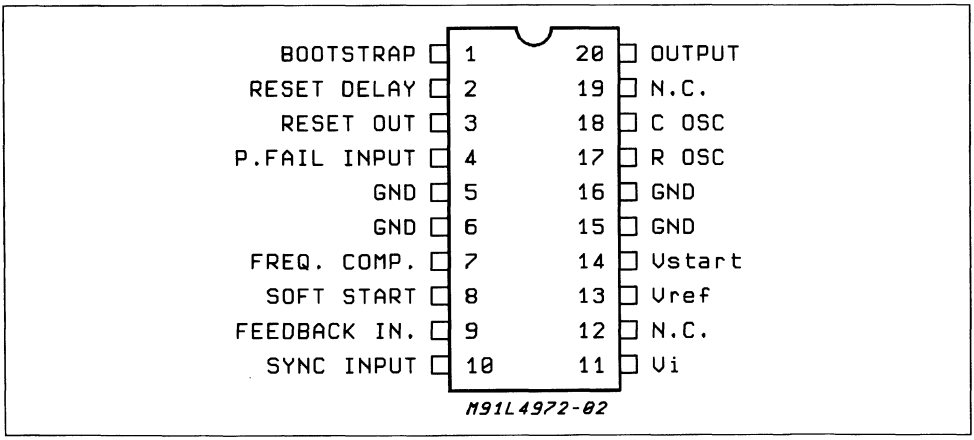
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at $T_{PINS} \leq 90°C$ at T_{amb} = 70°C (No copper area on PCB)	5 1.3	W W
T_J, T_{stg}	Junction and Storage.Temperature	-40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60	°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4974A's are synchronized by connecting pin 10 inputs togheter or via an external syncr. pulse..
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	V_{ref}	5.1 V_{ref} Device Reference Voltage
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output

CIRCUIT OPERATION

The L4974A is a 3.5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 3.5A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

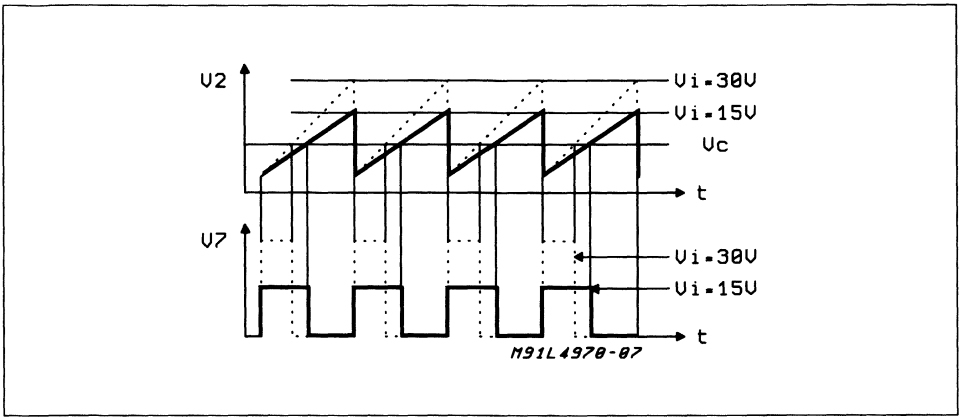


Figure 2 : Soft Start Function.

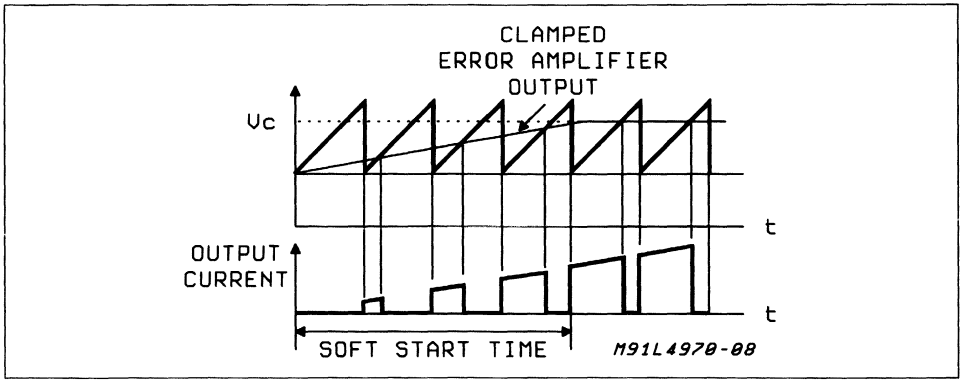


Figure 3 : Limiting Current Function.

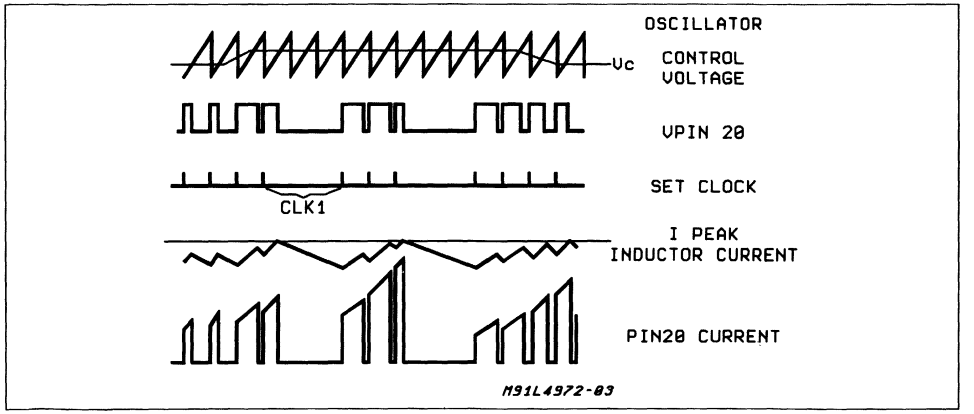
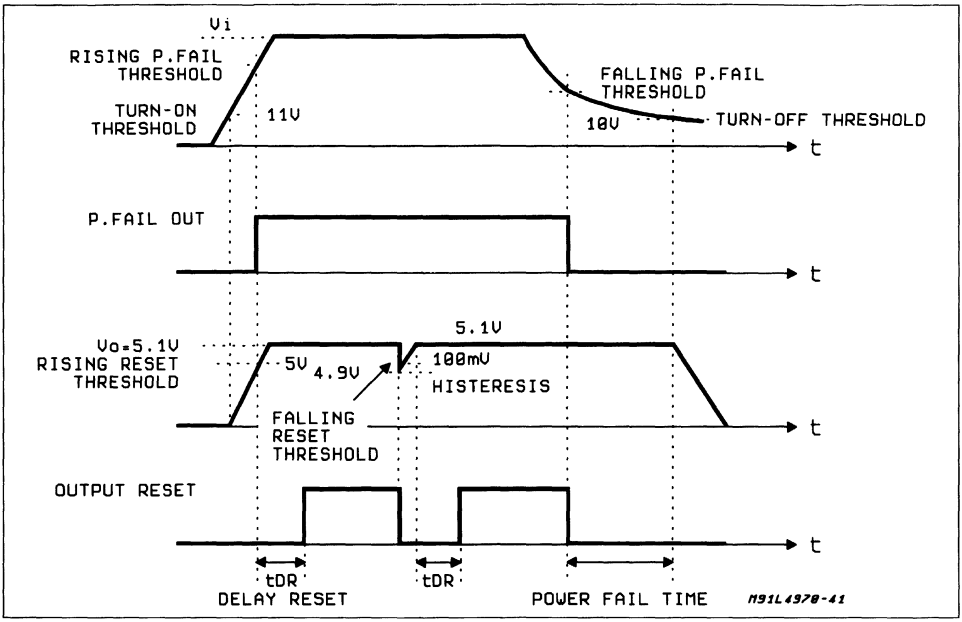
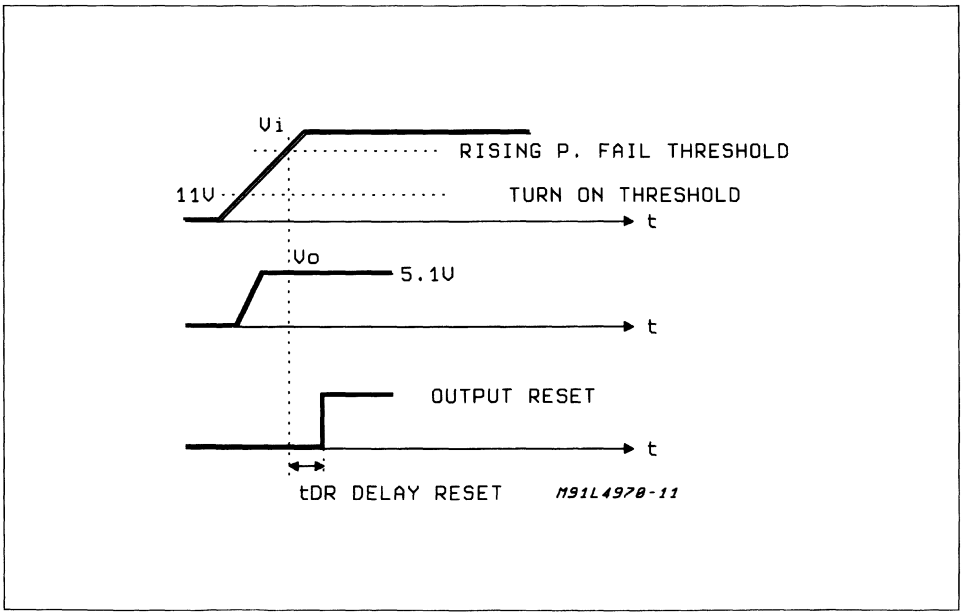


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 3.5A (*)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 2A; V_o = V_{ret}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_I = 15V to 50V I_o = 1A; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_O = V_{ref} I_o = 1A to 3.5A		8	25	mV	
		I_o = 2A to 3A		4	10	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A I_o = 3.5A		0.25 0.45	0.4 0.7	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	4	4.75	5.5	A	
η	Efficiency	I_o = 3.5A, f = 100KHz V_o = V_{ref} V_o = 12V	80	85 90		% %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 5A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta Vi$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125 C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref} R_4 = 15KΩ I_o = 3.5A C_9 = 2.2nF	200			KHz	5

(*) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\ short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\,Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	70	100	130	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200µA$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = -100µA$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100µA$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B		1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100µA$			270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$		2.4	2.7		mA	7A

SYNC FUNCTION (pin 10)

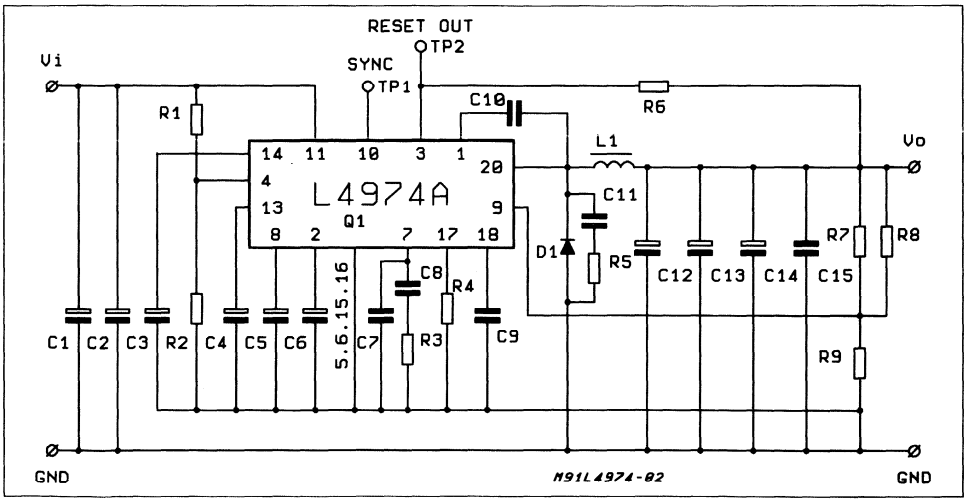
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	$V_8 = 0$; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
$+I_{10L}$	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
$+I_{10H}$	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
tw	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -120	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	40	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3 = 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.955	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 3.5A ; f_{sw} = 100KHz)

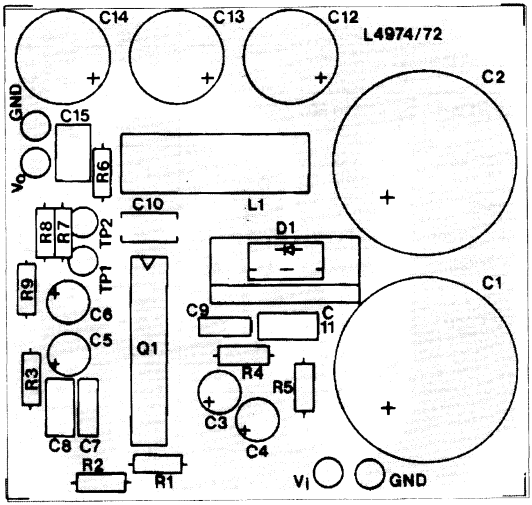
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 8mV (I_o = 1 to 3.5A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A.

V_O	R_9	R_7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

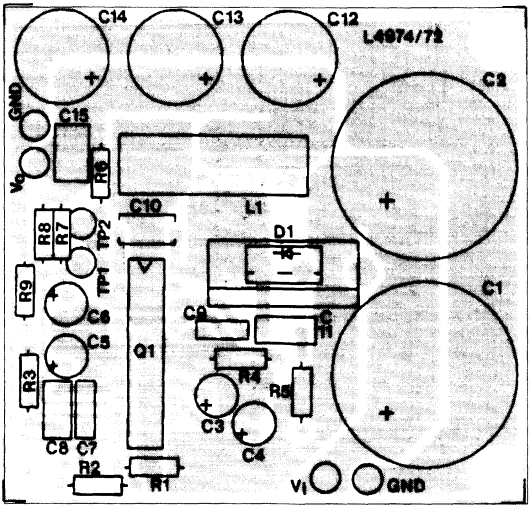


Figure 7 : DC Test Circuits.

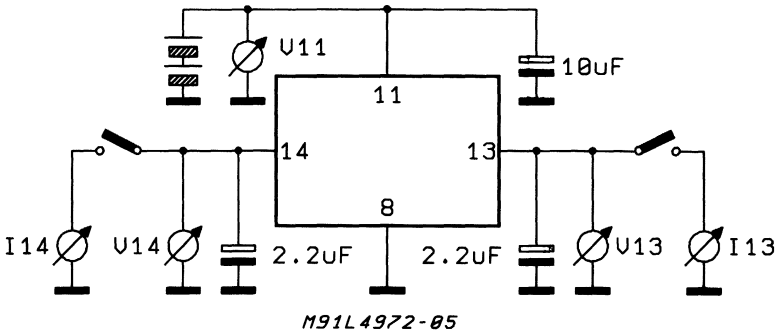


Figure 7A.

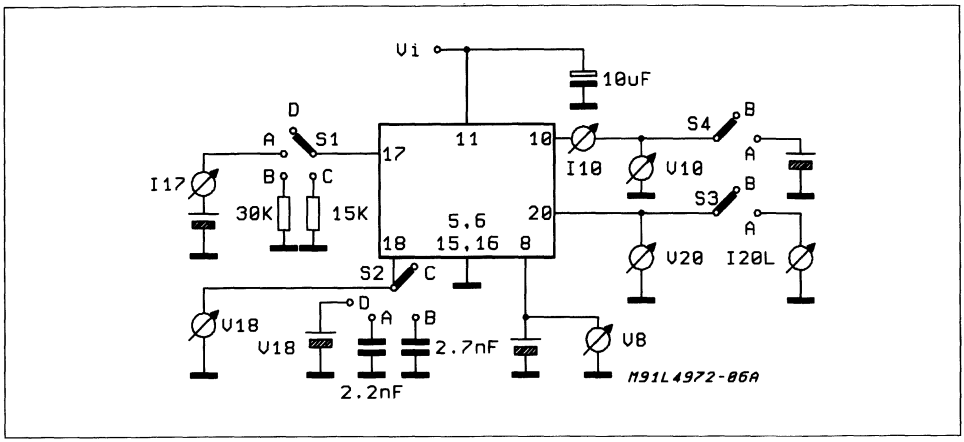


Figure 7B.

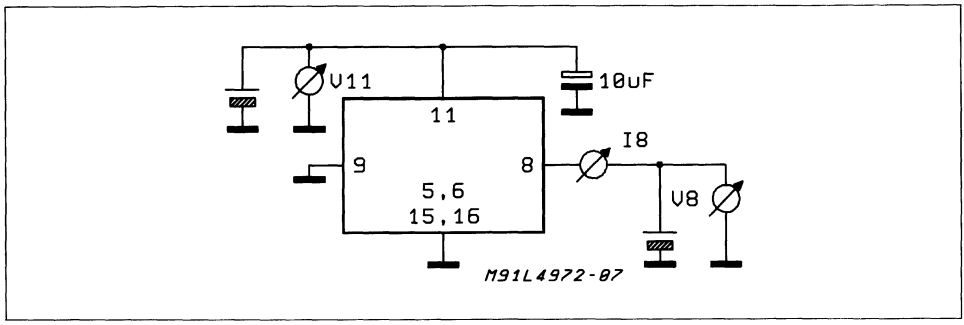


Figure 7C.

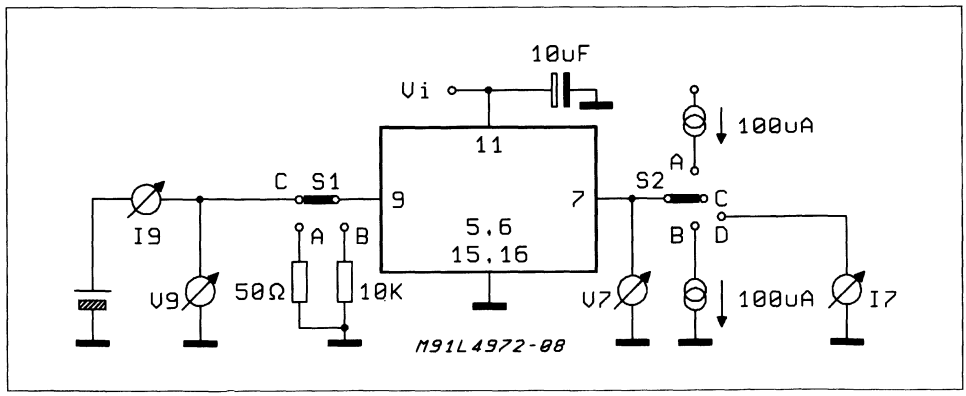


Figure 7D.

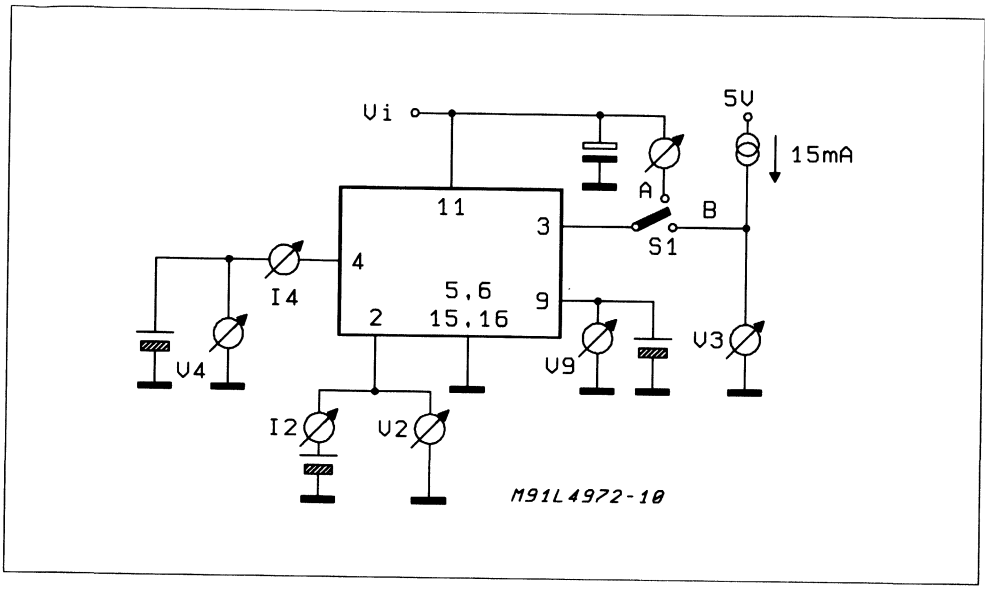


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

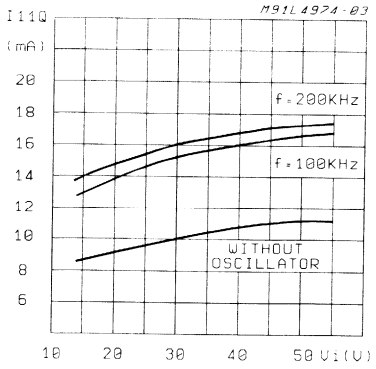


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

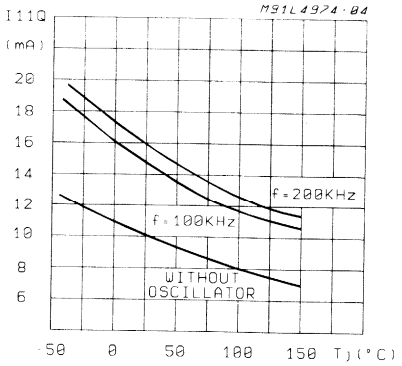


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

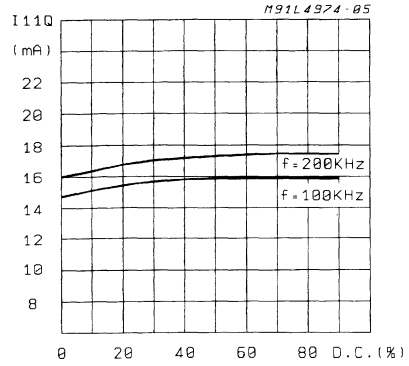


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

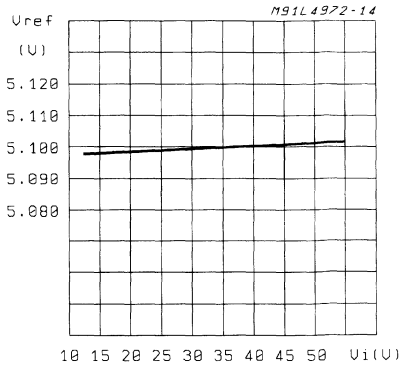


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

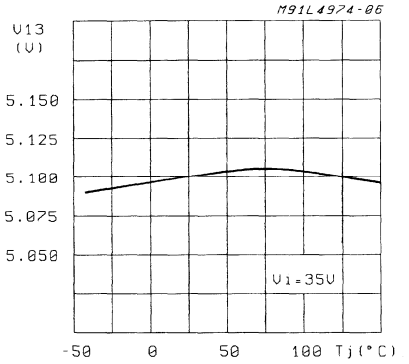


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

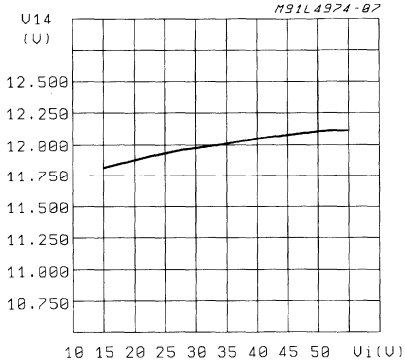


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

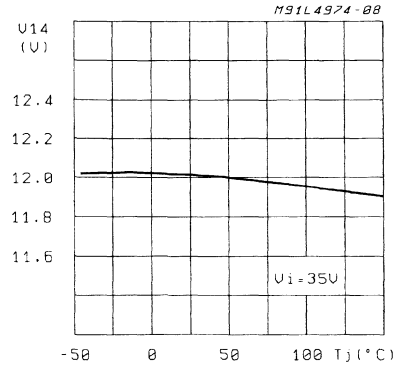


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-

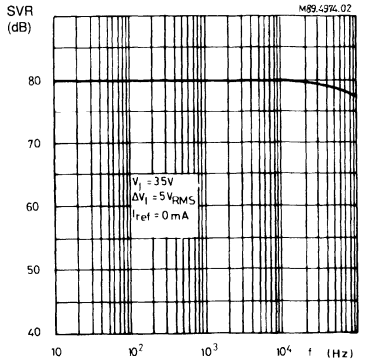


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

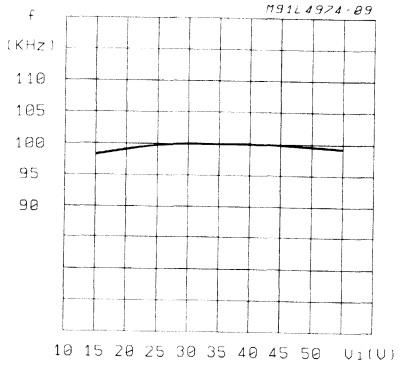


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

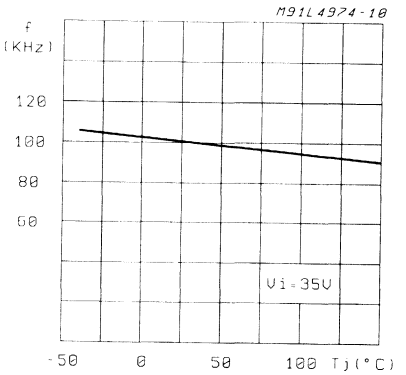


Figure 18 : Switching Frequency vs. R4 (see fig.5).

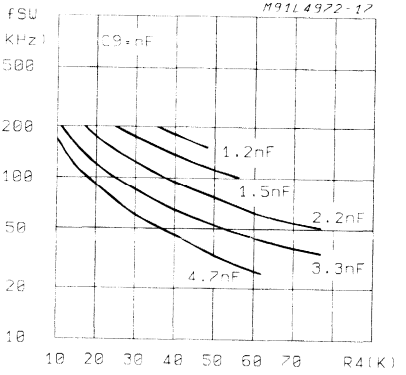


Figure 19 : Maximum Duty Cycle vs. Frequency.

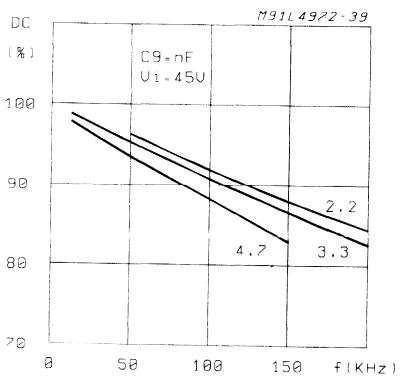


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

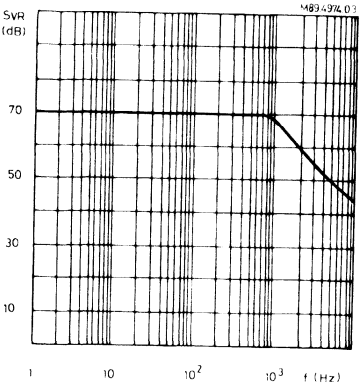


Figure 21 : Efficiency vs. Output Voltage.

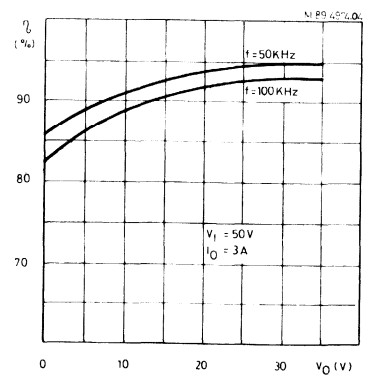


Figure 22 : Line Transient Response (see fig. 5).

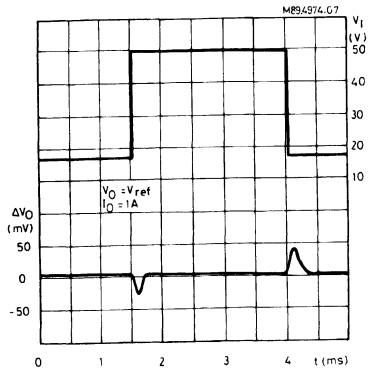


Figure 23 : Load Transient Response (see fig. 5).

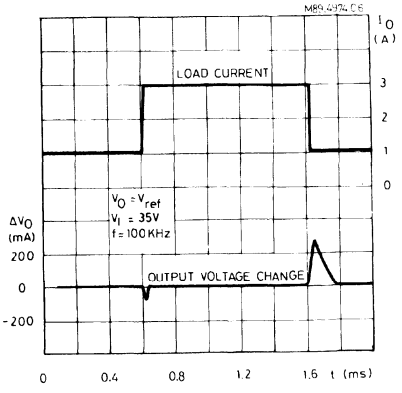


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

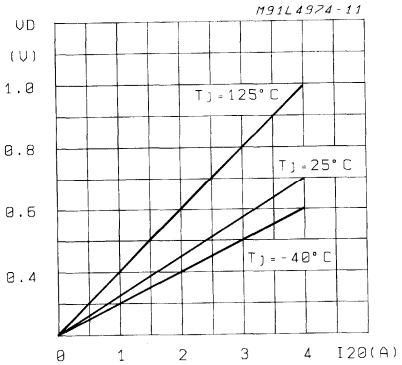


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

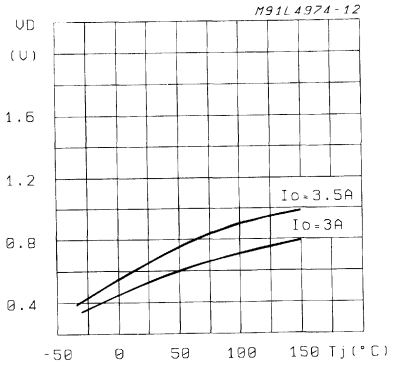


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

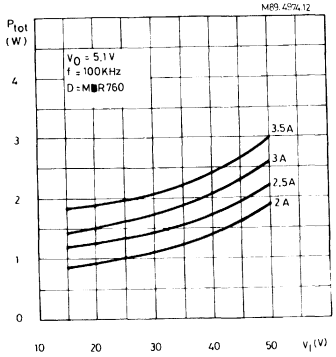


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

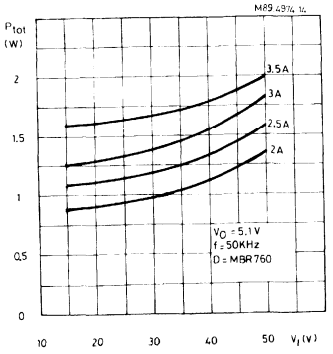


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

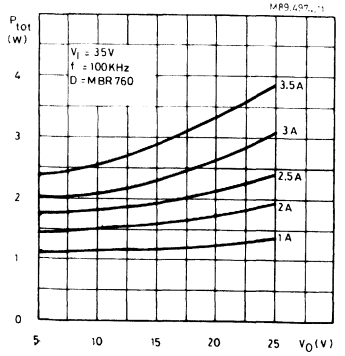


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

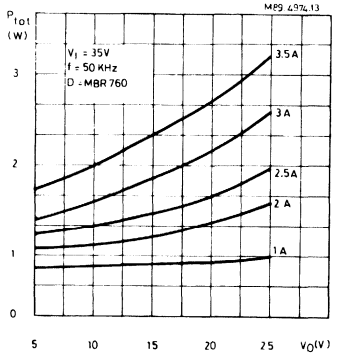


Figure 30 : Power Dissipation (device only) vs. Output Current.

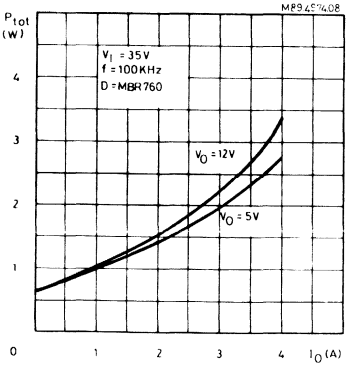


Figure 31 : Power Dissipation (device only) vs. Output Current.

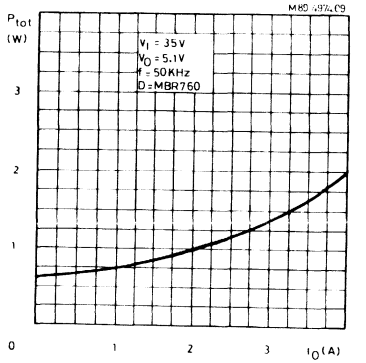


Figure 32 : Efficiency vs. Output Current.

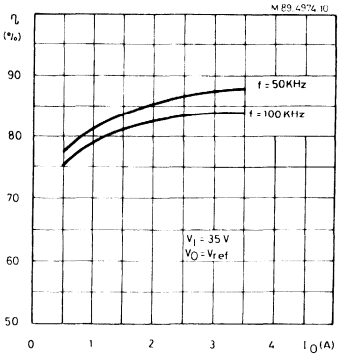


Figure 33 : Test PCB Thermal Characteristic.

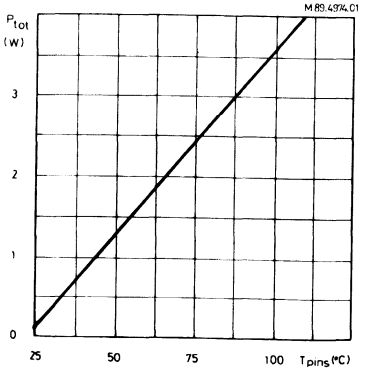


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

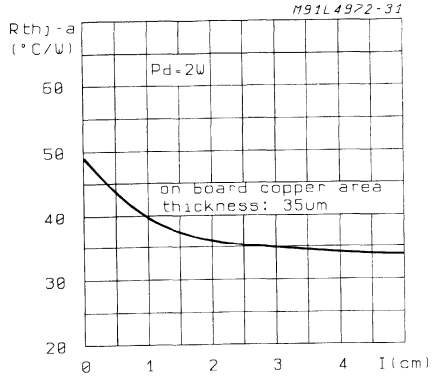


Figure 35: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

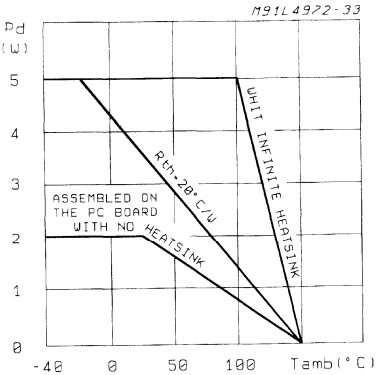


Figure 36: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

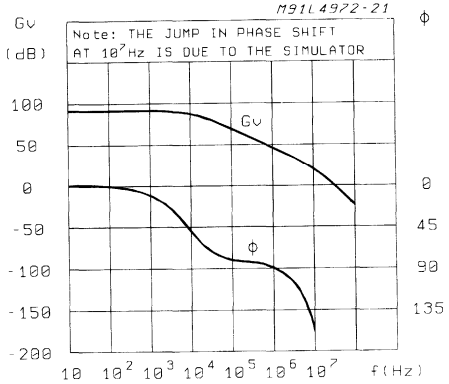


Figure 37 : 3.5A – 5.1V Low Cost Application Circuit.

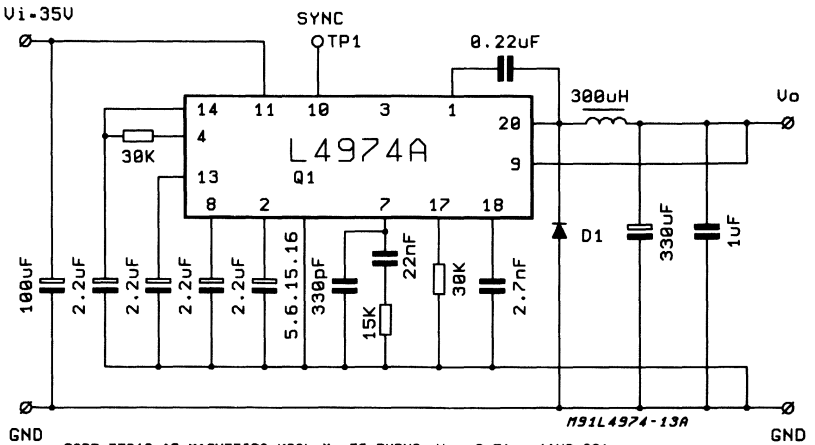


Figure 38 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4974A and L4970A.

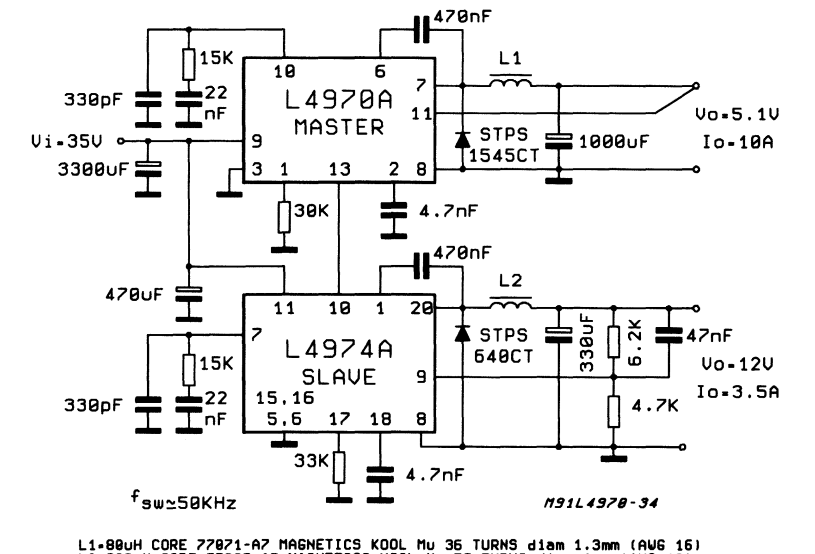


Figure 39 : L4974A's Sync. Example.

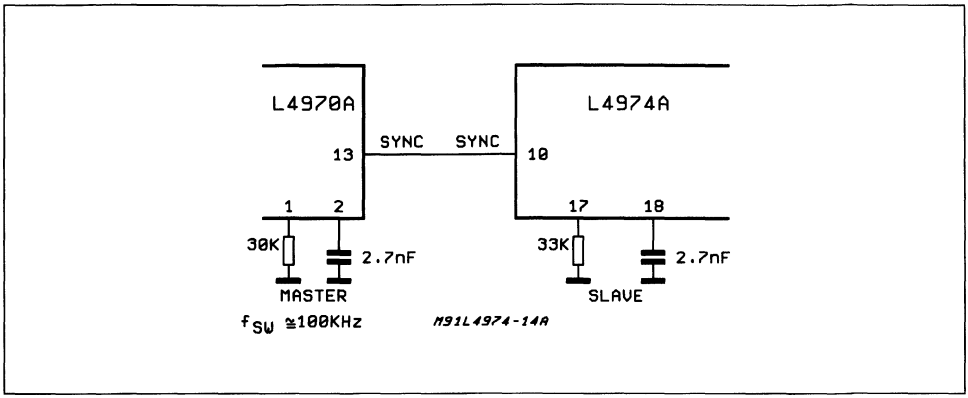
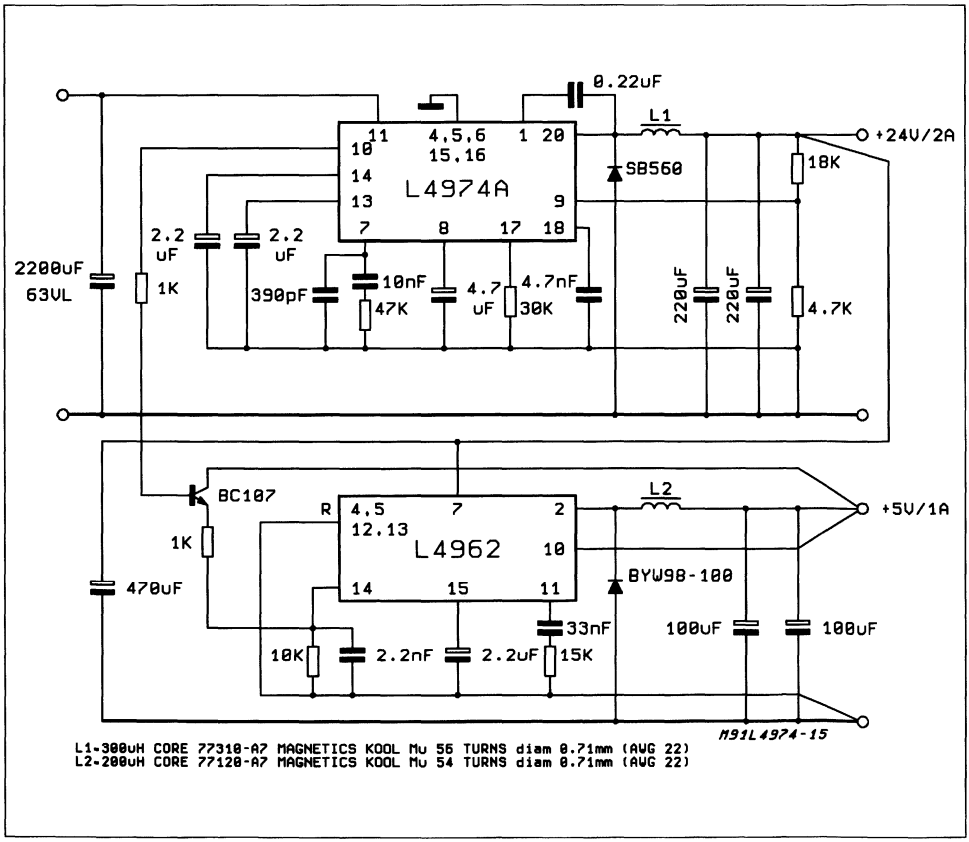


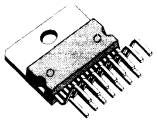
Figure 40: 1A/24V Multiple Supply. Note the synchronization between the L4974A and L4962



5A SWITCHING REGULATOR

- 5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



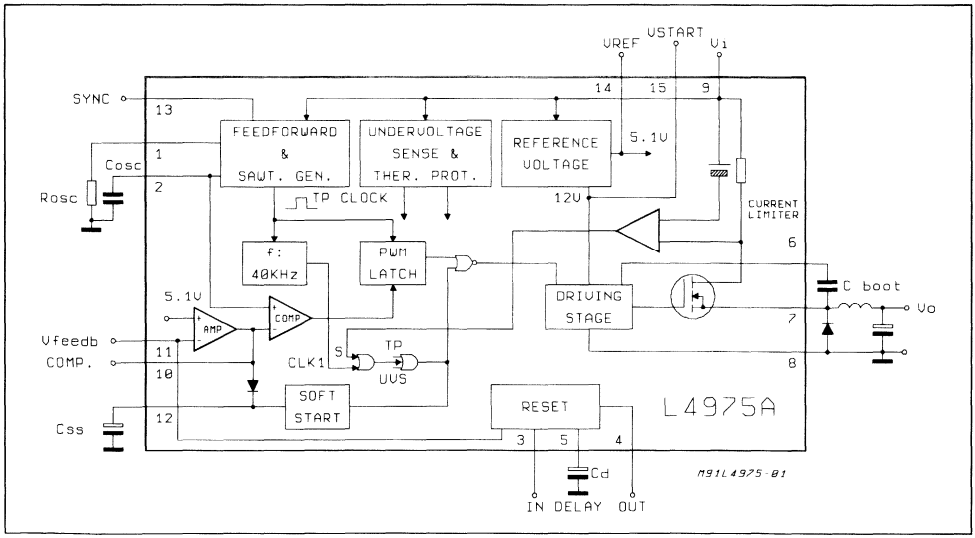
Multiwatt15V
ORDERING NUMBER: L4975A

DESCRIPTION

The L4975A is a stepdown monolithic power switching regulator delivering 5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4975A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

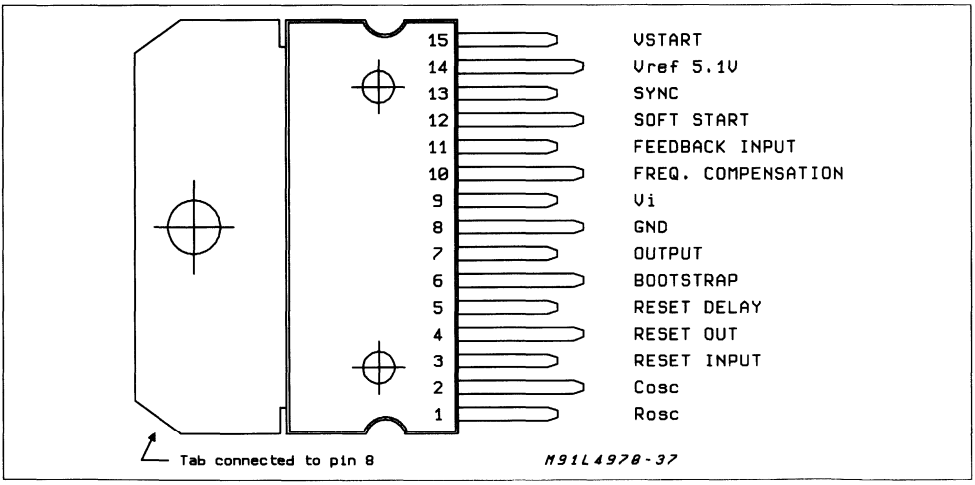
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4975A are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4975A is a 5A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 5A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

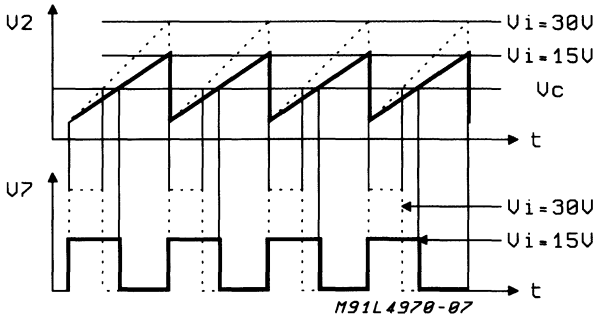


Figure 2: Soft Start Function

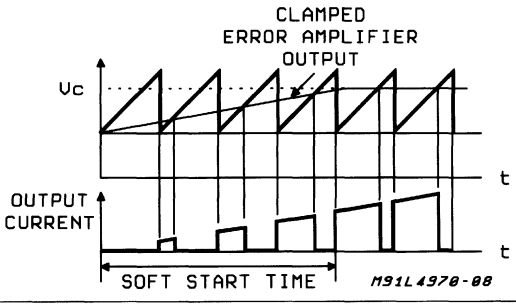
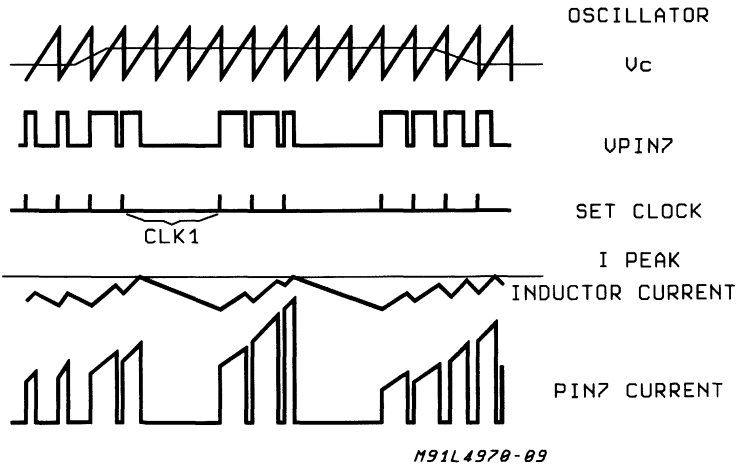


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

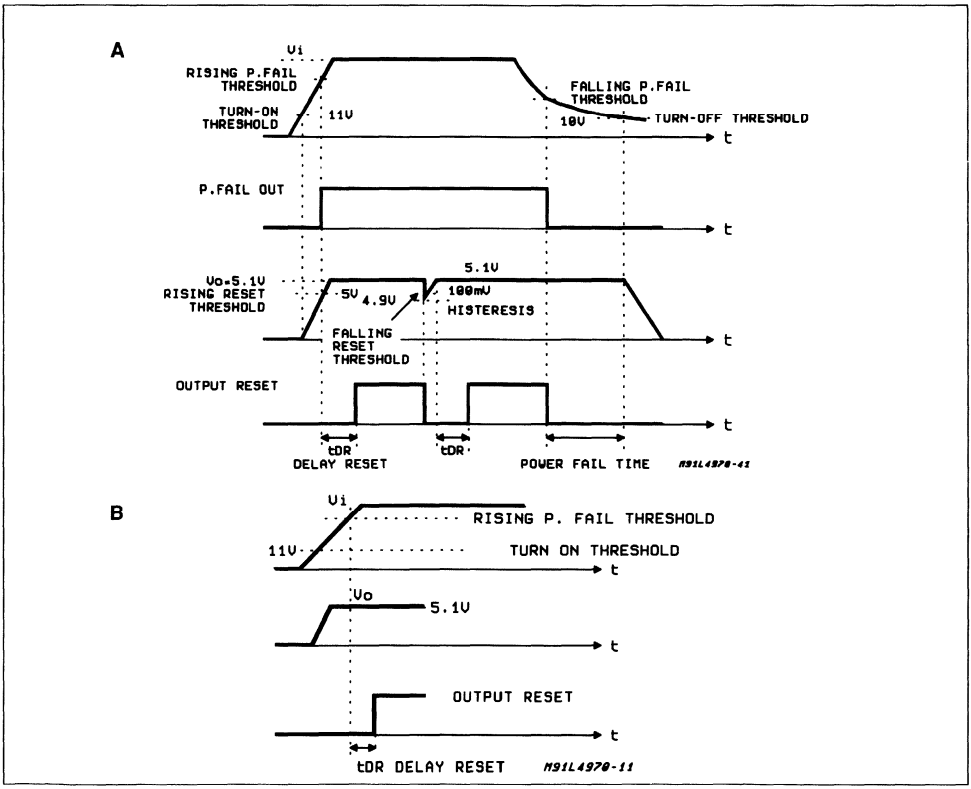
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	V_o = V_{ref} to 40V I_o = 5A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 2A to 4A I_o = 1A to 5A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 3A I_o = 5A		0.4 0.55	0.6 0.8	V V	5
I_{7L}	Max. Limiting Current	V_i = 15 to 50V V_o = V_{ref} to 40V	5.5	6.5	7.5	A	5
η	Efficiency	I_o = 3A V_o = V_{ref} V_o = 12V	70	75 80		% %	5
		I_o = 5A V_o = V_{ref} V_o = 12V	80	85 92		% %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref}; R_4 = 10KΩ I_o = 5A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\,Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	V_{12} = 0; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	V_i = 55V; S3 = A; V_{12} = 0			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V; V_{11} = 0V	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	I_{12} = 20mA; V_9 = 10V			1	V	7B
		I_{12} = 200µA; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	I_{10} = -100µA; S1 = C V_{11} = 4.7V	6			V	7C
V_{10L}	Low Level Out Voltage	I_{10} = +100µA; S1 = C V_{11} = 5.3V;			1.2	V	7C
I_{10H}	Source Output Current	V_{10} = 1V; S1 = E V_{11} = 4.7V	100	150		µA	7C
I_{10L}	Sink Output Current	V_{10} = 6V; S1 = D V_{11} = 5.3V	100	150		µA	7C
I_{11}	Input Bias Current	R_S = 10KΩ		0.4	3	µA	–
G_V	DC Open Loop Gain	V_{VCM} = 4V; R_S = 10Ω	60			dB	–
SVR	Supply Voltage Rejection	15 < V_i < 50V; R_S = 10Ω	60	80		dB	–
V_{OS}	Input Offset Voltage	R_S = 50Ω		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C	V_i = 15V		2.5		V	7A
		S2 = B	V_i = 45V		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; I_1 = 100µA			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; I1 = 1mA		2.4	2.7		mA	7A

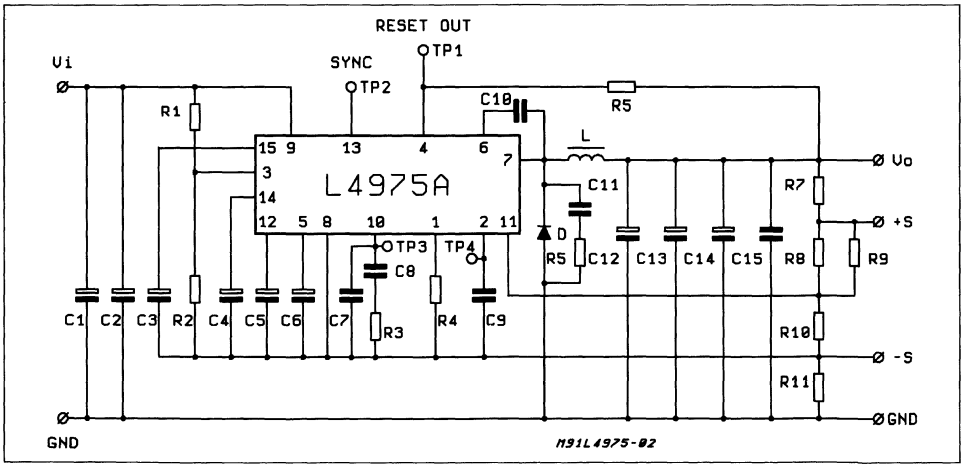
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	V_i = 15V to 50V; V_{12} = 0; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	V_{12} = 0; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	V_2 = V_{13} = 0.9V; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	V_{13} = 3.5V; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

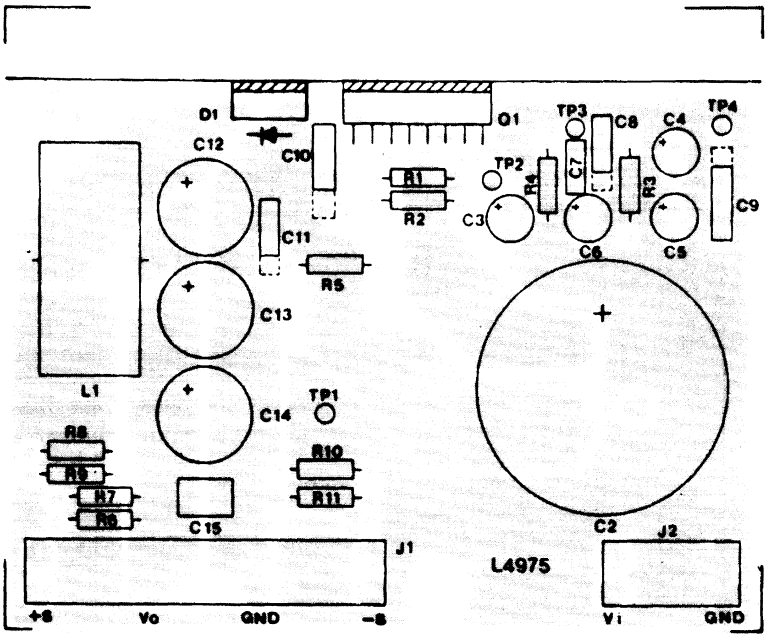
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} −120	V_{ref} −100	V_{ref} −80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	Vi = 15 to 50V V_3 = 5.3V	4.77	V_{ref} −200	V_{ref} −160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	Vi = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 5A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 5A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 760CT (or 7.5A/60V or equivalent)	
L1 = 80µH	core 58930 MAGNETICS 24 TURNS Ø 1.1mm (AWG 17) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

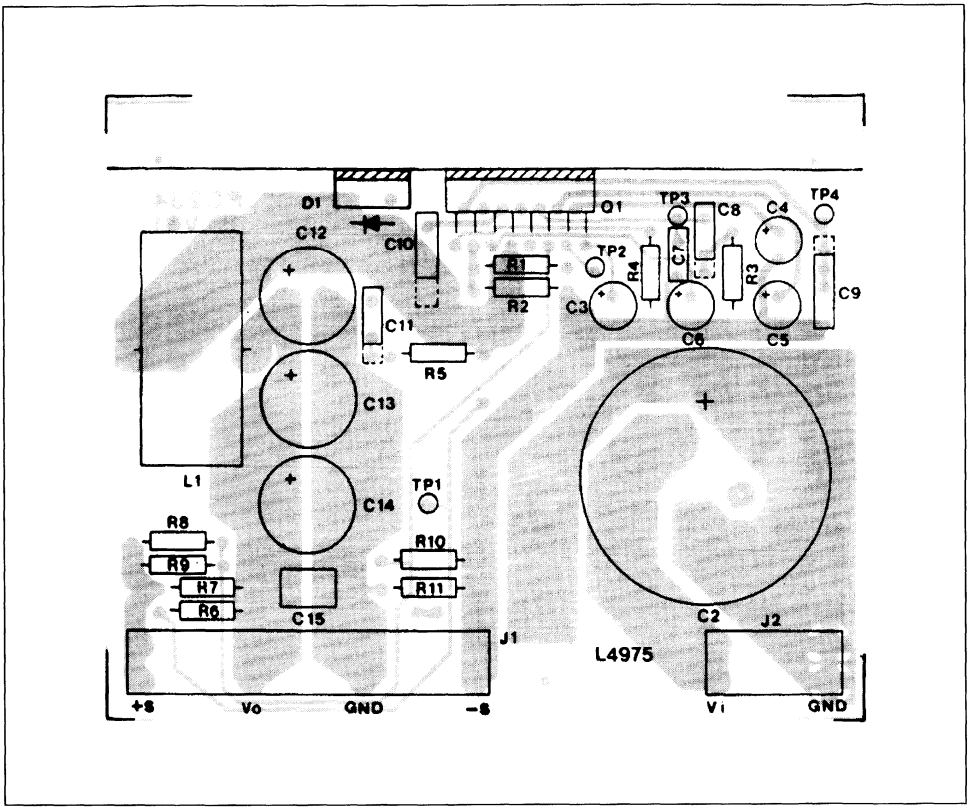


Figure 7: DC Test Circuits

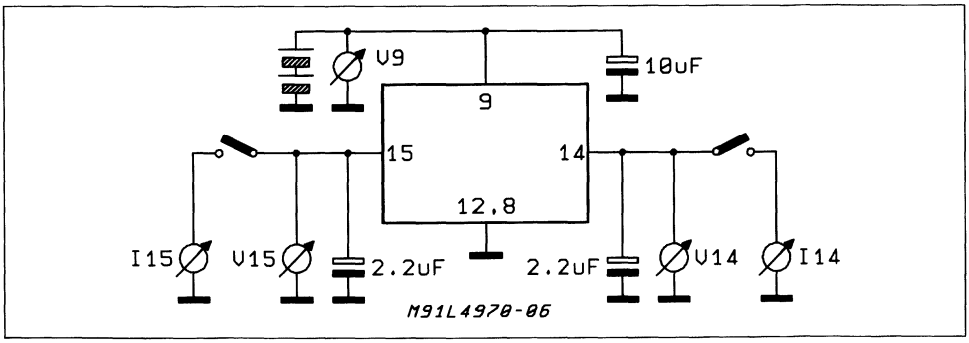


Figure 7A

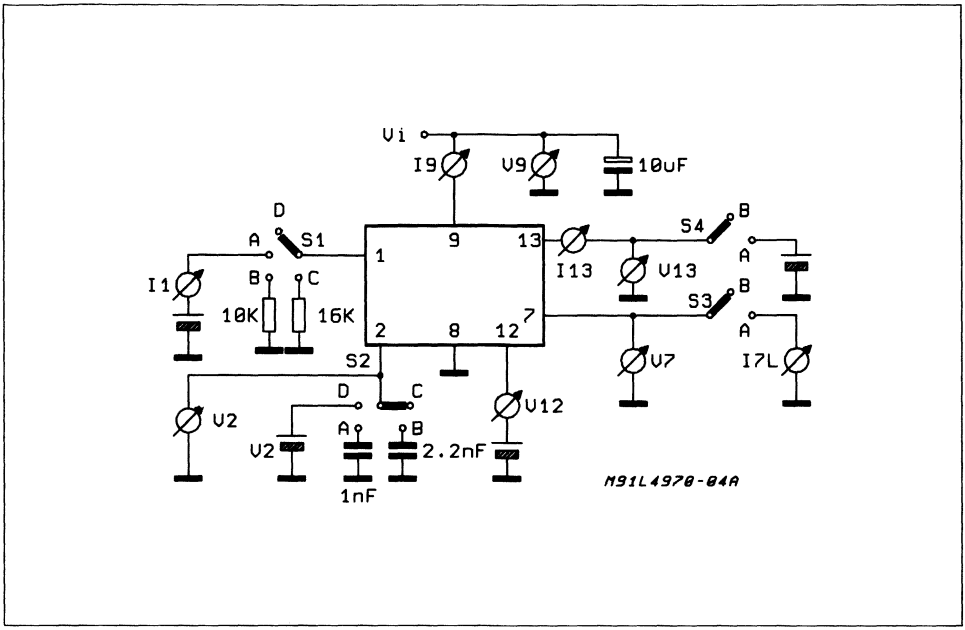


Figure 7B

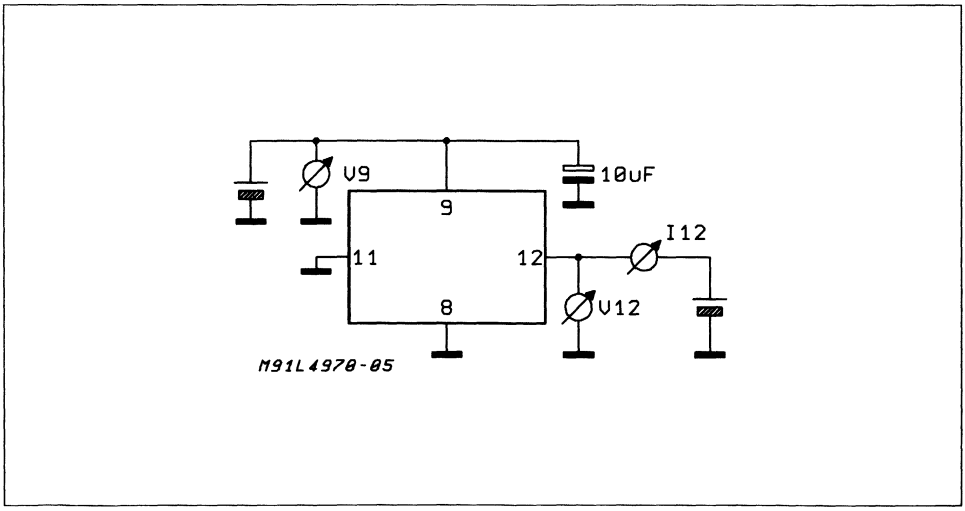


Figure 7D

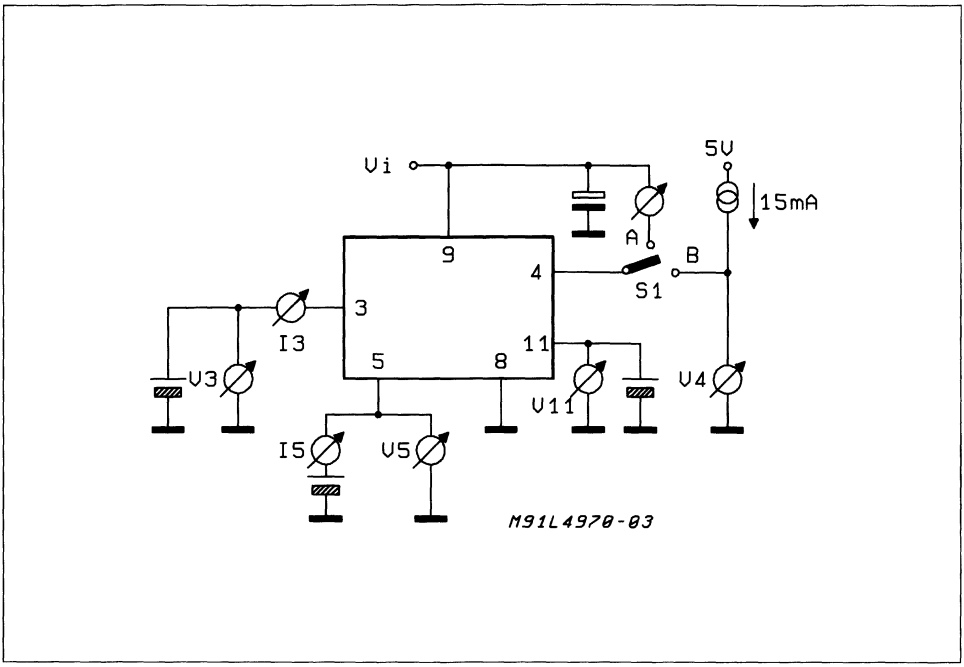


Figure 7C

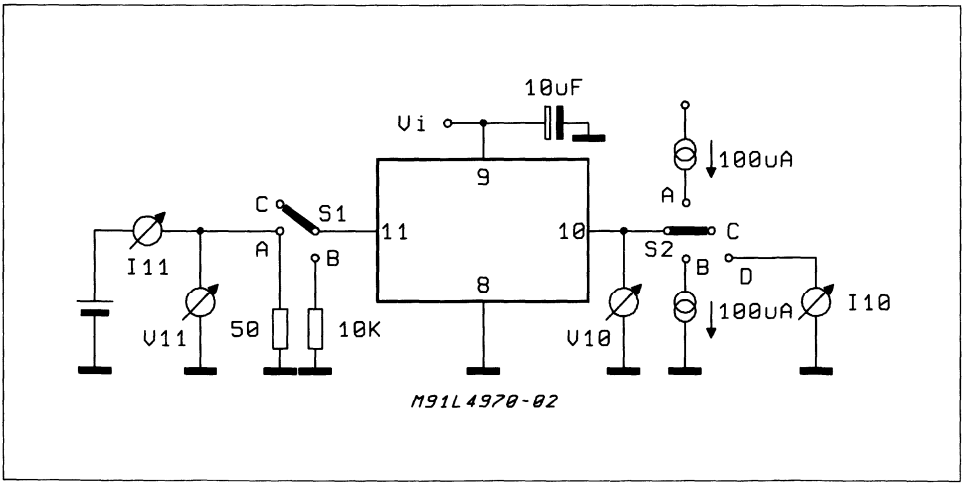


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

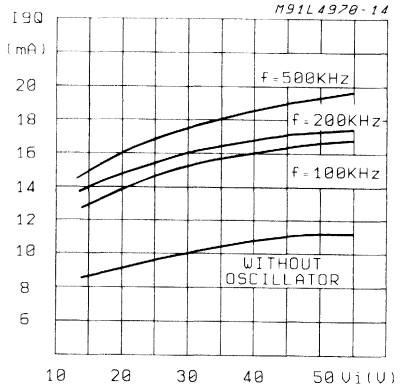


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

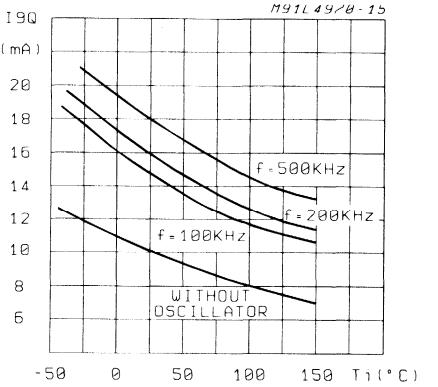


Figure 10: Quiescent Drain Current vs. Duty Cycle

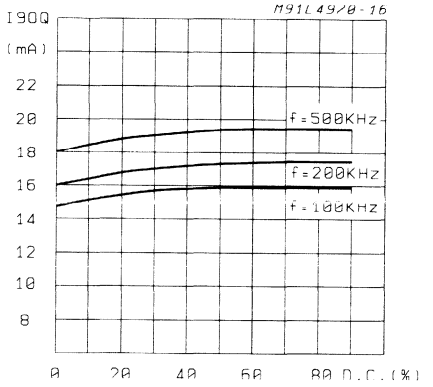


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

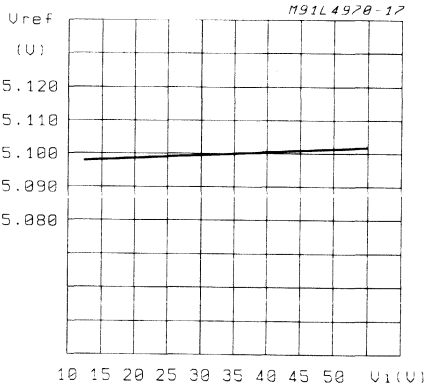


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

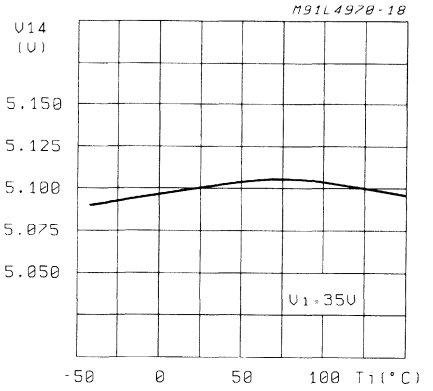


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

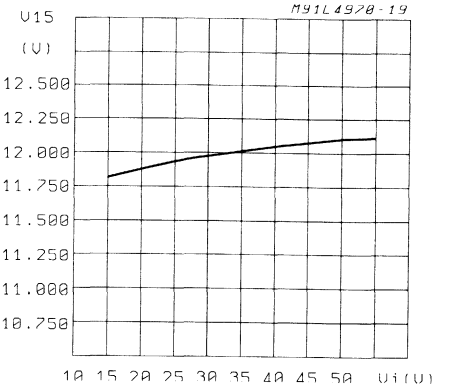


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

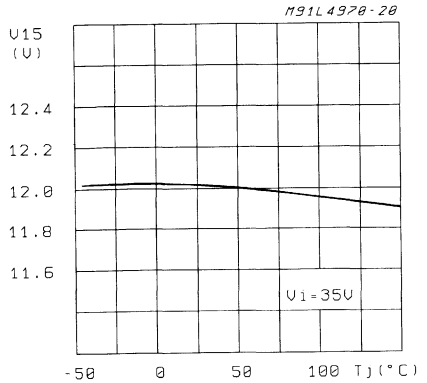


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

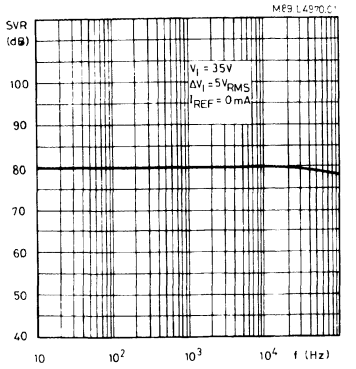


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

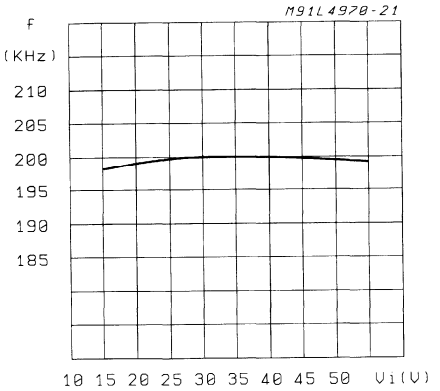


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

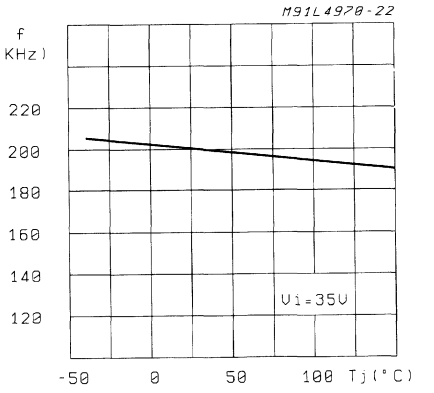


Figure 18: Switching Frequency vs. R4 (see fig. 5)

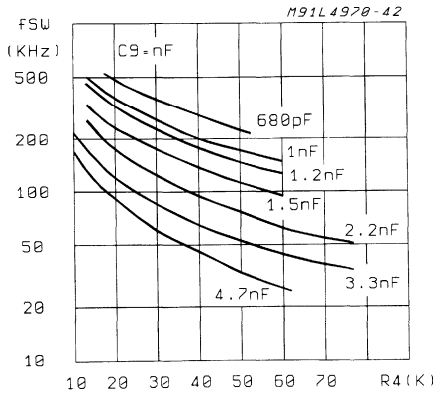


Figure 19: Max. Duty Cycle vs. Frequency

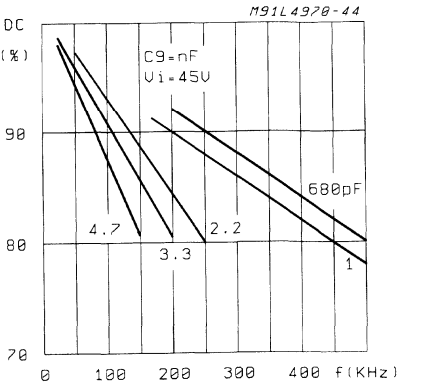


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

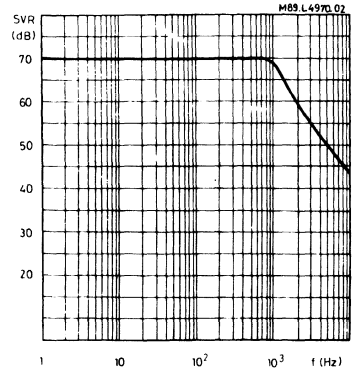


Figure 21: Line Transient Response (see fig. 5)

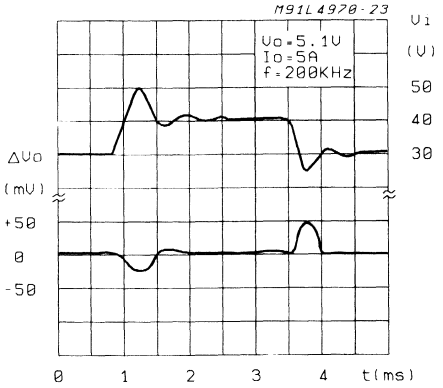


Figure 22: Load Transient Response (see fig. 5)

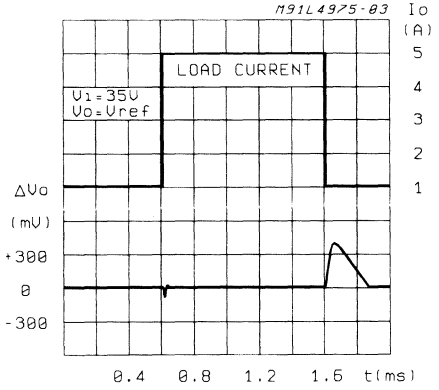


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

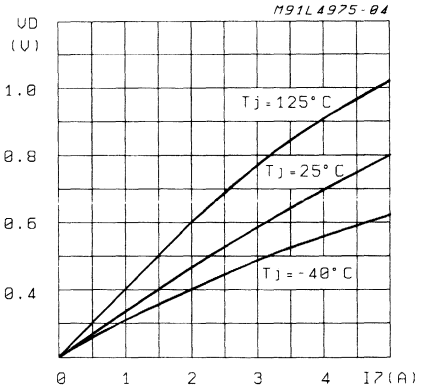


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

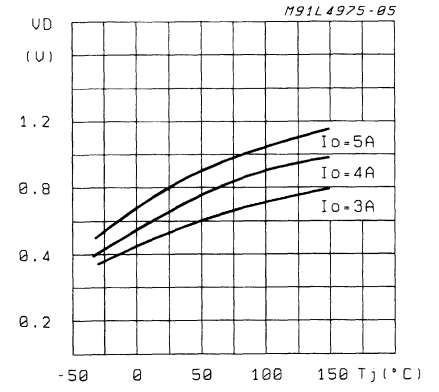


Figure 25: Power Dissipation (device only) vs. Input Voltage

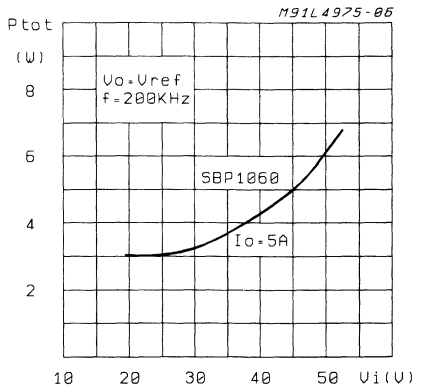


Figure 26: Power Dissipation (device only) vs. Output Voltage

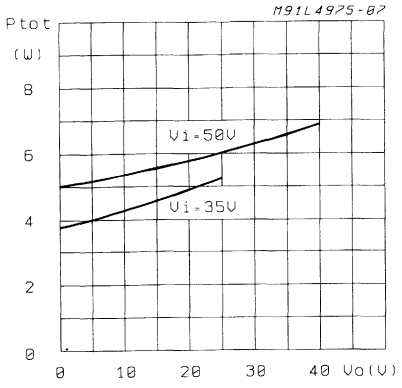


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

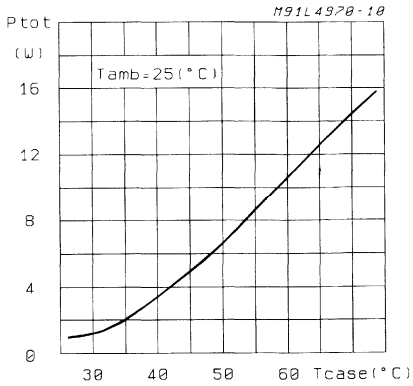


Figure 28: Efficiency vs. Output Current

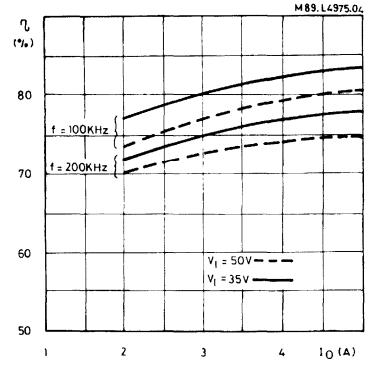


Figure 29: Efficiency vs. Output Voltage

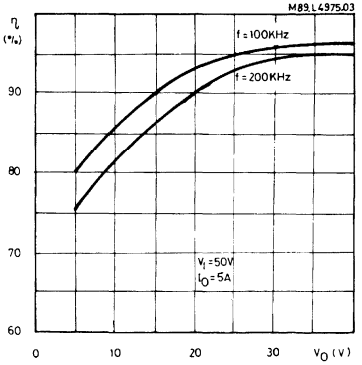


Figure 30: Efficiency vs. Output Voltage

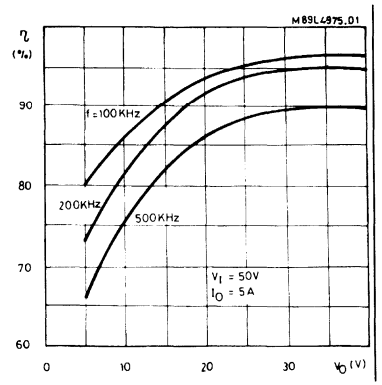


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

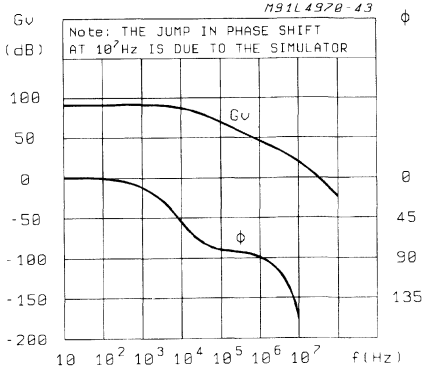


Figure 32: Power Dissipation Derating Curve

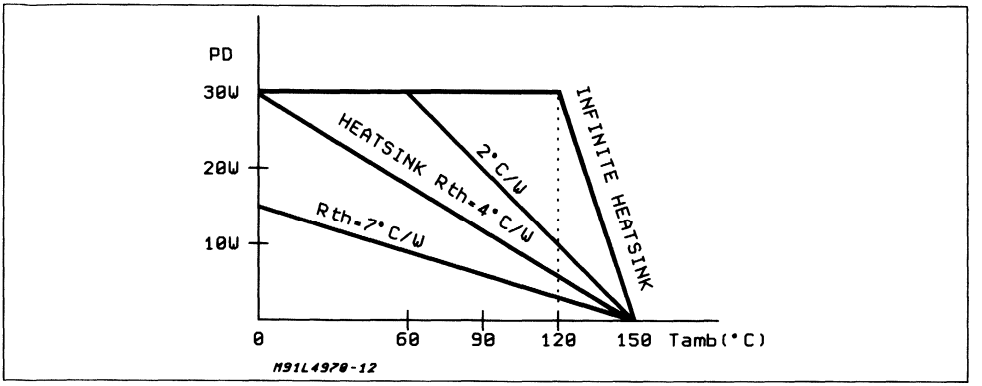


Figure 33: 5.1V/12V Multiple Supply. Note the Synchronization between the L4975A and the L4974A

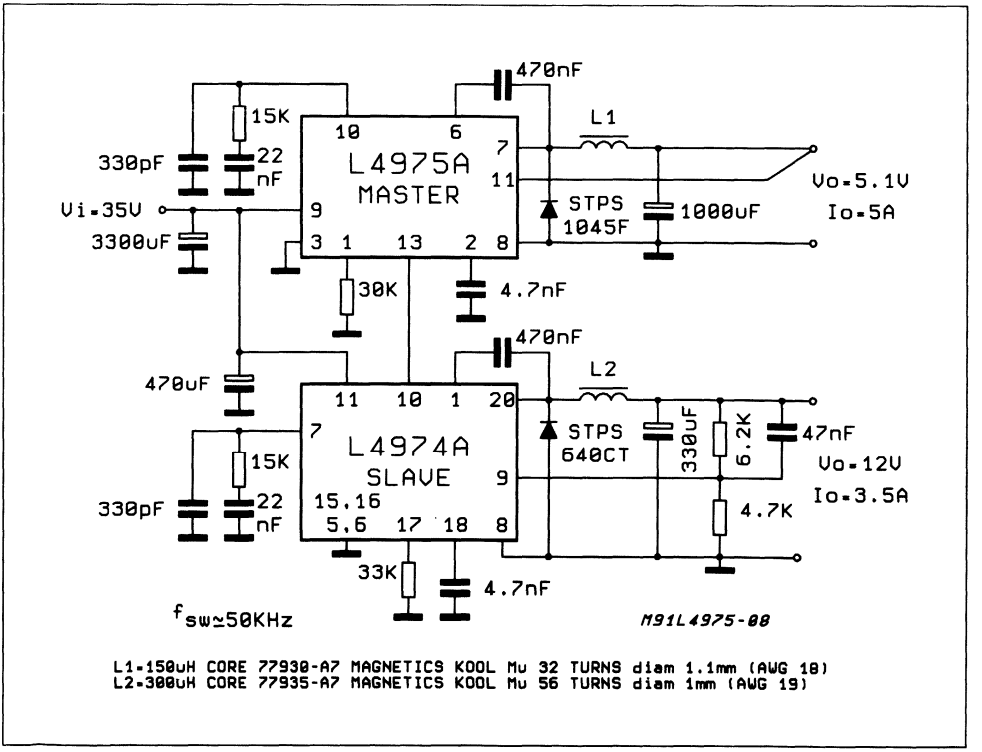


Figure 34: 5.1V / 5A Low Cost Application

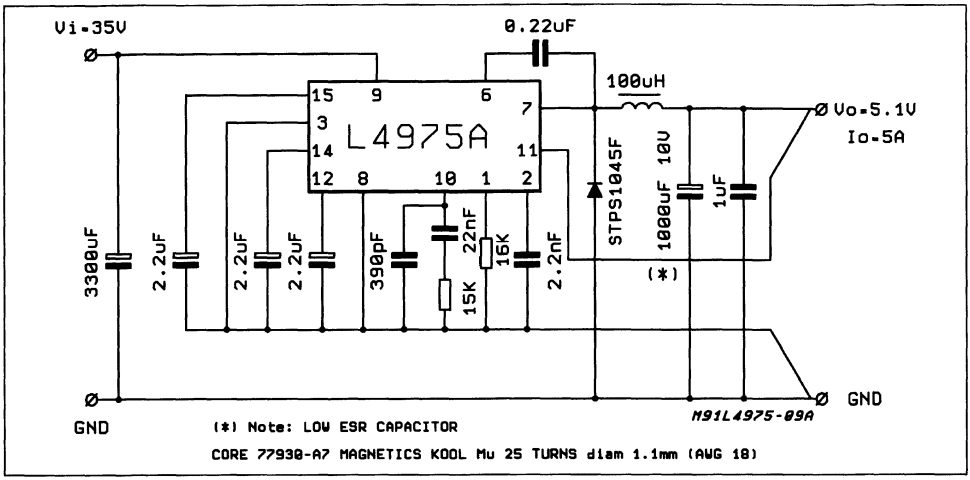


Figure 35: 5A Switching Regulator, Adjustable from 0V to 25V.

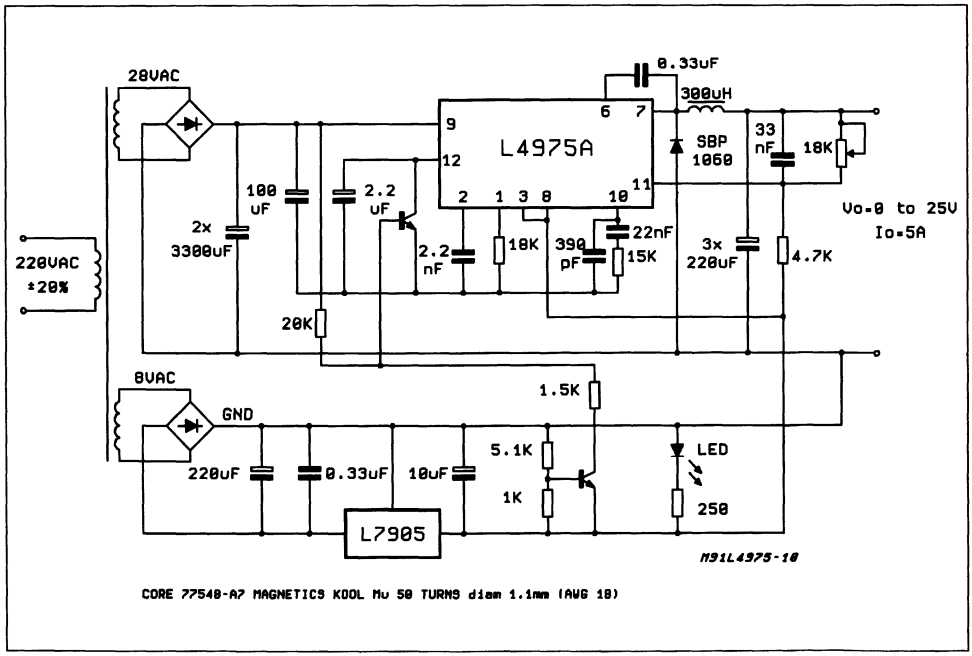
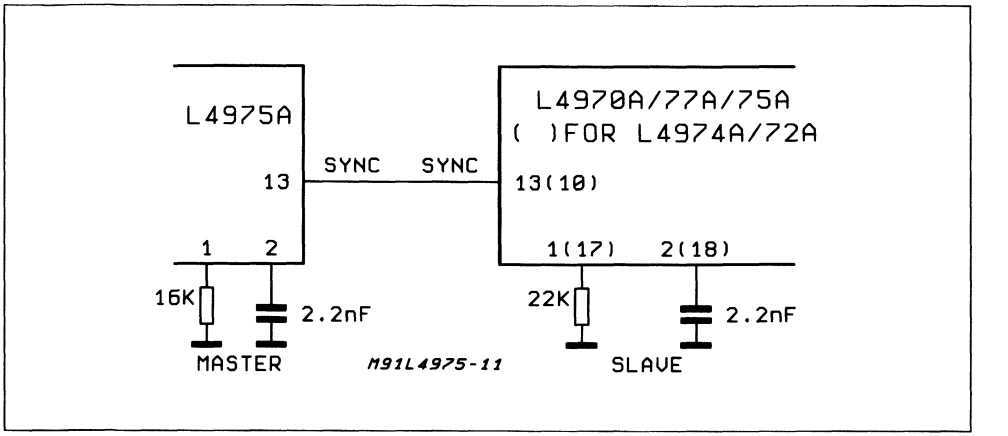


Figure 36: L4975A's Sync. Example



7A SWITCHING REGULATOR

- 7A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY

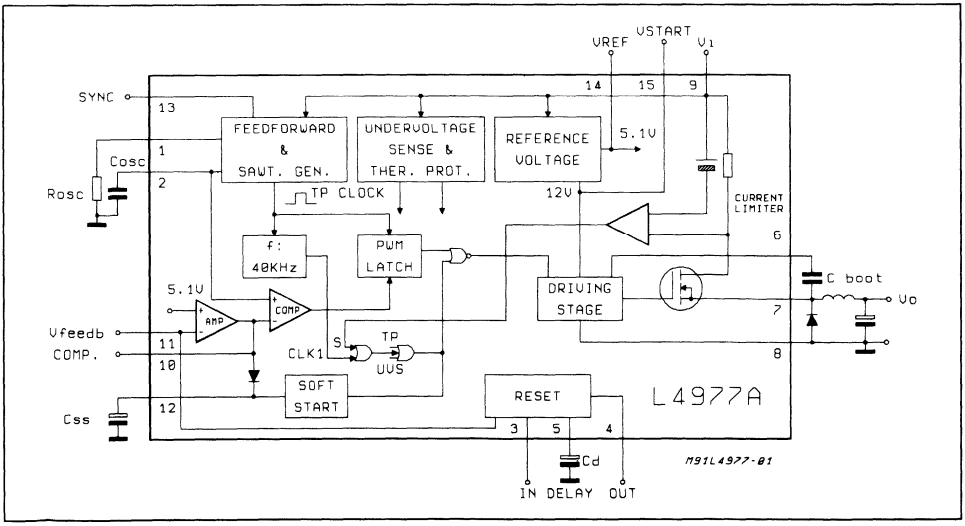
Multiwatt15V
ORDERING NUMBER: L4977A

DESCRIPTION

The L4977A is a stepdown monolithic power switching regulator delivering 7A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4977A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

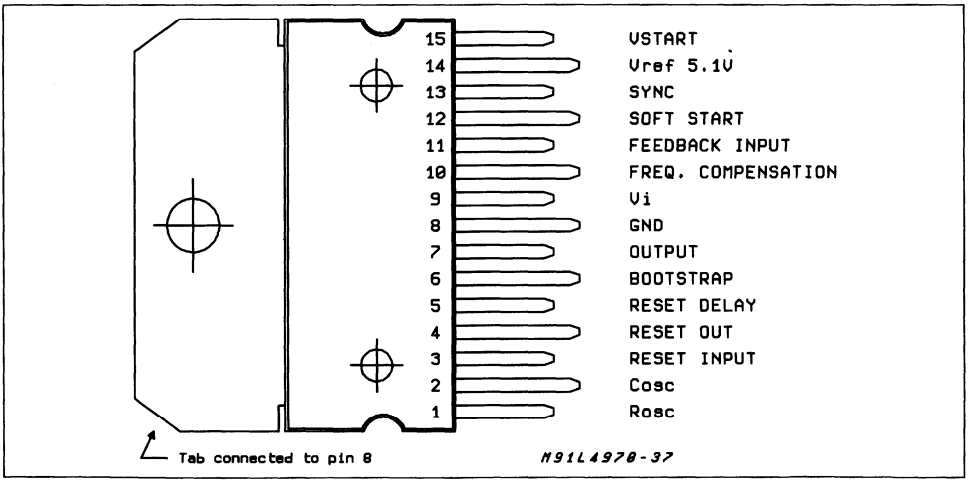
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	-1 -7	V V
I_7	Maximum Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	A
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4977A are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4977A is a 7A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 7A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator, in order to generate a fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and

Figure 1: Feedforward Waveform

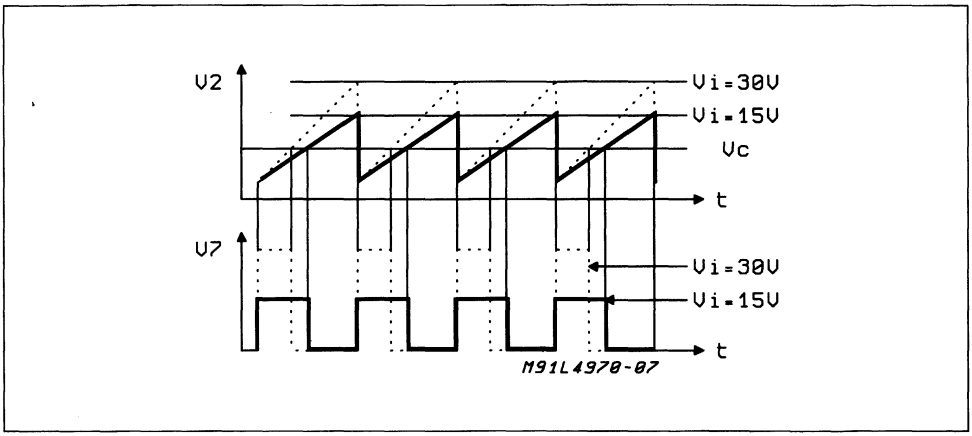


Figure 2: Soft Start Function

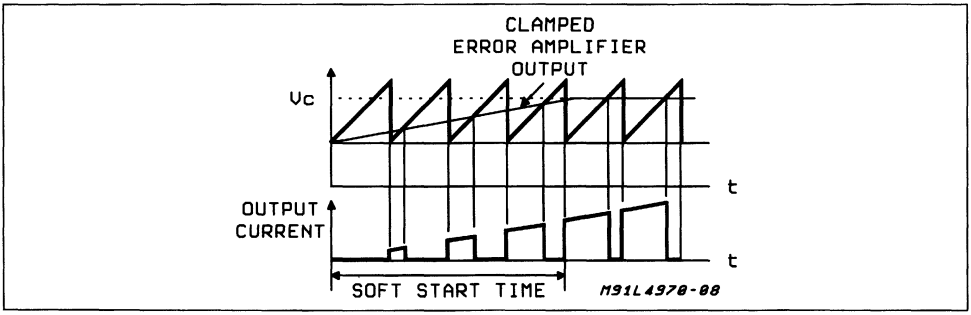
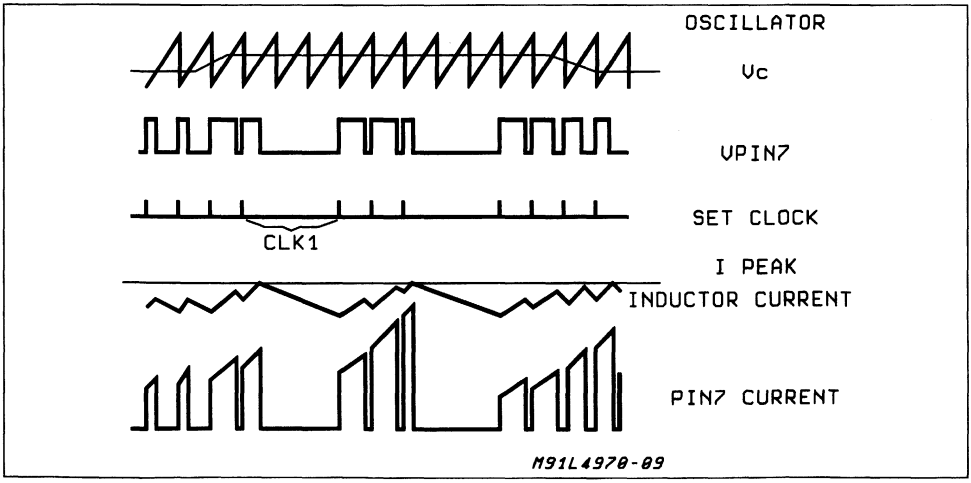


Figure 3: Limiting Current Function



stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit (fig. 3). The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

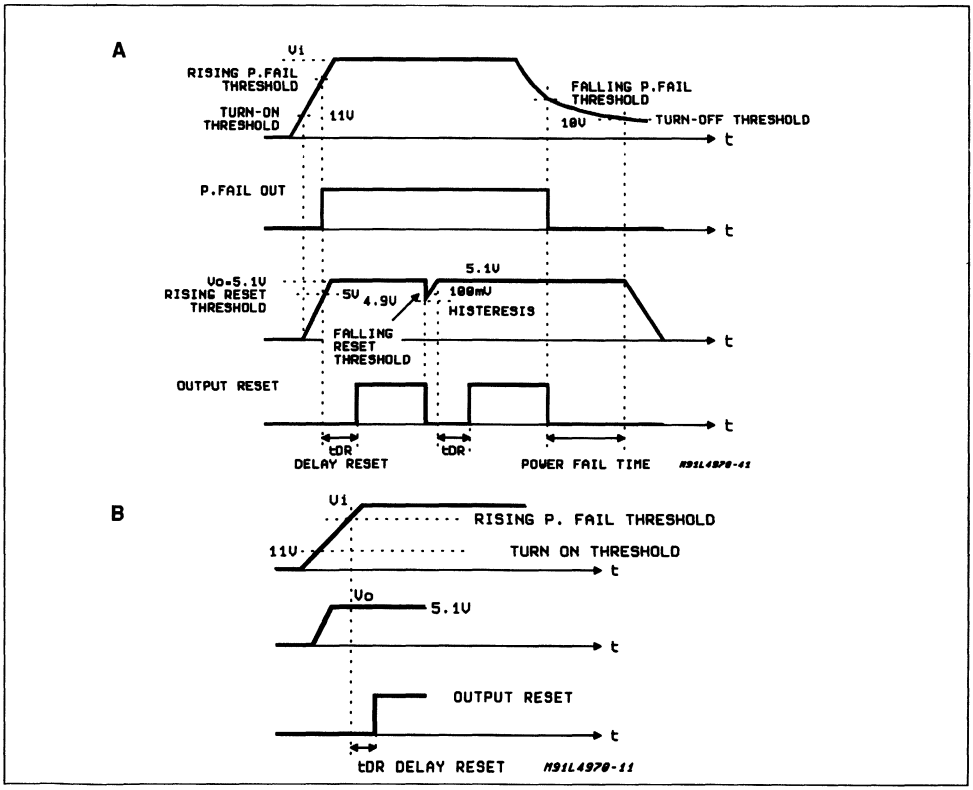
The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4: Reset and Power Fail Functions.



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 16KΩ, C_9 = 2.2nF, f_{SW} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_i	input Voltage Range (pin 9)	$V_o = V_{ref}$ to 40V I_o = 7A	15		50	V	5
V_o	Output Votage	V_i = 15V to 50V I_o = 3A; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A; $V_o = V_{ref}$		12	30	mV	5
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 3A to 5A I_o = 2A to 7A		 10 20	 25 40	 mV mV	5
V_d	Dropout Voltage Between Pin 9 and 7	I_o = 5A I_o = 7A		0.4 0.8	0.6 1.1	V V	5
I_{7L}	Max. Limiting Current	$V_o = V_{ref}$ to 40V V_i = 15 to 50V	8	9.5	11	A	5
η	Efficiency	I_o = 3A $V_o = V_{ref}$ V_o = 12V	70	75 80		% %	5
		I_o = 7A $V_o = V_{ref}$ V_o = 12V	75	80 87		% %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS; I_o = 3A f = 100Hz; $V_o = V_{ref}$	56	60		dB	5
f	Switching Frequency		180	200	220	KHz	5
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Swiching Frequency	V_i = 15V to 45V		2	6	%	5
$\frac{\Delta f}{T_j}$	Temperature Stability of Swiching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; R_4 = 10KΩ I_o = 7A; C_9 = 1nF	500			KHz	5

V_{ref} SECTION (pin 14)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{14}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{14}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{14\ short}$	Short Circuit Current Limit	V_{14} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{15}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{15}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{15}	Load Regulation	I_{15} = 0 to 1mA		50	200	mV	7
$I_{15\ short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Threshold		10	11	12	V	7A
$V_{9\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{9Q}	Quiescent Current	$V_{12} = 0$; S1 = D		13	19	mA	7A
I_{9OQ}	Operating Supply Current	$V_{12} = 0$; S1 = C; S2 = B		16	23	mA	7A
I_{7L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_{12} = 0$			2	mA	7A

SOFT START

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	$V_{12} = 3V$; $V_{11} = 0V$	70	100	130	µA	7B
V_{12}	Output Saturation Voltage	$I_{12} = 20mA$; $V_9 = 10V$			1	V	7B
		$I_{12} = 200µA$; $V_9 = 10V$			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level Out Voltage	$I_{10} = -100µA$; S1 = C $V_{11} = 4.7V$	6			V	7C
V_{10L}	Low Level Out Voltage	$I_{10} = +100µA$; S1 = C $V_{11} = 5.3V$;			1.2	V	7C
I_{10H}	Source Output Current	$V_{10} = 1V$; S1 = E $V_{11} = 4.7V$	100	150		µA	7C
I_{10L}	Sink Output Current	$V_{10} = 6V$; S1 = D $V_{11} = 5.3V$	100	150		µA	7C
I_{11}	Input Bias Current	$R_S = 10K\Omega$		0.4	3	µA	–
G_V	DC Open Loop Gain	$V_{VCM} = 4V$; $R_S = 10\Omega$	60			dB	–
SVR	Supply Voltage Rejection	$15 < V_i < 50V$; $R_S = 10\Omega$	60	80		dB	–
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$		2	10	mV	–

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit	Fig.
V_2	Ramp Valley	S1 = C; S2 = B		1.2	1.5		V	7A
V_2	Ramp Peak	S1 = C	$V_i = 15V$		2.5		V	7A
		S2 = B	$V_i = 45V$		5.5		V	7A
I_2	Min. Ramp Current	S1 = A; $I_1 = 100µA$			270	300	µA	7A
I_2	Max. Ramp Current	S1 = A; $I_1 = 1mA$		2.4	2.7		mA	7A

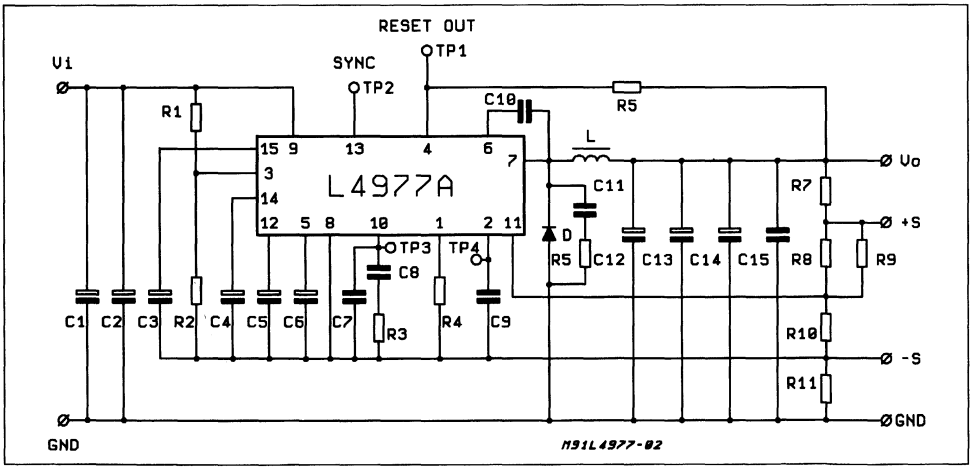
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Low Input Voltage	$V_i = 15V$ to 50V; $V_{12} = 0$; S1 = C; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{13}	High Input voltage	$V_{12} = 0$; S1 = C; S2 = B; S4 = B	3.5		5.5	V	7A
I_{13L}	Sync Input Current with Low Input Voltage	$V_{13} = V_2 = 0.9V$; S4 = A; S1 = C; S2 = B			0.4	mA	7A
I_{13H}	Input Current with High Input Voltage	$V_{13} = 3.5V$; S4 = A; S1 = C; S2 = B			1.5	mA	7A
V_{13}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)
RESET AND POWER FAIL FUNCTIONS

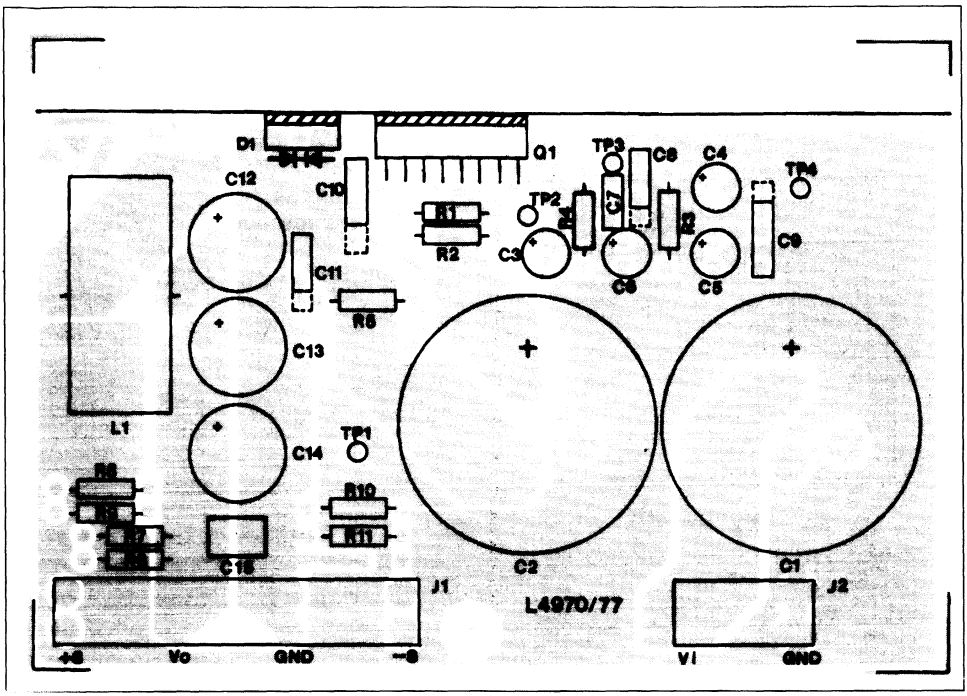
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	V_{ref} –120	V_{ref} –100	V_{ref} –80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	V_i = 15 to 50V V_3 = 5.3V	4.77	V_{ref} –200	V_{ref} –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	4.95	5.1	5.25	V	7D
V_{5L}	Delay Low Threshold Voltage	V_i = 15 to 50V V_{11} = V_{14} V_3 = 5.3V	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V; V_5 = 3V	40	60	80	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V; V_5 = 3V	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA; S1 = B V_3 = 4.7V			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V; S1 = A V_3 = 5.3V			100	µA	7D
V_{3R}	Rising Threshold Voltage	V_{11} = V_{14}	4.95	5.1	5.25	V	7D
V_{3H}	Hysteresys		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 7A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 7A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 7A)
For component values, refer to test circuit part list.

Figure 6a: P.C. Board (components side) and Components Layout of Figure 5 (1:1 scale).



PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300μF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2μF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220μF 40V_L EKR
R_{10} = 4K7	C_{15} = 1μF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40μH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 5. (1:1 scale)

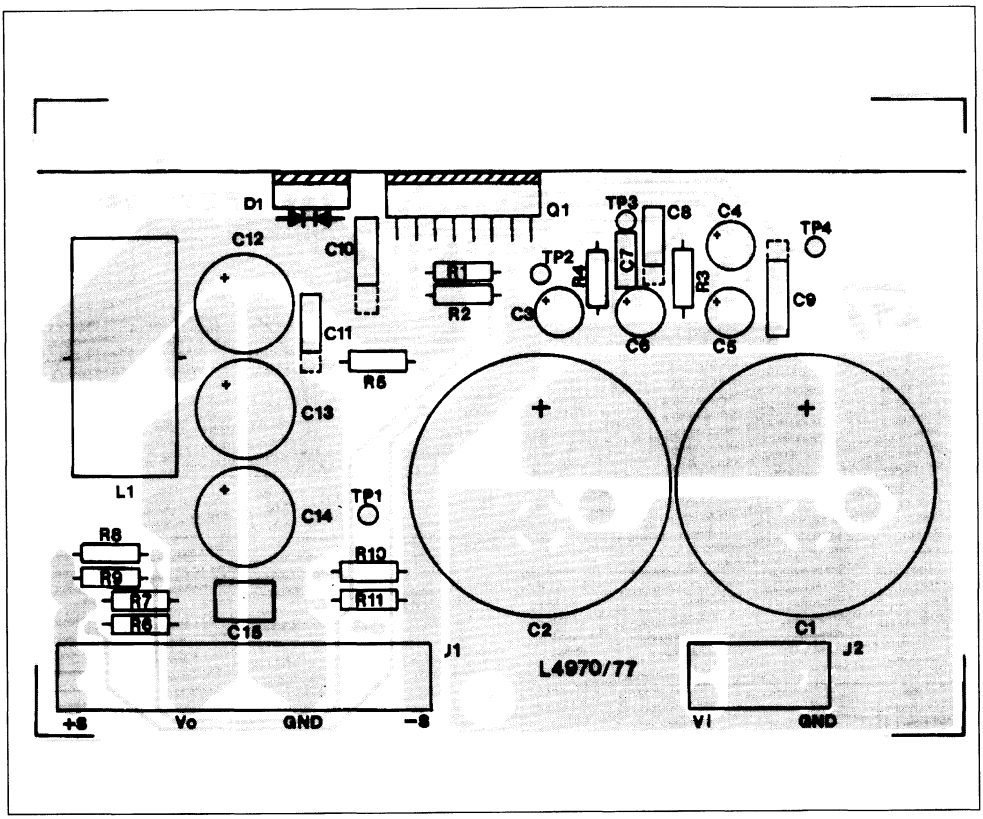


Figure 7: DC Test Circuits

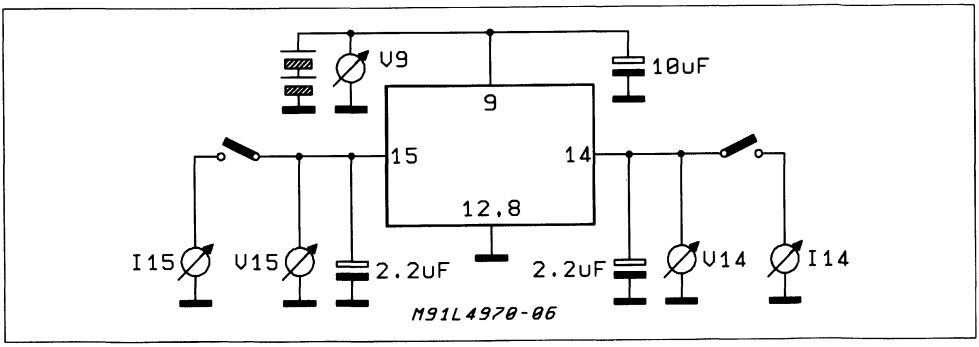


Figure 7A

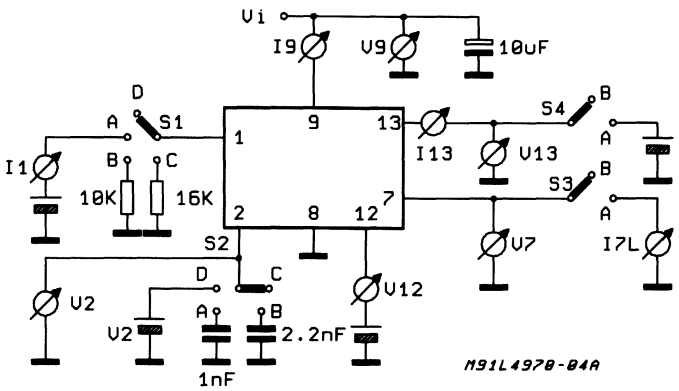


Figure 7B

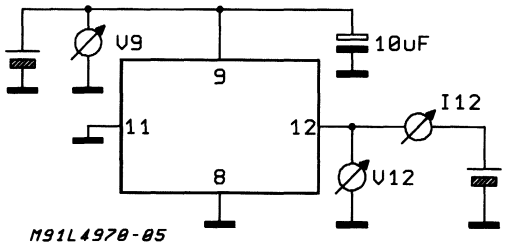


Figure 7D

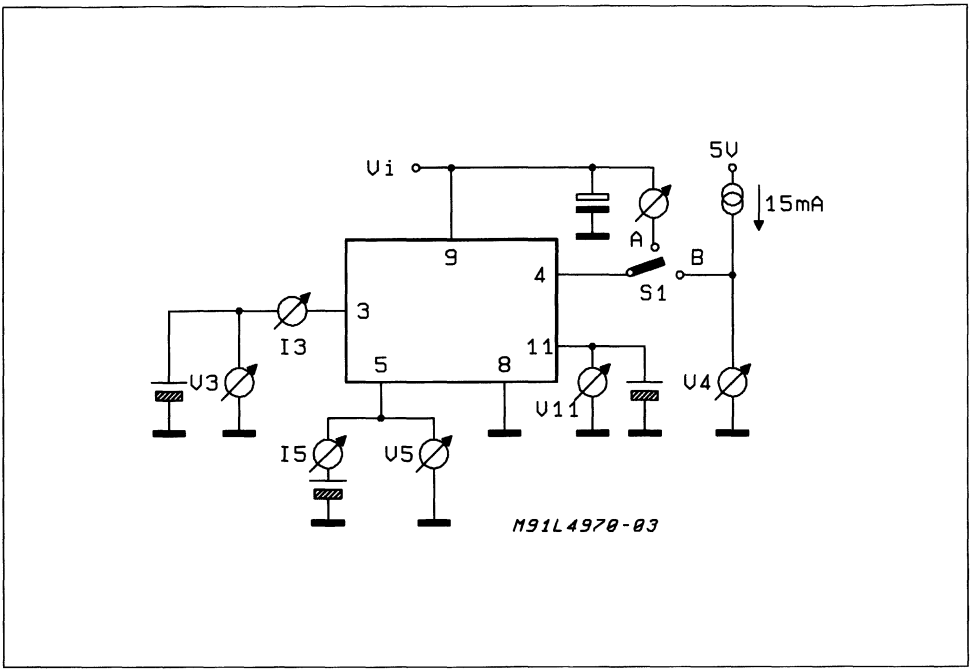


Figure 7C

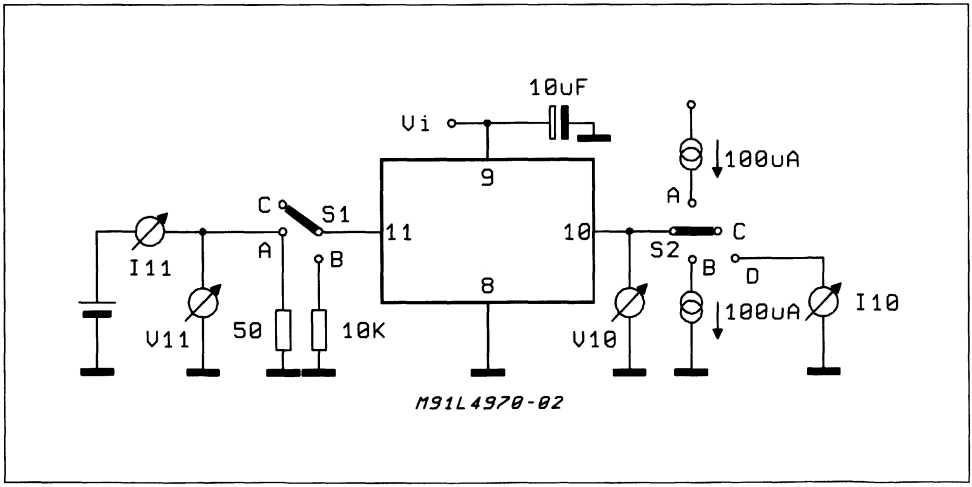


Figure 8: Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

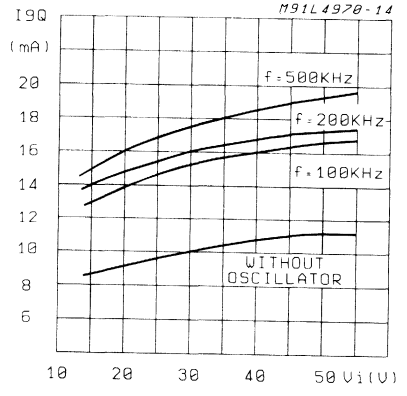


Figure 9: Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

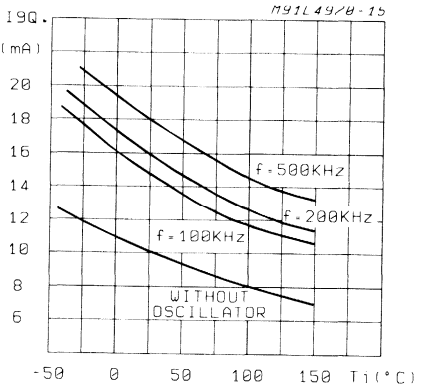


Figure 10: Quiescent Drain Current vs. Duty Cycle

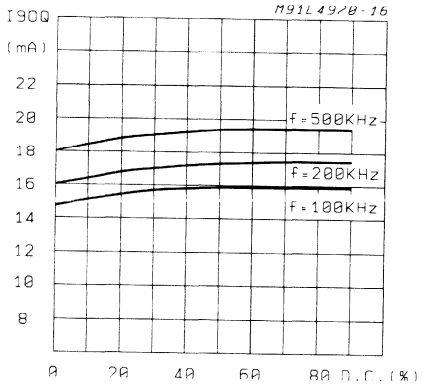


Figure 11: Reference Voltage (pin14) vs. V_i (see fig. 7)

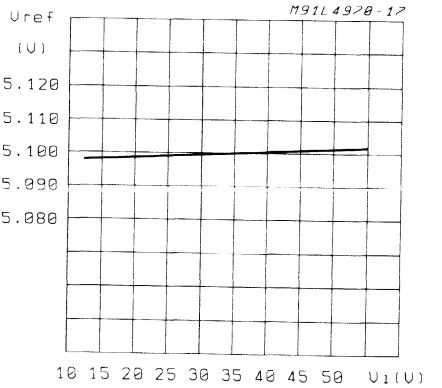


Figure 12: Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7)

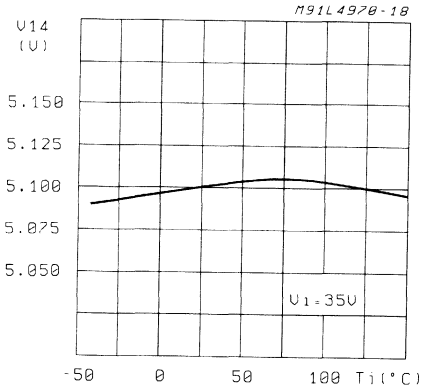


Figure 13: Reference Voltage (pin15) vs. V_i (see fig. 7)

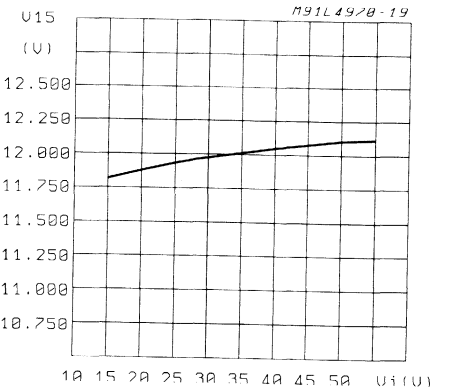


Figure 14: Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

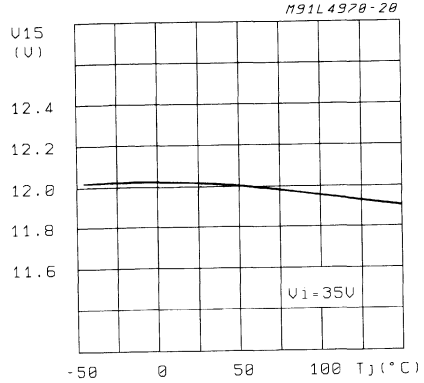


Figure 15: Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency

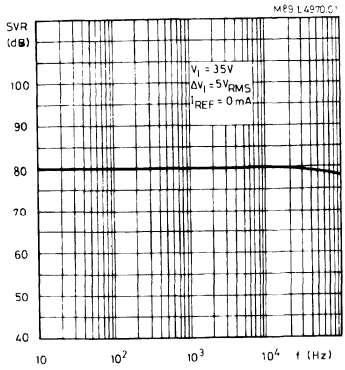


Figure 16: Switching Frequency vs. Input Voltage (see fig. 5)

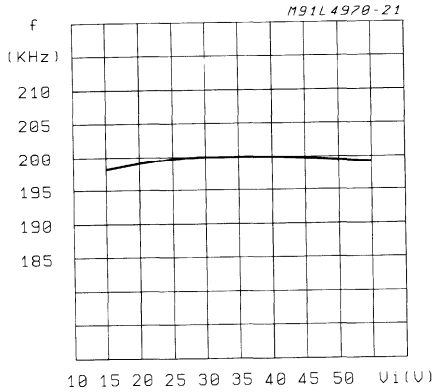


Figure 17: Switching Frequency vs. Junction Temperature (see fig 5)

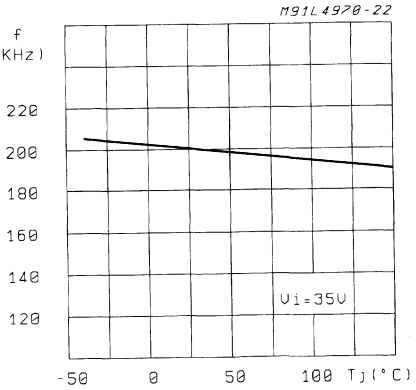


Figure 18: Switching Frequency vs. R4 (see fig. 5)

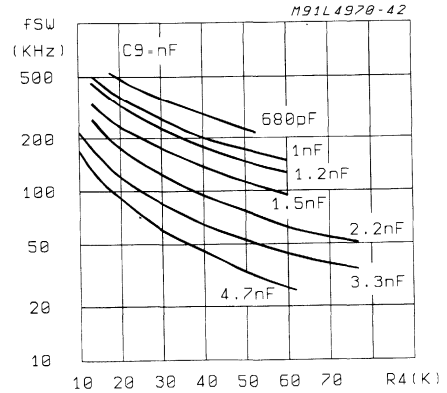


Figure 19: Max. Duty Cycle vs. Frequency

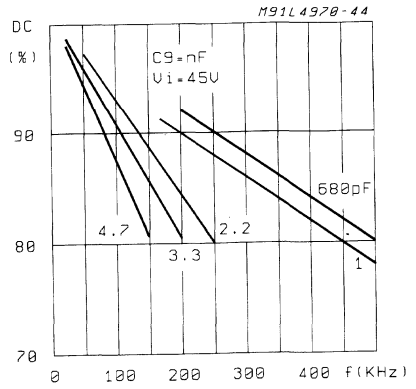


Figure 20: Supply Voltage Ripple Rejection vs. Frequency (see fig. 5)

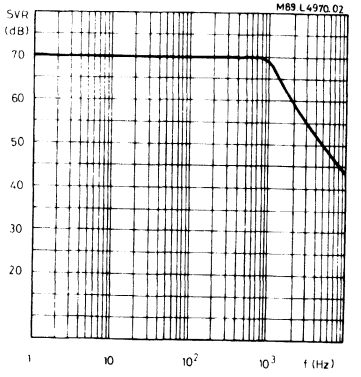


Figure 21: Line Transient Response (see fig. 5)

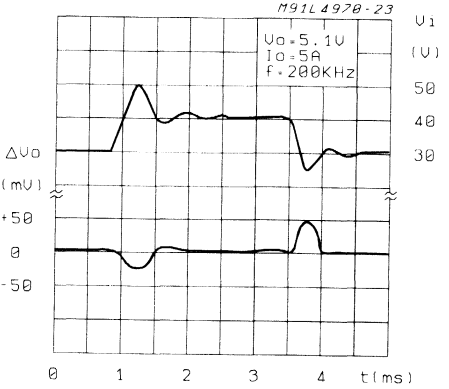


Figure 22: Load Transient Response (see fig. 5)

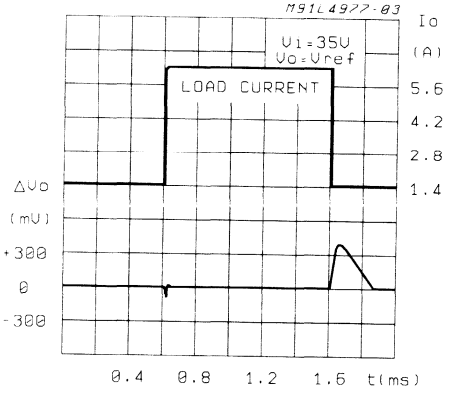


Figure 23: Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7

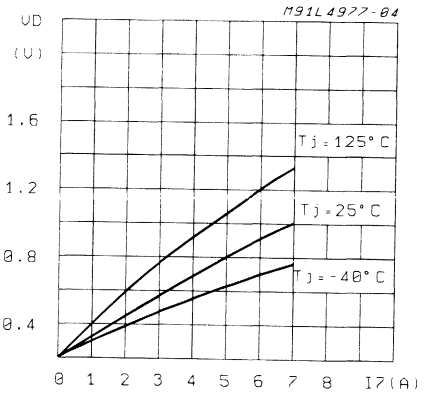


Figure 24: Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature

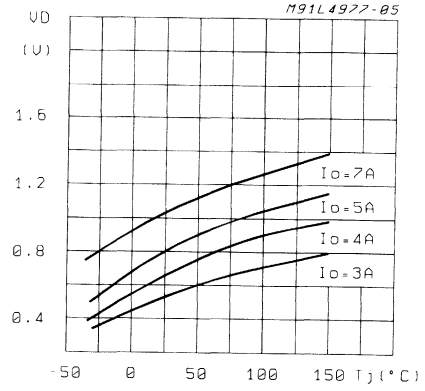


Figure 25: Power Dissipation (device only) vs. Input Voltage

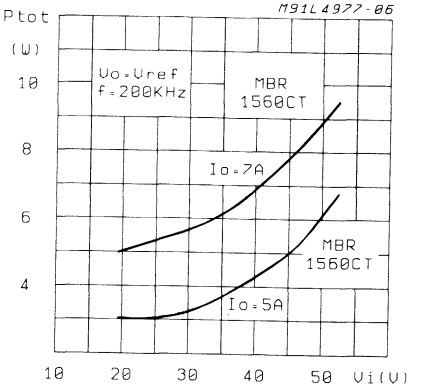


Figure 26: Power Dissipation (device only) vs. Output Voltage

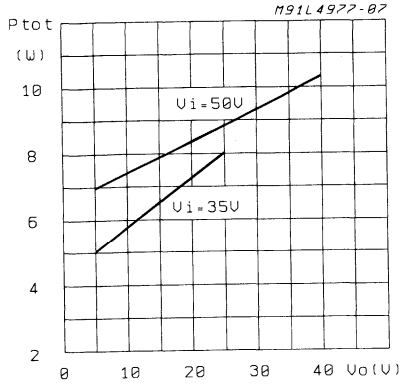


Figure 27: Heatsink Used to Derive the Device's Power Dissipation

$$R_{th}\text{ - Heatsink} = \frac{T_{case} - T_{amb}}{P_d}$$

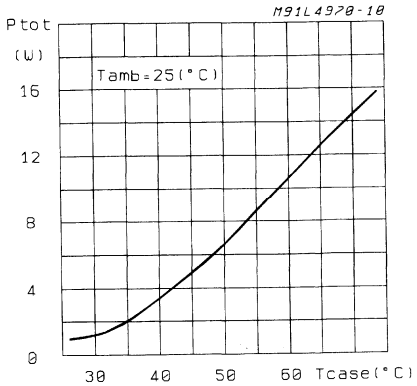


Figure 28: Efficiency vs. Output Current

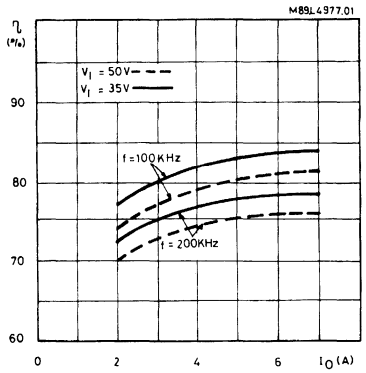


Figure 29: Efficiency vs. Output Voltage

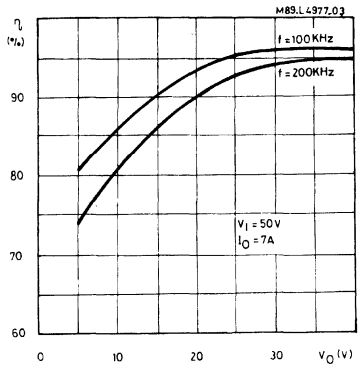


Figure 30: Efficiency vs. Output Voltage

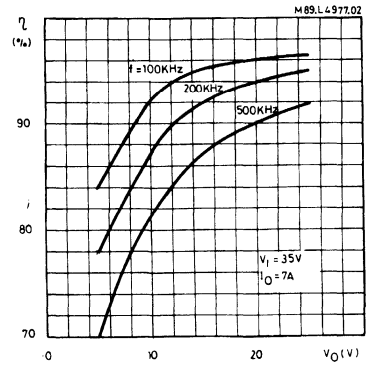


Figure 31: Open Loop Frequency and Phase Response of Error Amplifier (see fig.7C)

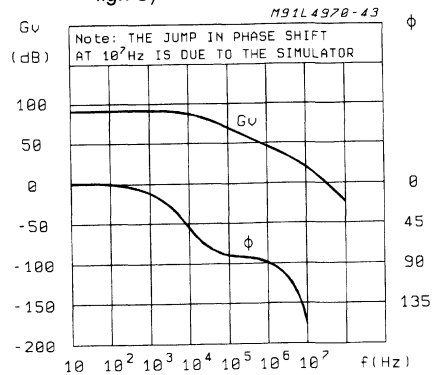


Figure 32: Power Dissipation Derating Curve

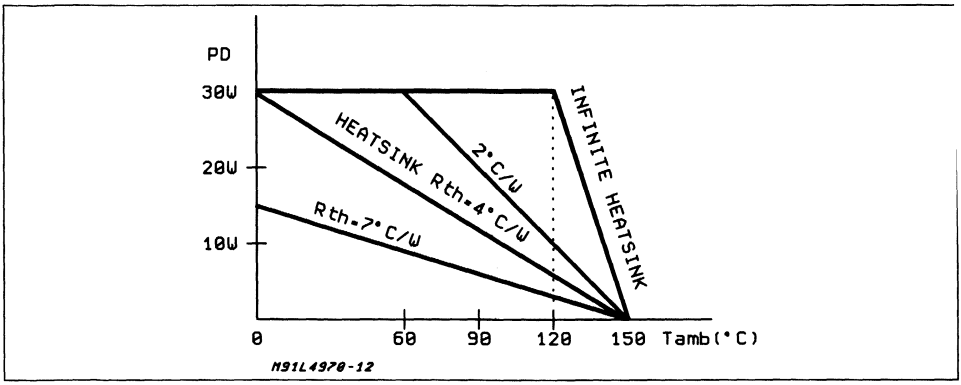


Figure 33: A5.1V/12V Multiple Supply. Note the Synchronization between the L4977A and the L4974A

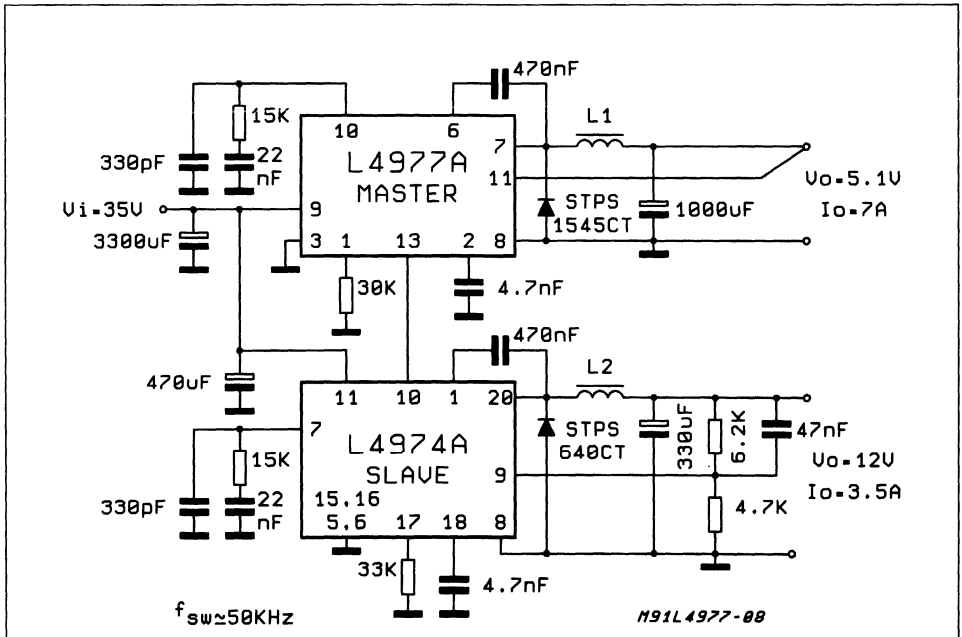


Figure 34: 5.1V / 7A Low Cost Application

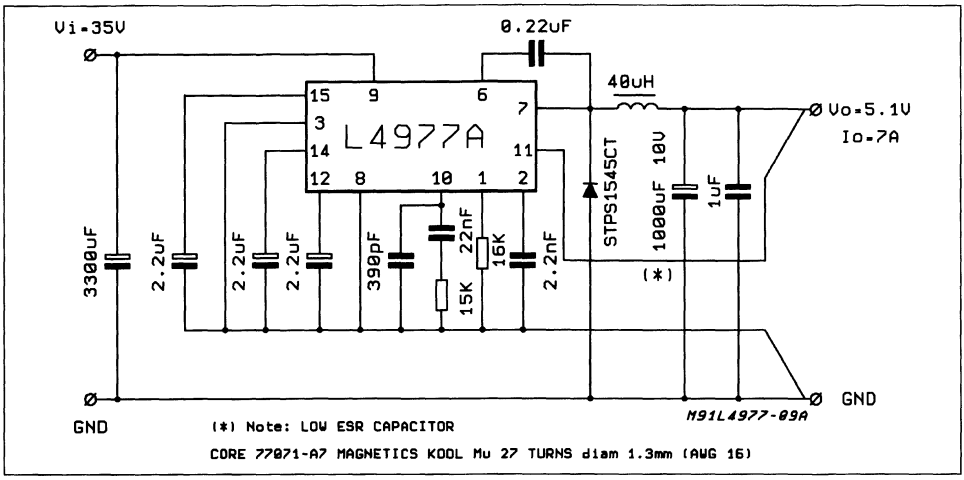


Figure 35: 7A Switching Regulator, Adjustable from 0V to 25V.

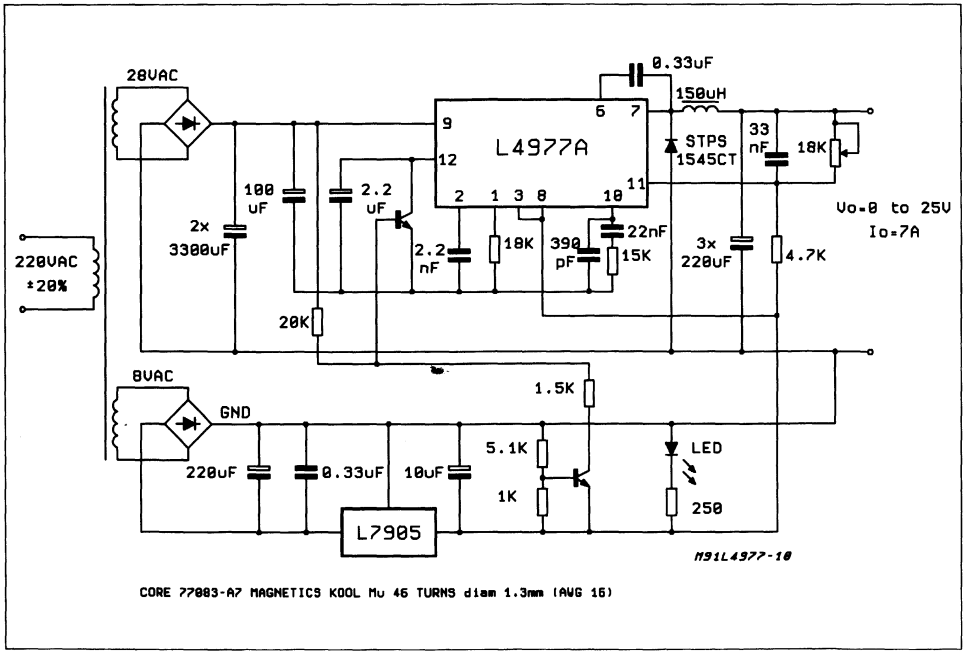
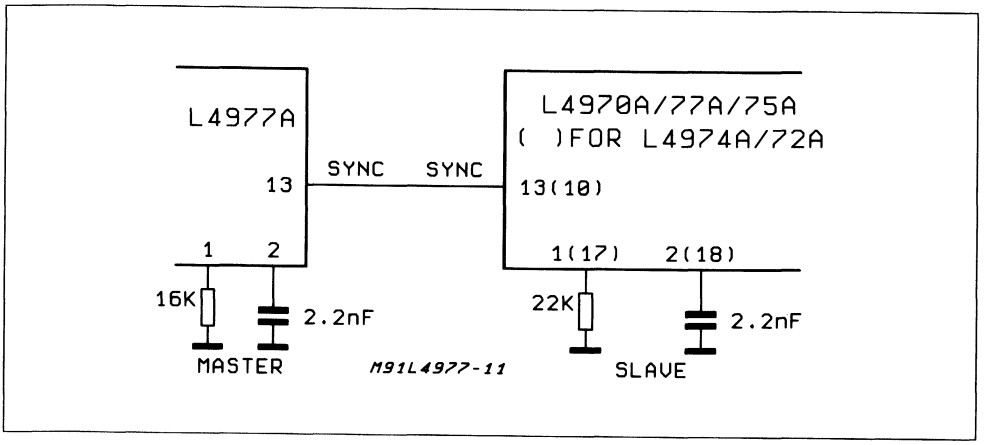


Figure 36: L4977A's Sync. Example



SGS-THOMSON MICROELECTRONICS

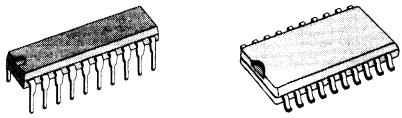
L4981A
L4981B

POWER FACTOR CORRECTOR

ADVANCE DATA

- CONTROL BOOST PWM UP TO 0.99P.F.
- LIMIT LINE CURRENT DISTORTION TO < 5%
- UNIVERSAL INPUT MAINS
- FEED FORWARD LINE AND LOAD REGULATION
- AVERAGE CURRENT MODE PWM FOR MINIMUM NOISE SENSITIVITY
- HIGH CURRENT BIPOLAR AND DMOS TOTEM POLE OUTPUT
- LOW START-UP CURRENT (0.5mATYP)
- UNDER VOLTAGE LOCKOUT WITH HYSTERESIS AND PROGRAMMABLE TURN ON THRESHOLD
- OVERVOLTAGE, OVERCURRENT PROTECTION
- PRECISE 2% ON CHIP REFERENCE EXTERNALLY AVAILABLE
- SOFT START

MULTIPOWER BCD TECHNOLOGY



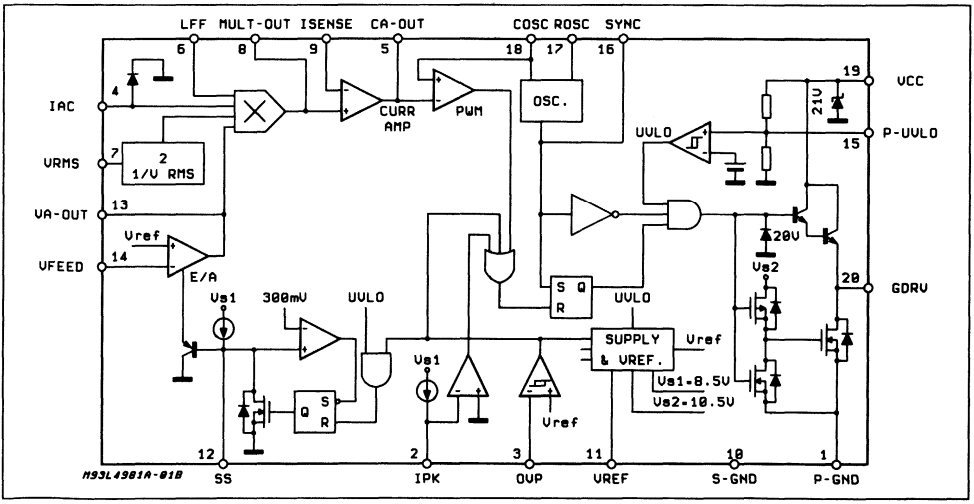
DIP 20 **SO20**

ORDERING NUMBERS: L4981X (DIP 20)
L4981XD (SO 20)

DESCRIPTION

The L4981 is provides the necessary features to achieve a very high power factor up to 0.99.
Realized in BCD 60II technology this power factor corrector (PFC) pre-regulator contains all the control functions for designing a high efficiency-mode power supply with sinusoidal line current consumption.
The L4981can be easily used in systems with mains voltages between 85V to 265V without any line switch. This new PFC offers the possibility to work at fixed frequency (L4981A) or modulated frequency (L4981B) optimizing the size of the in-

BLOCK DIAGRAM

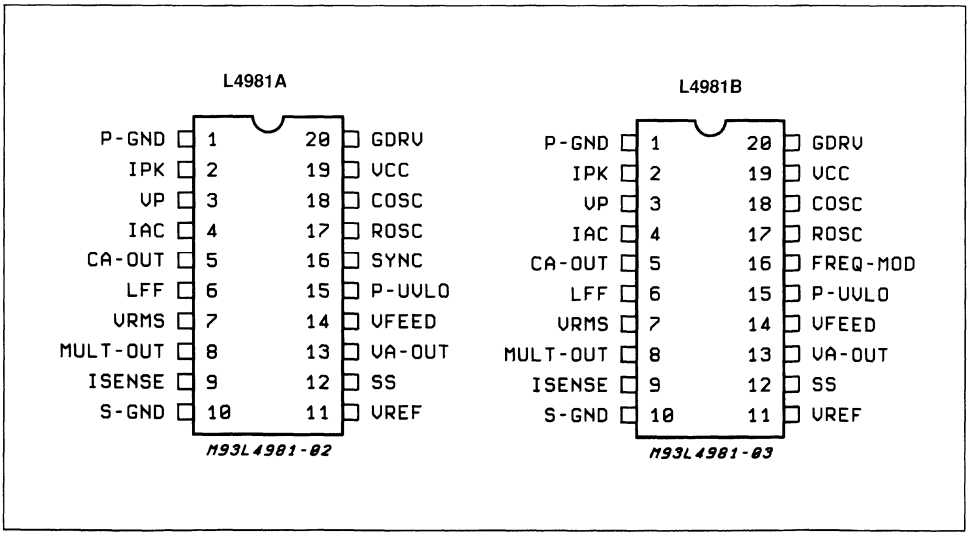


put filter; both the operating frequency modes working with an average current mode PWM controller, maintaining sinusoidal line current without slope compensation.
Besides power MOSFET gate driver, precise voltage reference (externally available), error amplifier, undervoltage lockout, current sense and the soft start are included. To limit the number of the external components, the device integrates protections as overcurrent and overvoltage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_{CC}	19	Supply Voltage (low impedance)	21	V
		Supply Voltage (I_{CC} ≤50mA)	selflimit	V
I_{GDRV}	20	Gate driv. output peak current (t = 1µs)	2	A
		Gate driv. output energy (C = 1µF)	40	µJ
V_{GDRV}		Gate driv. output voltage t = 0.1µs	-1	V
		Votages at pins 3, 14, 7, 6, 12, 15	-0.3 to 9	V
V_{VA-OUT}	13	Error Amplifier Voltage (Isource =-10mA; Isink = 20mA	-0.3 to 8.5	V
I_{AC}	4	AC Input Current	5	mA
		Voltages at pin 8, 9	-0.5 to 7	V
V_{CA-OUT}	5	Current Amplifier Volt. (Isource = -20mA; Isink = 20mA	-0.3 to 8.5	V
V_{ROSC}	17	Voltage at pin 17	-0.3 to 3	V
	11, 18	Voltage at pin 11, 18	-0.3 to 7	V
I_{COSC}	18	Input Sink Current	15	mA
$I_{FREQ-MOD}$	16	Frequency Mode Sink Current (L4981B)	5	mA
I_{COSC}	18	Input Sink Current	15	mA
V_{SYNC}	16	Sink Voltage (L4981A)	-0.3 to 7	V
V_{IPK}	2	Voltage at pin 2 Voltage at Pin 2 t = 1µs	-0.3 to 5.5 -2	V V
P_{tot}		Power Dissipation at T_{amb} = 25°C (DIP20)	1.5	W
		Power Dissipation at T_{amb} = 25°C (SO20)	1	W
T_j, T_{stg}		Junction and StorageTemperature	-40 to 150	°C

PIN CONNECTIONS (Top views)



THERMAL DATA

Symbol	Parameter	DIP 20	SO 20	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	80	120	°C/W

PIN FUNCTIONS

N.	Name	Description
1	P-GND	Power ground.
2	IPK	Peak Current limiting. An external resistor connected from pin 2 to the sense resistor allows to program the peak current limiting.
3	VP	Overvoltage protection. At this input is compared an internal precise 5.1 (typ) voltage reference with a sample of the boost output voltage obtained via a resistive voltage divider in order to limit the maximum output peak voltage.
4	IAC	Input for the AC current. An input current proportional to the rectifier mains voltage generates, via a multiplier, the current reference for the current amplifier.
5	CA-OUT	Current amplifier output. An external RC network determinates the loop gain.
6	LFF	Load feedforward; this voltage input pin allows to modify the multiplier output current proportionally to the load, in order to give a faster response versus load transient. The best control is obtained working between 1.5V and 5.3V. If this function is not used connect this pin to the voltage reference (pin = 11).
7	VRMS	Input for proportional RMS line voltage. the VRMS input compesates the line voltage changes. Connecting a low pass filter between the rectified line and the pin 7, a DC voltage proportional to the input line RMS voltage is obtained. The best control is reached using input voltage between 1.5V and 6.5V. If this function is not used connect this pin to the voltage reference (pin = 11).
8	MULT-OUT	Multiplier output. This pin common to the multiplier output and the current amplifier N.I. input is an high impedence input like I_{SENSE}. Configuring the current amplifier as differential amplifier a small current distortion is obtained even near zero crossing line voltage. The MULT-OUT pin must be taken not below -0.5V.
9	I_{SENSE}	Current amplifier inverting input. Care must be taken to avoid this pin goes down -0.5V.
10	S-GND	Signal ground.
11	V_{REF}	Output reference voltage (typ = 5.1V).Voltage refence at ± 2% of accuracy externally available, it's internally current limited and can deliver an output current up to 10mA.
12	SS	A capacitor connected to ground defines the soft start time. An internal current generator delivering 100µA (typ) charges the external capacitor defining the soft start time constant. An internal MOS discharge, the external soft start capacitor both in overvoltage and UVLO conditions.
13	VA-OUT	Error amplifier output, an RC network fixes the voltage loop gain characteristics.
14	VFEED	Voltage error amplifier inverting input. This feedback input is connected via a voltage divider to the boost output voltage.
15	P-UVLO	Programmable under voltage lock out threshold input. A voltage divider between supply voltage and GND can be connected in order to program the turn on threshold.
16	SYNC (L4981A)	This synchronization input/output pin is CMOS logic compatible. Operating as SYNC in, a rectangular wave must be applied at this pin. Opearting as SYNC out, a rectangular clock pulse train is available to synchronize other devices.
	FREQ-MOD (L4981B)	Frequency modulation current input. An external resistor must be connected between pin 16 and the rectified line voltage in order to modulate the oscillator frequency. Connecting pin 16 to ground a fixed frequency imposed by R_{OSC} and C_{OSC} is obtained.
17	R_{OSC}	An external resistor connected to to ground fixes the constant charging current of C_{OSC}.
18	C_{OSC}	An external capacitor connected to GND fixes the switching frequency.
19	V_{CC}	Supply input voltage.
20	GDRV	Output gate driver. Bipolar and DMOS transistors totem pole output stage can deliver peak current in excess 1A useful to drive MOSFET or IGBT power stages.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified V_{CC} = 18V, C_{OSC} = 1nF, R_{OSC} = 24KΩ, C_{SS} = 1µF, $V_{CA\text{-}OUT}$ = 3.5V, V_{ISENSE} = 0V, V_{LFF} = V_{REF}, I_{AC} = 100µA, V_{RMS} = 1V, V_{FEED} = GND, V_{IPK} = 1V, V_P = 1V, T_J = 25°C

Symbol	Prameter	Test Condition	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER SECTION						
V_{IO}	Input Offset Voltage				8	mV
I_{IB}	Input Bias Current	V_{FEED} = 0V	-500	-50	500	nA
	Open Loop Gain	1V ≤ $V_{VA\ OUT}$ ≤ 5V	70	100		dB
SVR	Supply Voltage Rejection	11V ≤ V_{CC} ≤ 19.5V	70	90		dB
V_{OH}	Output High voltage	V_{FEED} = 4.7V $I_{VA\text{-}OUT}$ = -0.5mA	5.5		7.5	V
V_{OL}	Output Low Voltage	V_{FEED} = 5.5V $I_{VA\text{-}OUT}$ = 0.5mA			1	V
I_{OS}	Output Source Current	V_{FEED} = 4.7V; $V_{VA\text{-}OUT}$ = 3.5V	-2	-10		mA
I_{OS}	Output Sink Current	V_{FEED} = 5.5V; $V_{VA\text{-}OUT}$ = 3.5V	2	10		mA
	Unit Gain Bandwidth			1		MHz
REFERENCE SECTION						
V_{ref}	Reference Output Voltage	T_j = 25°C I_{ref} = 0	5	5.1	5.2	V
	Load Regulation	1mA ≤ I_{ref} ≤ 10mA		3	25	mV
	Line Regulation	11V ≤ V_{CC} ≤ 19.5V		3	25	mV
	Temperature Stability			0.4		mV/C
	Short Circuit Current	V_{ref} = 0V		30		mA
OSCILLATOR SECTION						
	Initial Accuracy	T_j = 25°C	84	100	116	KHz
	Voltage Stability	11V ≤ V_{CC} ≤ 19.5V		0.5		%
	Temperature Stability	T_{min} ≤ T_{amb} ≤ T_{max}		2		%
	Ramp Valley to Peak		4.7	5	5.3	V
	Charge Current	V_{COSC} = 3.5V	0.45	0.55	0.65	mA
	Discharge Current	V_{COSC} = 3.5V		11.5		mA
	Ramp Valley Voltage		0.9	1.2	1.4	V
SYNC SECTION (Only for **L4981A**)						
	Output Pulse Width			0.6		µs
	Low Input Voltage				0.9	V
	High Input Voltage		3.5			V
	Pulse for Synchronization		300			ns
	Sink Current with Low Output Voltage	V_{SYNC} = 0.4V V_{COSC} = 0V	0.4			mA
	Source Current with High Output Voltage	V_{SYNC} = 4.6V V_{COSC} = 6.7V	-0.5			mA
FREQUENCY MODULATION FUNCTION (Only for **L4981B**)						
	Minimum Oscillator Frequency	$I_{FREQ\text{-}MOD}$ = 360µA (Pin 16) V_{VRMS} = 4V (Pin 7)	62	74	84	KHz
		$I_{FREQ\text{-}MOD}$ = 180µA (Pin 16) V_{VRMS} = 2V (Pin 7)	64	76	86	KHz
	Maximum Oscillation Frequency	$V_{FREQ\text{-}MOD}$ = 0V (Pin 16)	84	100	116	KHz
SOFT START SECTION						
	Soft Start Source Current	V_{SS} = 3V	60	100	140	µA
	Output Saturation Voltage	V_P = 6V, I_{SS} = 2mA			0.25	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OVER VOLTAGE PROTECTION COMPARATOR						
	Rising Threshold Voltage			5.1		V
	Hysteresis		180	250	320	mV
	Input Bias Current			0.05	1	µA
	Propagation delay to output	ΔV_{IN} = 100mV		300	1500	ns
OVER CURRENT PROTECTION COMPARATOR						
	Input Current	V_{IPK} = -0.1V	-200	-100		µA
	Propagation delay to Output			180	900	ns
CURRENT AMPLIFIER SECTION						
	Input Offset Voltage				2	mV
	Input Bias Current		-500	50	500	nA
	Open Loop Gain	1.1V ≤ $V_{CA\ OUT}$ ≤ 6V	70	100		dB
SVR	Supply Voltage Rejection	11V ≤ V_{CC} ≤ 19.5V	70	90		dB
	Output High Voltage	$V_{MULT\ OUT}$ = 200mV $I_{CA\ OUT}$ = -0.5mA, V_{IAC} = 0V	6.2			V
	Output Low Voltage	$V_{MULT\ OUT}$ = -200mV $I_{CA\ OUT}$ = 0.5mA, V_{IAC} = 0V			0.9	V
	Output Source Current	$V_{MULT\ OUT}$ = 200mV, V_{IAC} = 0V	-2	-10		mA
	Output Sink Current	$V_{MULT\ OUT}$ = -200mV	2	10		mA
	Voltage Output Range	No Load	0.8		6.5	V
	Unity Gain Bandwidth			1		MHz
OUTPUT SECTION (Pin 20)						
	Output Voltage Low	I_{SINK} = 250mA			0.8	V
	Output Voltage High	I_{SOURCE} = 250mA V_{CC} = 15V	11.5	12.5		V
	Output Voltage Rise Time	C_{OUT} = 1nF		50	150	ns
	Output Voltage Fall Time	C_{OUT} = 1nF		30	100	ns
TOTAL STANDBY CURRENT SECTION						
	Supply Current	before start up, V_{CC} = 14V		0.5	1	mA
	Operating Quiescent Current	V_{IPK} = 0.2V Pin 20 = open		8	12	mA
	V_{CC} Zener Voltage	I_{CC} = 50mA	20	23	25	V
UNDER VOLTAGE LOCKOUT SECTION						
	Turn on Threshold		14	15.5	17	V
	Turn off Threshold		9	10	11	V
	Programmable Threshold		1.18	1.28	1.38	V
LOAD FEED FORWARD						
I_{LFF}	Bias Current	V_6 = 1.6V		100		µA
		V_6 = 5.3V		200		µA
V_I	Input Voltage Range		1.6		5.3	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Prameter	Test Condition	Min.	Typ.	Max.	Unit
MULTIPLIER SECTION						
	Multipler Output Current	V_{CA-OUT} = 4V, V_{RMS} = 2V, $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 50µA, C_{OSC} = 0V	20	35	52	µA
		V_{CA-OUT} = 4V, V_{RMS} = 2V, $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 200µA, C_{OSC} = 0V	100	135	170	µA
		V_{CA-OUT} = 2V, V_{RMS} = 2V, $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 100µA, C_{OSC} = 0V	10	20	30	µA
		V_{CA-OUT} = 2V, V_{RMS} = 4V, $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 100µA, C_{OSC} = 0V	2	5.5	11	µA
		V_{CA-OUT} = 4V, V_{RMS} = 4V, $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 100µA, C_{OSC} = 0V	10	22	34	µA
		V_{CA-OUT} = 4V, V_{RMS} = 2V, $V_{MULTOUT}$ = 0, V_{LFF} = 2.5V C_{OSC} = 0V, I_{AC} = 200µA	20	37	54	µA
		V_{CA-OUT} = 4V, V_{RMS} = 4V $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 200µA, C_{OSC} = 0V	20	39	54	µA
		V_{CA-OUT} = 2V, V_{RMS} = 4V, $V_{MULTOUT}$ = 0, V_{LFF} = 5.1V I_{AC} = 0, C_{OSC} = 0V	-2	0	2	µA
K	Multiplier Gain			0.37		

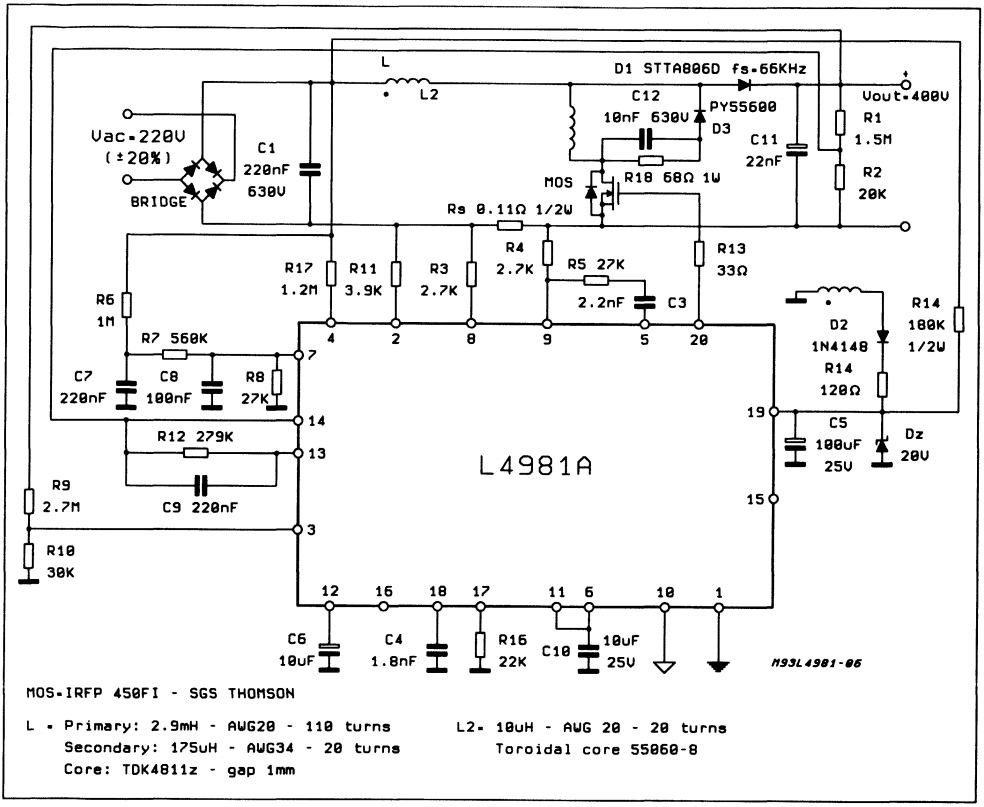
$$I_{MULT-OUT} = K \cdot I_{AC} \frac{(V_{A-OUT} - 1.28) \cdot (0.8 + V_{LFF} - 1.28)}{(V_{RMS})^2}$$

if $V_{LFF} = V_{REF}$

$$I_{MULT-OUT} = I_{AC} \frac{(V_{A-OUT} - 1.28)}{(V_{RMS})^2} \cdot K1$$

where:
K1 = 1V

Figure 3: L4981A Power Factor Corrector (200W)



SGS-THOMSON MICROELECTRONICS

L6560

POWER FACTOR CORRECTOR

ADVANCE DATA

- VERY PRECISE ADJUSTABLE INTERNAL OUTPUT OVERVOLTAGE PROTECTION
- HYSTERETIC START-UP ($I_{START-UP}$ < 0.5mA)
- VERY LOW QUIESCENT CURRENT (< 3.5mA)
- INTERNAL START-UP TIMER
- TRANSITION MODE OPERATING
- TOTEM POLE OUTPUT: ±400mA
- DIP8/SO8 PACKAGES

MULTIPOWER BCD TECHNOLOGY

MINIDIP **SO 8**

ORDERING NUMBER: L6560

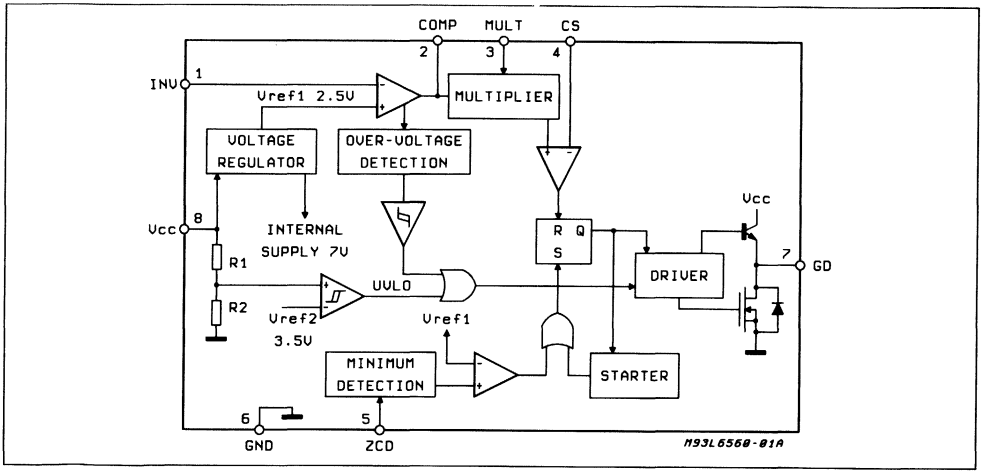
DESCRIPTION

The L6560 is a monolithic integrated circuit in Minidip package, designed as a controller and driver of a discrete power transistor for the implementation of active power factor correction, for sinusoidal line current consumption.

Realized in mixed BCD technology, the chip integrates:

- An undervoltage lockout with micropower start-up and hysteresis
- An internal temperature compensated band gap reference
- A stable error amplifier
- One quadrant multiplier
- Current sense comparator
- An output overvoltage protection circuit
- A totem-pole output stage able to drive a POWER MOS or IGBT devices with source and sink current of 400mA. The chip works in transition mode and is particularly intended for lamp ballast applications and for low power SMPS

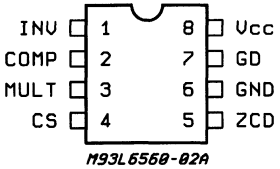
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	Supply Voltage (low impedance)	20	V
		Supply Voltage (I_{CC} ≤20mA)	selflimit	V
I_{GD}	7	Output Totem Pole Current	±700	mA
E	7	Output Energy on Capacitive Load	4	µJ
INV, COMP MULT	1, 2, 3	Analog Inputs & Outputs	-0.3 to 7	V
CS	4	Current Sense Input	-0.3 to 7	V
ZCd	5	Zero Current Detector	1 (source) 4 (sink)	mA mA
P_{tot}		Power Dissipation @T_{amb} = 50 °C (Minidip)	0.75	W
T_j		Junction Temperature Operating Range	-25 to 125	°C
T_{stg}		Storage Temperature	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	SO 8	MINIDIP	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	150	100	°C/W

PIN FUNCTIONS

N.	Name	Function
1	INV	Inverting input of the error amplifier. A resistive divider is connected between output regulated voltage and this point, to provide the voltage feedback.
2	COMP	Output of error amplifier. A feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input the multipler stage. A resistive divider connects to this pin the rectified mains. A voltage signal, proportional to the rectified mains, appears on this pin.
4	CS	Input to the comparator of the control loop. The current is sended by a resistor and the resulting voltage is applied to this pin.
5	ZCD	Zero current detection input.
6	GND	Ground of the control section.
7	GD	Gate driver output. A push pull output stage is able to drive the Power MOS with peak current of 400mA (source and sink).
8	V_{CC}	Supply voltage of driver and control circuits.

ELECTRICAL CHARACTERISTICS (V_{CC} = 13V; T_j = 0 to 70°C unless otherwise specified)

SUPPLY VOLTAGE SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	8	Operating Range	after turn-on	9.5		20	V
V_{ref1}		Int. Precision Reference		2.45	2.5	2.55	V
V_{ref2} [1]		Int. Precision Reference			3.5		V
V_{CCth}	8	Turn-on Threshold		14	15	16	V
Hys	8	Hysteresis		4.5	5	5.5	V

SUPPLY CURRENT SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ST}	8	Start-up Current	before turn-on		0.3	0.5	mA
I_{CC}	8	Operating Supply Current	no load		2.5	3.5	mA
			C_L = 1nF @ 70KHz		4	5	mA
V_{IZ}	8	Zener Voltage	I_{CC} = 15mA	25	27	30	V

ERROR AMPLIFIER SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INV}	1	Voltage Feedback Input Threshold		2.45	2.5	2.55	V
T_S		Temperature Stability	Tamb = -25 to 85°C		1		%
R_L		Line Regulation	V_{CC} = 12 to 18V		1	10	mV
I_{INV}	1	Input Bias Current			0.1	1	µA
G_V		Voltage Gain	Open loop	60	80		dB
V_{COMP}	2	Output Voltage	I_{COMP}: source = 0.2mA		5		V
			I_{COMP}: sink = 0.5mA		2		V
I_{COMP}	2	Source Current		0.15	0.2		mA
		Sink Current		0.5	1		mA
		Gain Product bandwidth			1		MHz

MULTIPLIER SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
M_1	3	Mult Operating Voltage		0		4.6	V
M_2	2	Comp Operating Input Voltage Range		V_{REF2}	-	V_{REF2}+2	V
K		Multiplier Gain			0.6		1/V

CURRENT SENSE COMPARATOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CS}	4	Input Voltage Range		0		1.8	V
I_{CS}	4	Input Bias Current				50	nA
		Input Offset Voltage				15	mV
tdcs	4	Delay to Output (td_{L-H})			200		ns

NOTE[1]: Not tested, guaranteed by design

ELECTRICAL CHARACTERISTICS (continued)

ZERO CURRENT DETECTOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ZCD}	5	Operative Voltage		0.7		5.1	V
t_{dZCD}	4	delay to output (td_{L-H})			200		ns
V_{ZCD}	5	Input Threshol Voltage		1.3		1.8	V
		Hysteresis			0.5		V
V_{ZCD}	5	Clamp Voltage	I_{ZCD} = 3mA		5.1		V
V_{ZCD}	5	Clamp Voltage	I_{ZCD} = –3mA		0.7		V

OUTPUT SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{GD}	7	Output Voltage High	$I_{GDsource}$ = 100mA	11.8			V
			$I_{GDsource}$ = 20mA	12			V
		Output Voltage Low	I_{GDsink} = 100mA			0.5	V
			I_{GDsink} = 20mA			0.2	V
t_r	7	Output Voltage Rise Time	CL = 1nF		50		ns
t_f	7	Output Voltage Fall Time	CL = 1nF		40		ns

OUTPUT OVERVOLTAGE SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{OVP}	2	OVP Triggering Current			40		µA

OVER VOLTAGE PROTECTION OVP

The output voltage is expected to be kept by the operation of the PFC circuits close to its reference value that is set by the ratio of the two external resistors R_1 and R_2, taking into consideration that the non inverting input of the error amplifier is biased inside the L6560 at 2.5V.

In steady state conditions, the current through R1 and R2 is:

$$I_{SC} = \frac{V_{outsc} - 2.5}{R1}$$

$$\text{or } I_{SC} = \frac{2.5}{R2}$$

and, if the external compensation network is made only with a capacitor C, the current through C is equal zero.

When the output voltage increases the current through R1 becomes:

$$I_{R1} = \frac{V_{out} - 2.5}{R1}$$

$$I_{R1} = \frac{V_{outsc} + \Delta V_{OUT} - 2.5}{R1} = I_{sc} + \Delta I.$$

Since the current through R2 doesn't change, the ΔI current must flow through the capacitor C and enter in the error amplifier.

This current is mirrored inside the L6560, and compared with a precise internal reference of 40µA. Whenever such 40µA limit is exceed, the OVP protection is triggered, and the external power transistor is switched off, until the overvoltage situation disappears.

The OVP value is threfore set by the equation OVP = ΔVout = $R_1 \bullet 40\mu A$.

Typical values for R_1, R_2 and C are reported in the application circuit. The overvoltage can be set independently from the average output voltage. The precision in setting the overvoltage threshold is 7% of the overvoltage value (for instance ΔV = 60V ± 4.2V).

The average output voltage in the L6560 can be set with a precision of for instance at 400V ± 8V.

Figure 2: Overvoltage Protection Circuit

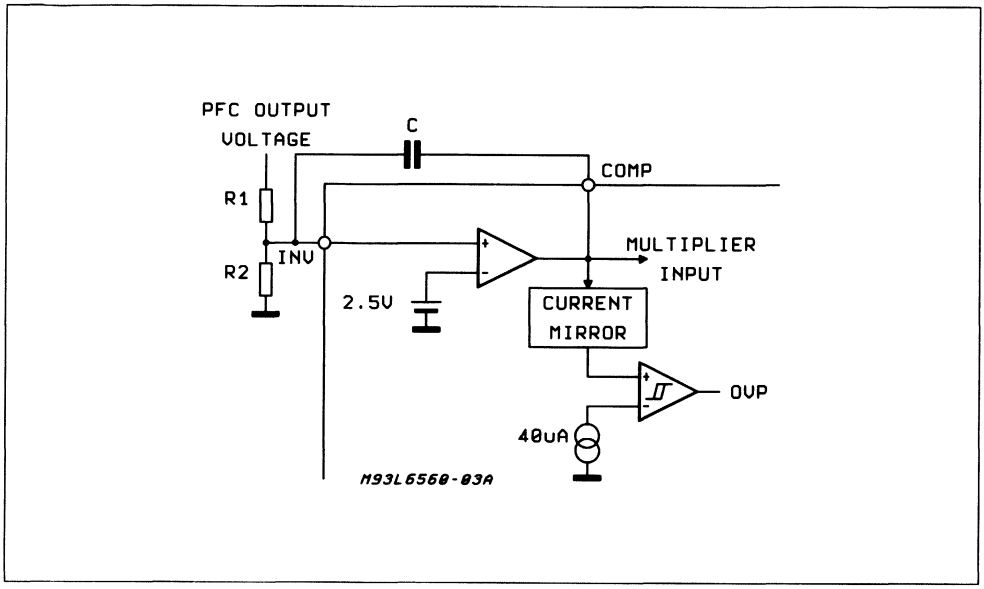
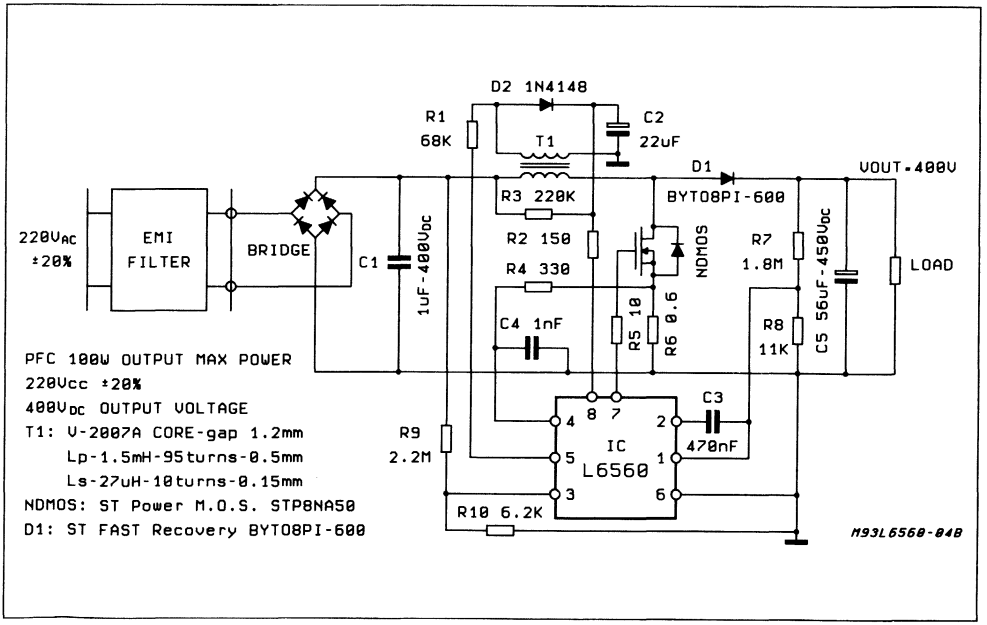


Figure 3: Application Circuit (100W)



APPLICATION NOTES

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

EASY APPLICATION DESIGN WITH THE L4970A, MONOLITHIC DC-DC CONVERTERS FAMILY

by G. Gattavari and C. Diazzi

The L497XA series of high current switching regulator ICs exploit Multipower-BCD technology to achieve very high output currents with low power dissipation – up to 10A in the Multiwatt power package and 3.5A in a DIP package .

THE TECHNOLOGY

The technology architecture is based on the vertical DMOS silicon gate process that allows a channel length of 1.5 micron ; using a junction isolation technique it has been possible to mix on the same chip Bipolar and CMOS transistors along with the DMOS power components (Fig. 2). Figure 1 shows how this process brings a rapid increase in power IC complexity compared to conventional bipolar technology.

In the 70's class B circuits and DC circuits allowed output power in the range of 70W. By 1980, with the introduction of switching techniques in power ICs, output powers up to 200W were reached ; with BCD technology the output power increased up to 400W.

Figure 1: BCD process and increase in power ICs complexity.

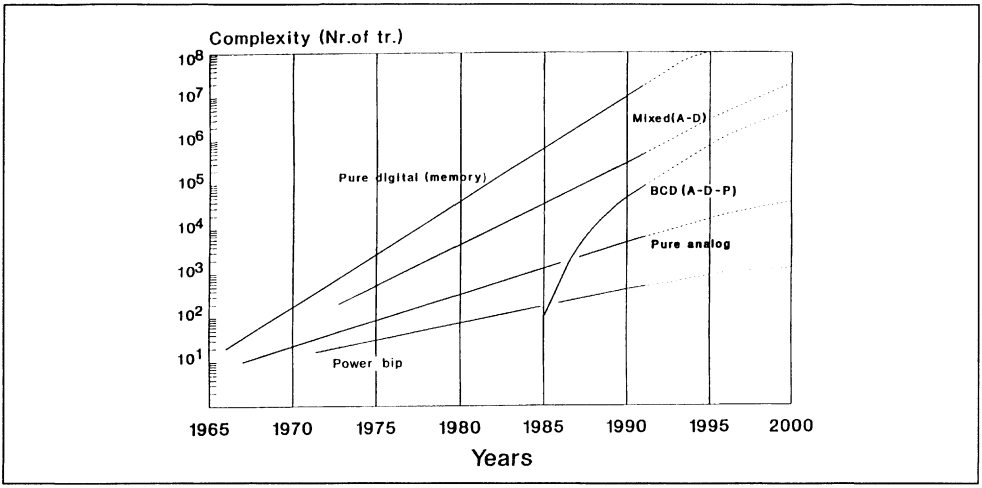
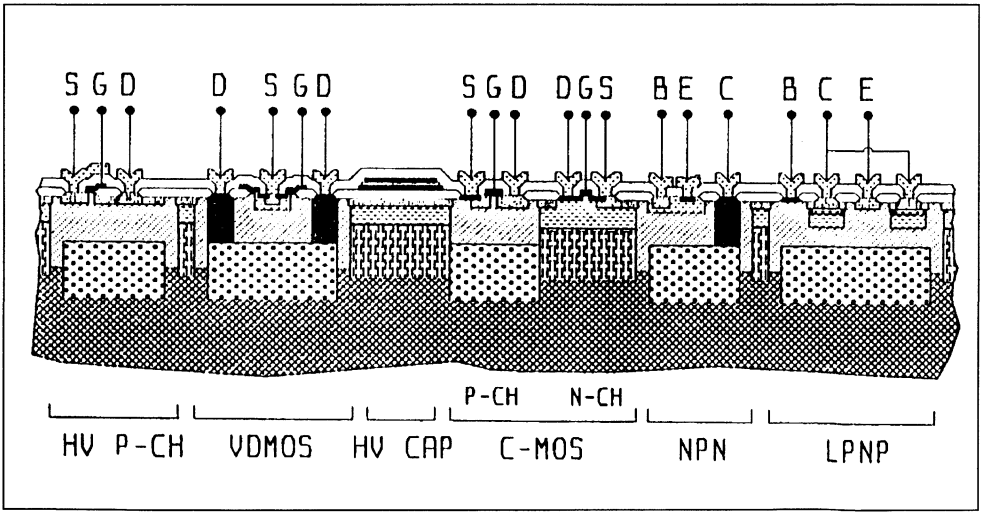


Figure 2: Cross Section of the BCD Mixed Technology.



THE STEP-DOWN CONFIGURATION

Fig. 3 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows : Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component super-imposed on it, ΔI_L, due to the voltage across L.

Figure 3: The Basic Step-down Switching Regulator Configuration

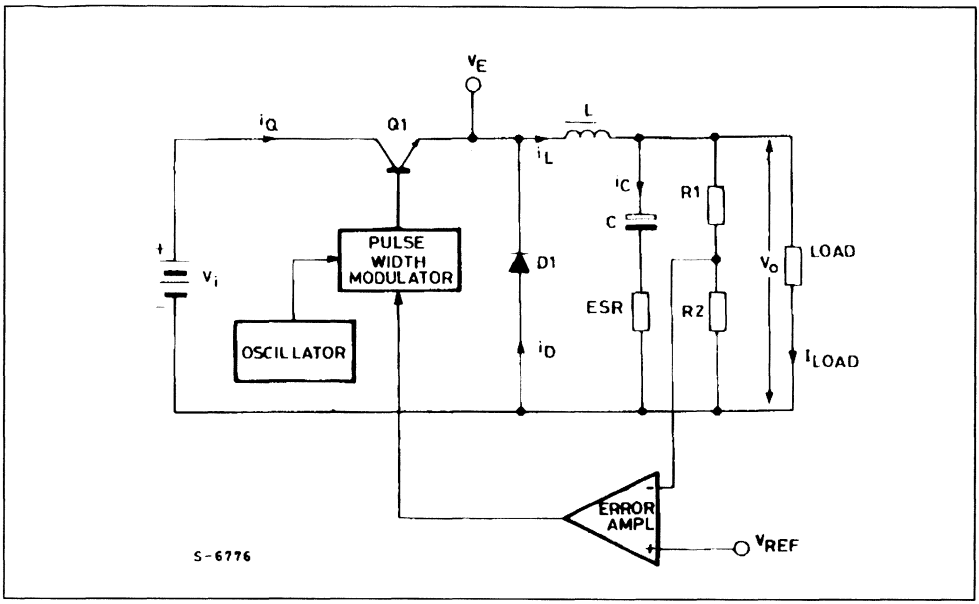


Fig. 4 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode era taken into account.

The ON and OFF times are established by the following expression :

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 4b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 4c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in Fig. 4e. In balanced conditions the ΔI_L^+ current increase occuring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula :

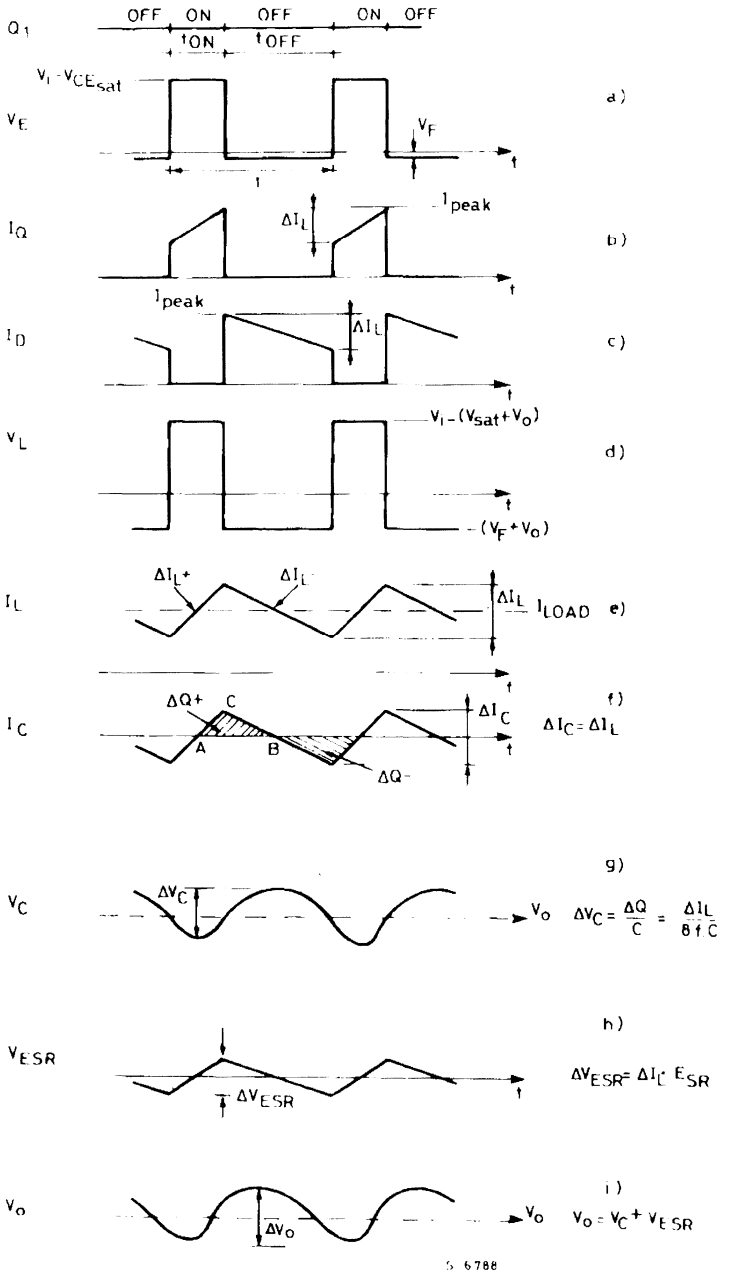
$$\Delta i_L^+ = \Delta i_L^- = \frac{(V_i - V_{sat}) - V_O}{L} T_{ON} = \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect to $I_{OMIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 4d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 4f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.
This ripple consists of two components : a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Fig. 4g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in Fig. 4f :

Figure 4: Principal Circuit Waveforms of the figure 1 Circuit.



$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

Which therefore gives:

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 4h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is V_{ESR} (t) = i_C (t) · ESR. Fig. 4i shows the overall ripple V_o, which is the sum of the two previous components. As the frequency increases (> 20kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in Fig. 4 into account.

Starting from the initial conditions, where Q = ON, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression :

$V_i = v_L + v_C$ (V_{sat} is neglected against V_i).

$$V_i = L \frac{dI_L}{dt} + v_C = L \frac{dI_L}{dt} + V_o \quad (1)$$

which gives :

$$\frac{dI_L}{dt} = \frac{(V_i - V_o)}{L} \quad (2)$$

The current through the inductance is given by :

$$I_L = \frac{(V_i - V_o)}{L} \quad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that :

$$\Delta I_L^+ = \frac{(V_i - V_o)\, T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot very instantaneously, the voltage across the ased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present :

$v_C(t) = V_o$, i_L (t) = i_D (t) = I_{peak}

And the equation associated to the following loop may be written :

$$V_F + L \frac{dI_L}{dt} + v_C = 0 \quad (5)$$

where:

$v_C = V_o$

$$\frac{dI_L}{dt} = -(V_F + V_o) / L \quad (6)$$

It follows therefore that :

$$i_L (t) = -\frac{V_F + V_o}{T} t \quad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs :

$$I_L = \frac{V_o}{L} t \quad (8)$$

therefore :

$$\Delta I_L^+ = \frac{V_o}{L} T_{OFF} \quad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$ if follows that :

$$\frac{(V_i - V_o)\, T_{ON}}{L} = \frac{V_o\, T_{OFF}}{L}$$

which allows us to calculate V_o :

$$V_o = V_i \frac{T_{ON}}{T_{ON}\, T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relation-ship between the currents is the following :

$$I_{iDC} = I_{oDC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula :

$$\eta\ \% = \frac{P_o}{P_i} \cdot 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o,

plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \quad (12)$$

DC LOSSES

P_{sat} :saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} + V_{sat}\ I_o \frac{V_o}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current Io.

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F\ I_o \frac{V_i - V_o}{V_i} = V_F I_o\ (1 - \frac{V_o}{V_i}) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S\ I_o^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current :

$$P_q = V_i\ I_q, \quad (16)$$

in which Iq is the operating supply current at the operating switching frequency.
Iq includes the oscillator current.

SWITCHING LOSSES

P_{sw} :switching losses of the power transistor :

$$P_{sw} = V_i\ I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculation T_{ON} and T_{OFF} through (4) and (9) respectively it follows that :

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \qquad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

But because :

$T_{ON} + T_{OFF} = T$ and $\Delta I_L^+ = \Delta I_L^- = \Delta I_L$,

it follows that :

$$T_{ON} = \frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T \quad (17)$$

Calculating L, the previous relation becomes :

$$L = \frac{(V_i - V_o)\ V_o}{V_i\ \Delta I_L} T \quad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that :

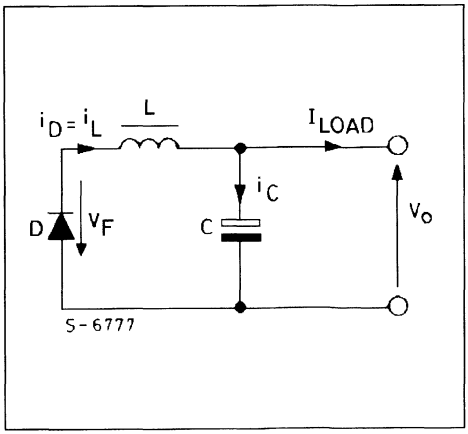
$L = \frac{(V_i - V_o)\ V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$ where L is in Henry and f in Hz

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by :

$i_C(t) = i_L(t) - I_o$

Figure 5: Equivalent Circuit Showing Recirculation when Q1 is Turned Off.



From the behaviour shown in Fig. 4 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that :

$$\Delta V_C = \frac{\Delta I_L}{4C} \frac{T}{2} = \frac{\Delta I_L T}{8C} = \frac{\Delta I_L}{8fc} \qquad (19)$$

but, remembering expression (4) :

$$\frac{\Delta I_L^+ = (V_i - V_o) T_{ON}}{L} \text{ and } T_{ON} = \frac{V_o}{V_i} T$$

therefore equation (19) becomes :

$$\Delta V_C = \frac{(V_i - V_o) V_o}{8 V_i f^2 L C}$$

Finally, calculating C it follows that :

$$C = \frac{(V_i - V_o) V_o}{8 V_i \Delta V_C f^2 L} \qquad (20)$$

where : L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true :

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \qquad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C\ (dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value. Moreover, the following is true :

$$v_L = L \frac{di_L}{dt} \qquad (23)$$

where $di_L = \Delta I_o$

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and (23) and equalizing, it follows that :

$$L \frac{di_L}{v_L} = C \frac{dv_C}{i_C}$$

Calculating dv_c and equalizing it to ΔV_o, it follows that :

$$\Delta V_o = \frac{L \Delta I_o^2}{C (V_i - V_o)} \qquad (24) \quad \text{for } + \Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \qquad (25) \quad \text{for } - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the under-shoot, which could trigger the reset function.

DEVICE DESCRIPTION

For a better understanding of how the device functions, a description will be given of the principle blocks that compose the device. The block diagram of the device is shown in fig.6

POWER SUPPLY

The device contains a stabilized regulator (Vstart = 12V) that provides power to the analogic and digital control blocks as well as the section of the bootstrap. The Vstart voltage also powers the blocks that operates the internal reference voltage of 5.1V, with a precision of ±2%, necessary for the feedback.

OSCILLATOR, SYNC. AND VOLTAGE FEEDFORWARD FUNCTIONS

The oscillator block generates a sawtooh wave signal that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal that will then sent to the power output stage. The oscillator also contains the voltage feedforward function that, being completely integrated, does not require additional external components to function. The VFF function operates with supply voltages from 15V to 45V. The $\Delta V/\Delta t$ of the sawtooh is directly proportional to the supply voltage Vi.

As Vi increases, the conduction time (ton) of the power transistor decreases in such way as to provide to the coil, and therefore to the load, the product Volt x Sec constant.

Figure 6: Block Diagram of the 10A Monolithic Regulator L4970A.

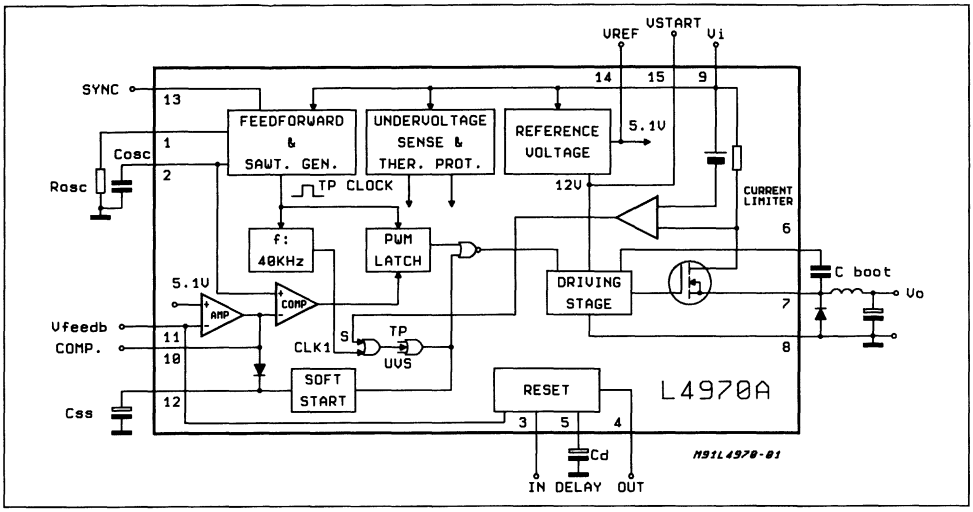


Figure 7: Voltage Feeforward Waveform.

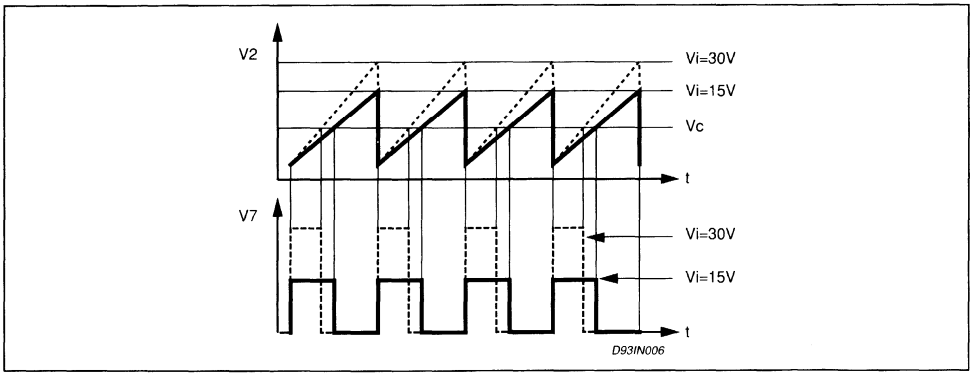


Fig. 7 shows the duty-cycle varies as a result of the changes in slope of the ramp with the input voltage Vi. The output of the error amplifier should not change to maintain the output voltage in regulation. This function allows for the increase of speed in response to the rapid change of the supply voltage and for a greatly reduced ouput ripple at the mains frequency.

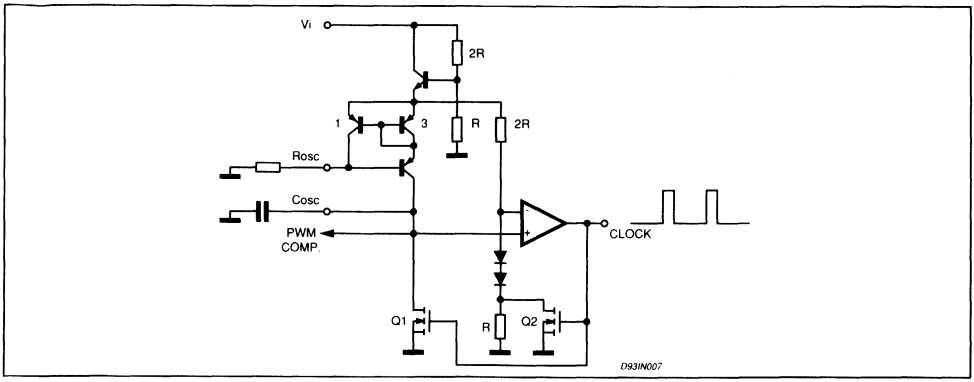
In fact, the slope of the ramp is modulated by the ripple, generally present in the order of several volts on the input of the regulator, particularly when the solution with a mains transformer is used.

Fig. 8 shows the simplified electrical diagram of the oscillator.

A resistor, connected between the Rosc pin and GND, sets the current that is internally reflected in the pin Cosc, in order to charge the external capacitor to which it is connected. The voltage to the Rosc pin is not fixed, but is tied to the instantaneous value of Vi; this is needed to achieve the feedforward voltage function, in which the slope of the ramp is directly proportional to the supply voltage. A comparator senses the voltage at the Cosc capacitor. When the voltage reaches the value present at the inverting input of the comparator, the output from the comparator goes high and is sent to the two transistors Q1 and Q2.

Q1 is responsible for discharging the external Cosc capacitor with a current of approx. 20mA, while Q2 imposes at the inverted input of the comparator a voltage of 2Vbe (approx. 1.3V) that is the low-threshold of the ramp. Some useful formulas for calculating the various parameters of the oscillator block are:

Figure 8: Oscillator Circuit.



1) Oscillator charge current:

$$I_{CHARGE} = \frac{V_i - 9V_{be}}{R_{osc}} \quad (For\ 15V < Vi < 45V)$$

2) Oscillator discharge current:

$I_{DISCH} = 20mA$

3) Peak voltage ramp:

$$V_{th-H} = \frac{V_i - 9V_{be}}{Rosc} + 2V_{be}$$

This formula is obtained in the following way: indicating with Ve the voltage of the emitter of the NPN transistor connected to Vcc, and V- the voltage at the inverted input of the comparator, one has:

$$(a)\quad V_e = \frac{V_i}{3} - V_{be}$$

$$(b)\quad V- = \left(\frac{V_e - 2V_{be}}{3R} \cdot R\right) + 2V_{be}$$

by substituting (a) into (b), one obtains:

$$V- = \frac{(\frac{V_i}{3} - V_{be}) - 2V_{be}}{3} + 2V_{be} = \frac{V_i - 9V_{be}}{9} + 2V_{be}$$

4) Valley voltage ramp:

$V_{th-L} = 2V_{be}$

5) Switching frequency:

$$f_{SW} = \frac{9}{R_{osc}\, C_{osc}}$$

It should be noted that formula (5) does not take into account the discharge time of Cosc which cannot be neglected when one is working at frequencies equal or higher than 200KHz. The discharge time is also tied to the value of Cosc itself.

Analitycally one has:

$$6)\quad T_{DISCH} = \frac{V_{th-H} - V_{th-L}}{20mA} \cdot C_{osc}$$

from which is obtained the more closely approximate expression of the oscillator frequency:

$$7)\quad f_{SW} = \frac{1}{\frac{R_{osc} \cdot C_{osc}}{9} + T_{DISCH}}$$

During the discharge time of Cosc, a clock pulse is generated internally that is made subsequently available on the Sync. pin and that can be used to synchronize other regulators. (3 devices of the same family maximum). The Sync. pulse generated has a typical range of 4.5V and the current availability is 4.5mA. In general, it is better that the Sync pulse is at least 300-400ns in order to be able to synchronize a range of existing regulators; to obtain this result, values of suggested capacitors, in different test circuits, have been selected. The typical duration of the synchronizing pulse with the suggested values of Cosc are as follows:

L497X Family (MULTIWATT PACKAGE)	
C_{osc} (nf) - R_{osc} = 16KΩ	Sync (ns)
0.68	140
1	230
1.2	270
1.5	330
2.2	450
3.3	680
4.7	1100

L497X Family (POWERDIP PACKAGE)	
C_{osc} (nf) - R_{osc} = 30KΩ	Sync (ns)
1.2	230
1.5	280
2.2	420
3.3	600
4.7	900

Obviously, synchronize pulses of eccessive duration can greatly reduce the max duty-cycle and produce distortions in the sawtooth of the synchronized regulator working as slave.

P.W.M.

Comparing the sawtooth signal generated by the oscillator and the output of the error amplifier, generates the PWM signal which is sent to the driver of the output power stage. The PWM signal, in the path towards the output stage, also encounters a latch block to prevent other pulses from being sent at same period to the output, possibly damaging the power stage. In the PWM block, a duty-cycle limiter has also been introduced. Such a limiter is obtained by taking advantage of the synchronizing pulse generated, the power output stage is inhibited. Even if the error amplifier gives a large signal to the peak of the ramp, the power stage will not be able to operate in DC, but will be switched off at each clock pulse.

The max. obtainable duty-cycle is higher than 90%; this, however depends on the working frequency and the value of Cosc. Using the formulas 6) and 7) a precise calculation can be done.

SOFT START

The Soft Start function is essential for a correct startup of the device and for an output voltage that, at the switch on, increases in a monotonous mode without dangerous output overvoltages and without overstress for the power stage.

Soft Start operates at the startup of the system and after an intervention of the thermal protection. Fig. 9 shows the simplified diagram of the startup functions. The function is carried out by means of an external capacitor connected to the Soft Start pin, which is charged with a constant current of about 100μA to a value of around 7V. During the charging time, the output of the error transconductance amplifier, because of Q1, is forced to increase at the same rising edge time of the external softstart capacitor Css.

Figure 9: Soft Start Circuit.

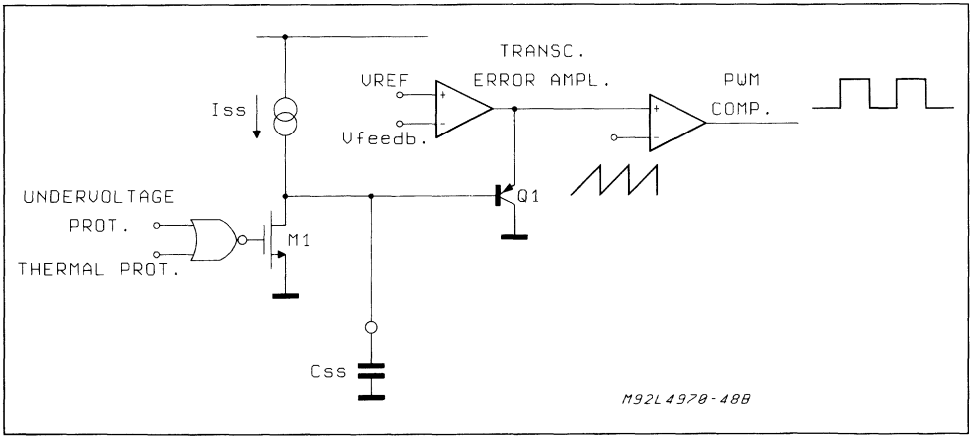
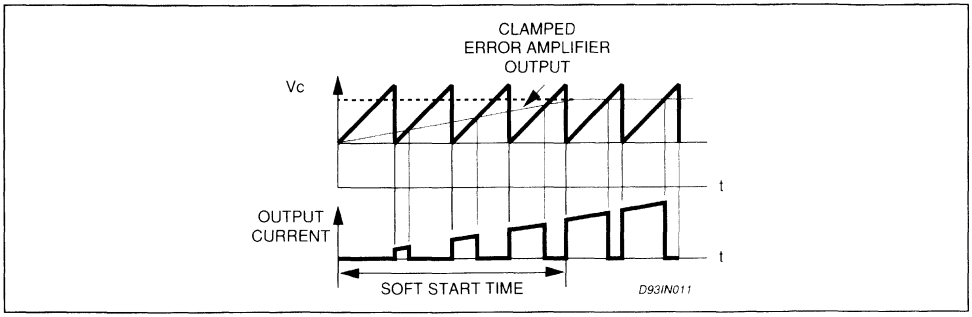


Figure 10: Soft Start Waveforms.



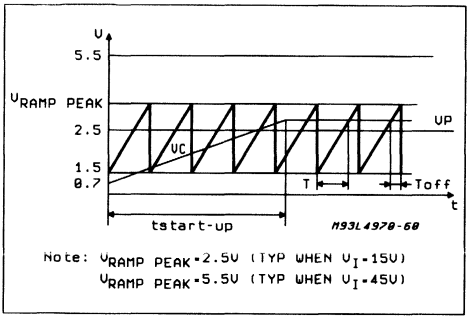
The PWM signal begins to be generated as soon as the output voltage of the error amplifier crosses the ramp; at this point the output stage begins to commutate, slowly increasing its ON time (see fig. 10).

The charge of the Css capacitor, as already mentioned, begins each time the device is supplied with power and after which an anomalous condition is created, as the intervention of thermal protection or of the undervoltage lockout.

CALCULATING THE DUTY-CYCLE AND SOFT-START TIME

Let us suppose that the discharge time of the oscillator capacitor, Cosc, is neglected. This is an approx. valid for switching frequencies up to 200KHz. Let us indicate with Vr the output voltage of the error amplifier, and with Vc the voltage of the oscillator ramp.

Figure 11: Soft Sart Time Waveform.



The PWM comparator block commutates when Vr = Vc. Therefore:

$$8)\quad V_r = V_c = \frac{V_{pp}}{T}\cdot t = \frac{V_i - 9V_{be}}{9\cdot T}\cdot t$$

from which is obtained

$$9)\quad t = \frac{V_r \cdot T \cdot (V_i - 9V_{be})}{9}$$

The time **t** obtained from this equation is equal to the ON time of the power transistor. The corresponding duty-cycle is given by:

10)

$$D = \frac{t_{on}}{T} = \frac{V_r \cdot T \cdot (V_i - 9V_{be})}{9T} = \frac{V_r \cdot (V_i - 9V_{be})}{9} = \frac{V_O}{V_i}$$

Consequently, after leaving the discharged capacitor of Soft Start, the output of the regulator will reach its value when the voltage across the Css capacitor, charged with constant current, has reached the value Vr - 0.5V.

The time necessary in order that the output rises from zero to the nominal value is given by:

$$11)\quad t_{start\text{-}up} = C_{ss}\cdot\frac{(V_r - 0.5V)}{I_{ss}}$$

in which Css is the Soft Start capacitor and Iss the Soft Start current. Considering Soft Start time as tss, the required time for the Soft Start capacitor to change itself approx from (2Vbe - 0.5V) = (1.2V - 0.5V) to Vr - 0.5V, is:

$$12)\quad t_{ss} = C_{ss}\cdot\frac{(V_r - 1.2V)}{I_{ss}}$$

By taking Vr from (10):

$$13)\quad V_r = \frac{V_o}{V_i}\cdot\frac{9}{V_i - 9V_{be}}$$

and substituting it in (12), we obtain:

$$14)\quad t_{ss} = \frac{C_{ss}}{I_{ss}}\left(\frac{V_o}{V_i}\cdot\frac{9}{V_i - 9V_{be}} - 1.2V\right)$$

UNDERVOLTAGE LOCKOUT

The device contains the protection block of undervoltage lockout which keeps the power stage turned-off as long as the supply voltage does not reach at least 12V. At this point the device starts up with Soft Start.

The function of undervoltage is also provided with an hysteresis of 1V to make it better immune to the ripple present on the supply voltage.

ERROR AMPLIFIER

The error amplifier is a transconductance type and deliver an output current proportional to the voltage inbalance of the two inputs. The simplified diagram is presented in fig 12.The principal characteristics of this uncompensated operational amplifier are the following:

Gm = 4mA/V, Ro = 2.5Mohm, Avo = 80dB, Isource-sink = 200uA, Input Bias Current = 0.3uA.

The frequency response of the op. amp. is given in fig. 13.

Ignoring the high frequency response and hypothesizing that the second pole is below the 0 dB axis in the all the conditions of loop compensation, it is possible to make a first approximation with the equivalent circuit of fig. 14

Figure 12: Error Amplifier Circuit.

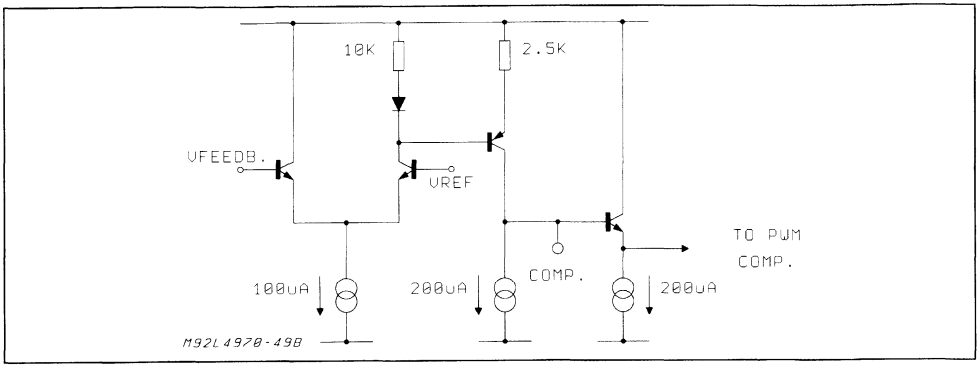


Figure 13: Open loop gain (error amplifier only)

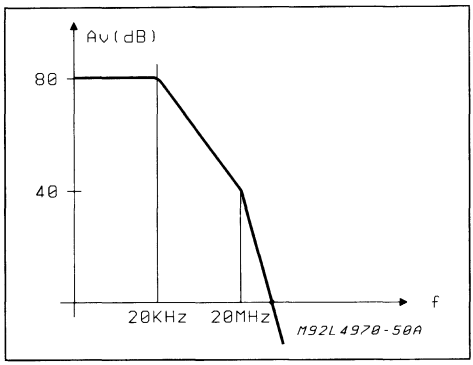
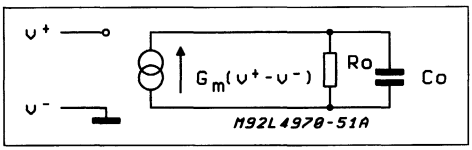


Figure 14: Error amplifier equivalent circuit.



In which:

15) $Av(s) = Gm \cdot \frac{R_o}{1 + sR_o C_o}$ where $C_o = 3pF$

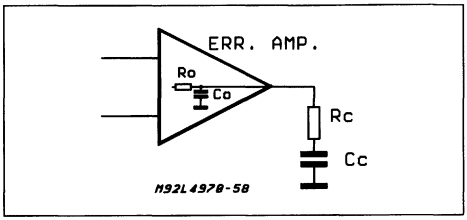
The error amplifier can be easily compensated thanks to the high output impedance (see fig. 14)

The resulting transfer function is as in the following:

(16)

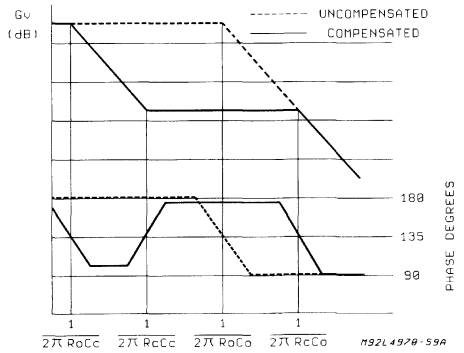
$$Av(s) = Gm \cdot \frac{R_o \cdot (1 + sRcCc)}{s^2 R_o C_o R_c C_c + s(R_o C_c + R_o C_o + R_c C_c) + 1}$$

Figure 15: Compensation network of the error amplifier



The Bode diagram is shown in fig.16.

Figure 16: Bode plot showing gain and phase of compensated error amplifier



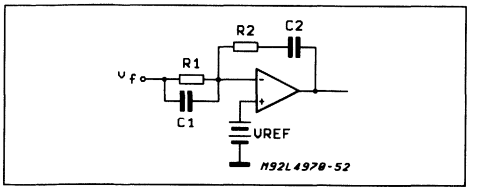
The compensation circuit introduces a pole at low frequency and a zero that is generally calculated to be put in the proximity of the resonance frequency of the output LC filter.

The second pole at high frequency generally falls in a zone of no interest (for the system stability, one must consider the zero introduced by ESR

characteristic of the output capacitor. Not all the designers agree on this solution).

If necessary, however, one can turn to more sophisticated compensation circuitry. An example is shown in fig. 17.

Figure 17: One pole, two zero compensation network



Such a circuit introduces a pole at low-frequency and two zeros.

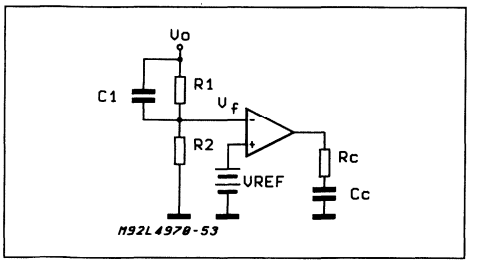
$$17)\quad Z1 = \frac{1}{2\Pi\ R1\ C1} \qquad Z2 = \frac{1}{2\Pi\ R2\ C2}$$

It must be remembered, however, that because of the high output impedance of the error amplifier, a second pole is also present:

$$18)\quad P2 = \frac{Gm}{2\Pi\ C1}$$

We normally suggest a high value for R1 to reduce the value of the capacitor C1 and allocate the pole P2 at the highest possible frequency. The essential limitation to the max value of R1 is the offset introduced by the input bias current of the error amplifier. In the case of output voltage regulated higher than 5.1V, an external divider should be introduced. It's than possible to introduce a second zero using the following network:

Figure 18: Compensation network for output voltages higher than 5.1V



Two zeros and two poles are introduced:

$$19)\quad Z1 = \frac{1}{2\Pi\ R_o\ C_c} \qquad Z2 = \frac{1}{2\Pi\ R1\ C1}$$

$$P1 = \frac{1}{2\Pi\ R_o\ C_c} \qquad P2 = \frac{1}{2\Pi\ Rx\ C1}$$

$$\text{Where } Rx = \frac{R1 \cdot R2}{R1 + R2}$$

APPLICATION EXAMPLE

Consider the block diagram of fig. 19, representing the internal control loop section, with the application values:
Fswitch = 200KHz, L = 100µH, C = 1000µF,
Po = 50W, Vo = 5.1V, Io = 10A and Fo = 500Hz.
G_{loop} = PWM · Filter

Figure 19: Block diagram used in stability calculation

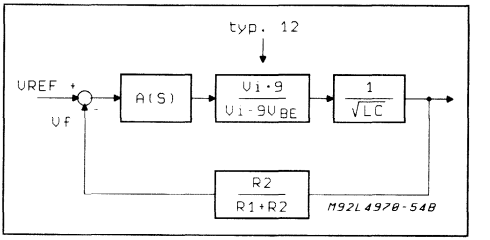
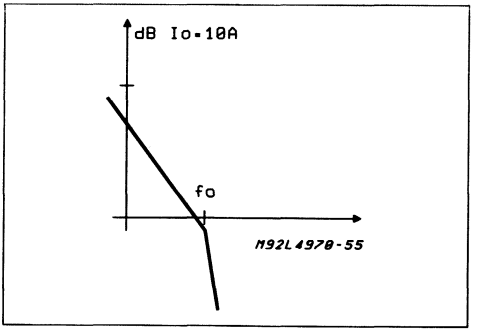


Figure 20: Frequency behaviour of the circuit of fig. 19



The system requires that DC gain is maximum to achieve good accuracy and line rejection. Beyond this a bandwidth of some KHz is usually required for a good load transient response. The error amplifier transfer function must guarantee the above constrainst. A compensation network that could be used is shown in fig. 21.

$$A(s) = \frac{(1 + sR1\ C1)\ (1 + sR2\ C2)}{sR1\ C1\ (1 + s\frac{C1}{Gm})}$$

Figure 21: Compensation network.

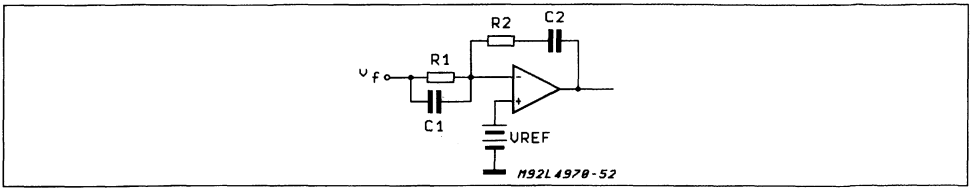
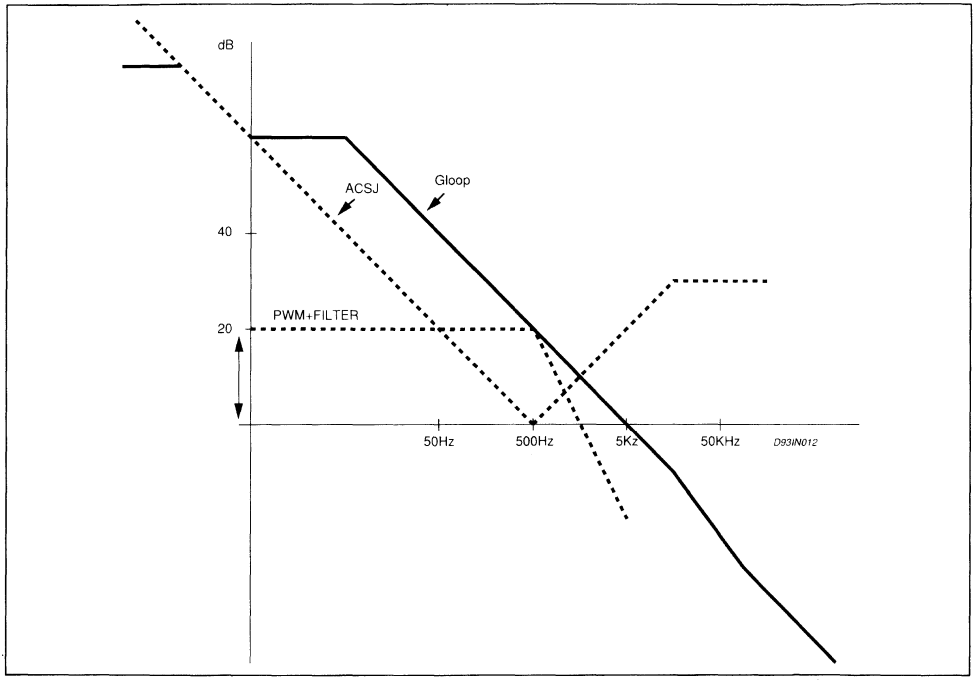


Figure 22: Bode plot of the regulation loop with the compensation network of fig. 21.



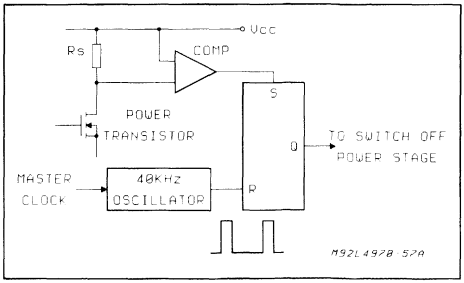
The criterium is to define Z1, Z2 close to the resonant pole of the output LC filter. The Gm/2ΠC1 pole must be placed at a frequency at which open loop gain is below 0dB axis (fig. 22).

CURRENT LIMITING

A complete regulation system will be equipped with a good current limiter able to protect from load breaking and operator error controlls.
The current limiting function is totally integrated and does not require any external component. The output current is sensed by an internal low-value resistor, in series with the drain of the DMOS vertical power transistor..

A precision current limitation of ± 10% relative at the peak current is guaranted. During overcurrent situation the pulse by pulse current limitation produce an output stage switching frequency reduction. The block diagram of the current limiting is shown in fig. 23.

Figure 23: Current protection circuit.



In overcurrent situation the comparator send a signal at the flip-flop set input, an inhibit pulse is immediatly generated from it and sended at the output stage switching off the power mos.

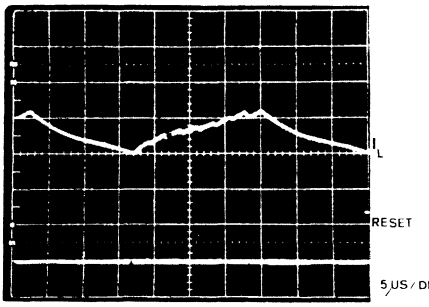
A reset pulse input in generated from an 40KHz internal oscillator.

After the first reset pulse the control loop will start to regulate the system an the output current will increase following the principal oscillator frequency. If overcurrent condition is still present the current limiting will be activate again.

This type of current limiting ensure a constant output current in overload or short circuit condition and allow a good reliability at high frequency (500KHz) reducing the problems relative at the internal signal delay through the protection blocks.

The inductor current in overload condition in shown in fig. 24.

Figure 24: Overload inductance current.



The 40KHz internal oscillator is synchronized with the principal one. If the system work with a oscillator tracks the principal oscillator frequency. In this way the switching frequency will not increase in overload situation.

A particular care has to be taken in the inductor value in order to avoid problems during overload or short circuit conditions. A critical situation is present with high switching frequency, (more than 200KHz) where a small inductor value is used and with high capacitive load.

In order to return in nominal condition after a short circuit the inductor ripple at 40KHz with the nominal output voltage and current has to be lower than the current limitation value.

Example

Let us consider L4970A, 10A. (the same approach can be used for all the family).

The inductor ripple current is given by the following formula:

$$\Delta I_L = \frac{(V_i - V_o) \cdot V_o}{V_i \cdot fsw \cdot L}$$

where fsw = 40KHz ±10%

In order to get the maximum inductor ripple current, the previous formula becomes:

$$\Delta I_L = \frac{(V_{imax} - V_{omax}) \cdot V_{omax}}{V_{imax} \cdot f_{sw\,min} \cdot L}$$

The current limitation for L4970A will start to work at 13A.

therefore:

$$I_{lim\,min} > I_{onom} + \frac{\Delta I_L}{2}$$

where I_{onom} = 10A for L4970A.

POWER FAIL-RESET CIRCUIT

The L4970A include a voltage sensing circuit that may be used to generate a power on power off reset signal for a microprocessor system. The circuit senses the input supply voltage and the output generated voltage and will generate the required reset signal only when both the sensed voltages have reached the required value for correct system operation. The Reset signal is generated after a delay time programmable by an external capacitor on the delay pin. Fig 25 shows the circuit implementation of Reset circuit. The supply voltage is sensed on an external pin, for programmability of the threshold, by a first comparator. The second comparator has the reference threshold set at slightly less the ref. voltage for the regulation circuit and the other input connected internally at the feedback point on the regulated voltage. When both the supply voltage and the regulated voltage are in the correct range, transistor Q1 turns off and allows the current generator to charge the delay capacitor discharges completely before initialization of a new Reset cycle. The output gate assures immediate take of reset signal without waiting for complete discharge of delay capacitor. Reset output is an open collector transistor capable of sinking 20mA at 200mV voltage. Fig 26 shows reset waveforms.

Figure 25: Power fail and reset circuit.

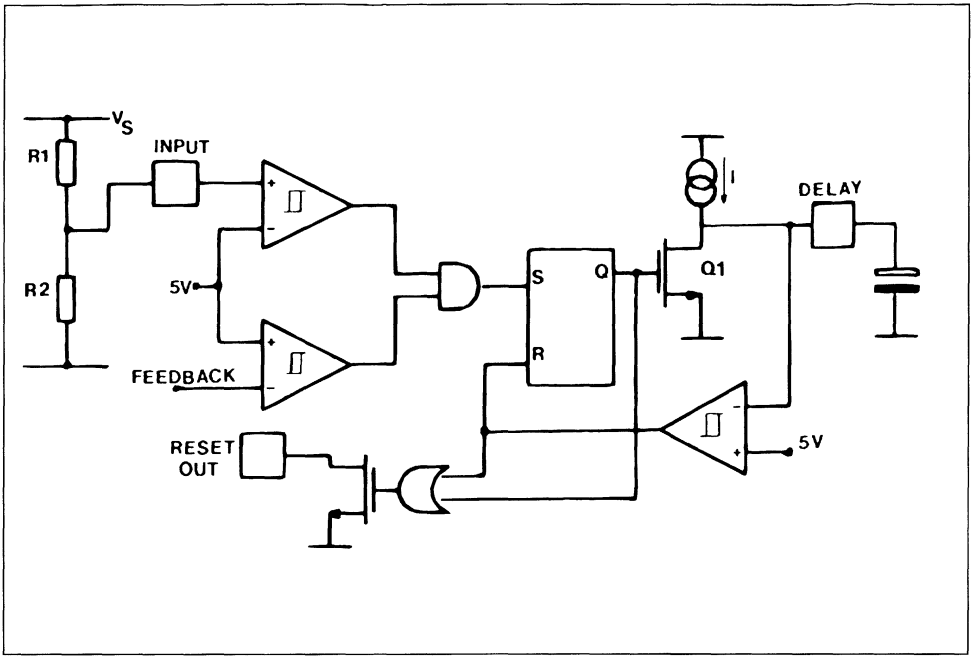


Figure 26: Reset and power fail and reset circuit.

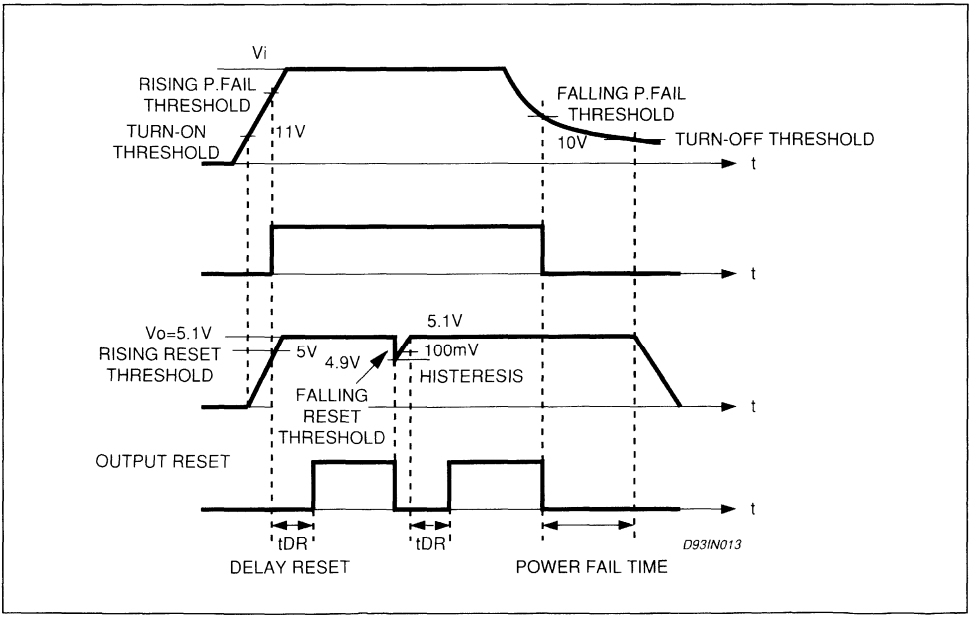
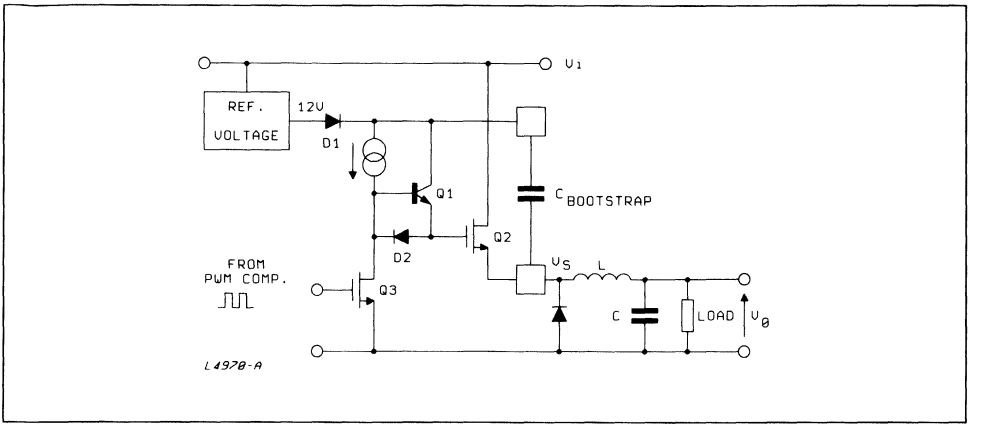


Figure 27: Power stage circuit.



POWER STAGE

The simplified diagram of the output stage is shown in the fig. 27.

The power stage and the circuit connected with it are by far the most important and critical components when one wants to obtain good performance at high switching frequency.

The power transistor must have excellent characteristics from the point of view of both the switching speed and the robustness.

The transistor DMOS, with its intrinsic characteristics of elevated speed, no second breakdown phenomenom and easy driving proves to be particularly suitable for this type of application that normally works at high frequency.

For a properly driving of the DMOS gate it is necessary to use an external bootstrap capacitor.

When the voltage Vs is low the Cboot capacitor is charged through the internal diode D1, at the value of voltage equal to that of Vstart, which is about 12V; the next step oversees that Q3 is turned off, Q2 is driven in gate by Q1 so that Q1 can go in saturation, and its source can go up rise towards Vi.

Cboot maintains its charge and guarantees a voltage equal Vi+12V at the gate of Q7, so that can enter into region of low resistance.

At this point the diode D1 turns on to be inversely polarized, disconnecting the 12V section from that of the driving power stage.

When Q2 is ON the driven current of the power stage requires from the bootstrap capacitor a typical current of 400uA.

When Q2 is Off a current of 2.5mA is required to mantain Q2 in that state. This current however is not delivered from the bootstrap capacitor, but rather from the internal regulator of 12V, while the output current flowing in the freewheeling diode.

The circuit described is capable of obtaining commutation, rise and fall time, a typical value of 50ns.

In principle, it would have been feasible to reduce furthermore the commutation time whithout any reliability problems.

This was not believed to be advantageous since it would not have been of any benefit if one thinks of the trr time of the catch diode (with trise of 50ns also the Schottky diodes begin to show limitations) and of the conseguent increase of different disturbances caused bt too higly elevated dI/dt.

Ther following table shows the main features of the DMOS transistor.

Figure 28: Gate-charge curve for the power

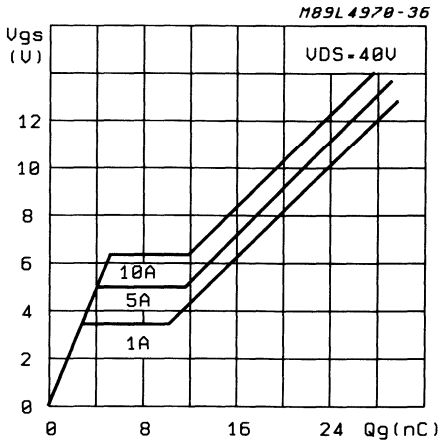


Table 1.

B_{VDSS} > 60V	at I_D = 1mA		V_{GS} = 0V
$R_{DS(ON)}$ = 100mΩ	at I_D = 10A	T_j = 25°C	V_{GS} = 10V
$R_{DS(ON)}$ = 150mΩ	at I_D = 10A	T_j = 150°C	V_{GS} = 10V
V_{TH} = 3V	at I_D = 1mA		

THERMAL SHUTDOWN

The thermal protection intervenes when the junction temperature reaches 150°C; it intervenes directly on the output stage turning it off quikly and in the meantime discharging the soft start capacitor.

The reference voltage and the oscillator will continue to work regularly.

The thermal shutdown has a hysteresis, after its intervention, it is necessary to wait for the junction temperature to lower around 30°C before the device will begin to work properly again.

The device restart to work by using the soft start function.

Table 2: High Current Switching Regulator ICs.

Parameter	L497X FAMILY					
	L4970A	**L4977A**	**L4975A**	**L4974A**	**L4972A**	**L4972AD Surf. Mount.**
Max. Input Operating Voltage	50V	50V	50V	50V	50V	50V
Output Voltage Range	5.1V (±2%) to 40V					
Max. Output Current	10A	7A	5A	3.5A	2A	2A
Power Switch R_{DSON} at 25°C	0.13Ω typ.					
Switching Mode Control System	Continuous Mode, Direct Duty Cycle Control with Voltage Feed-Forward					
Max. Switching Freq.	500KHz	500KHz	500KHz	200KHz	200KHz	200KHz
Efficiency V_{INPUT} = 35V V_{OUT} = 5.1V	10A 80% at 200KHz	7A 80% at 200KHz	5A 85% at 200KHz	3.5A 85% at 100KHz	2A 85% at 100KHz	2A 85% at 100KHz
Current Limiting	Constant Current					
Soft Start	Yes					
Reset and Power Fail	Yes					
Synch	Yes					
Crowbar	No					
Package Max. $R_{th\ j\text{-}case\ (pin)}$ $R_{th\ j\text{-}amb}$	Multiwatt15 1°C/W 35°C/W	Multiwatt15 1°C/W 35°C/W	Multiwatt15 1°C/W 35°C/W	Powerdip 16+2+2 12°C/W 60°C/W	Powerdip 16+2+2 12°C/W 60°C/W	SO20L 6°C/W 80°C/W

APPLICATIONS

Even though the regulators of the L4970A family has been designed to work only in step down configuration we will see next how these regulators can be use in large range of applications.
In same cases the L4970A device will be used as an example for the entire family assembled in Multiwatt package and the L4974A will be used for the types in powerdip package.

Anyway the suggested applications can be extended to any other device of the family by adjusting if necessary the external components using the given equation for the calculation.

Typical Application

The Fig. 29 shows the electrical diagram of the typical application, complete with all the auxiliary functions. The same application suggested in the data sheet as test circuit and is the same used for the final dynamic test. All our devices are 100% tested both in static and dynamic conditions.

Included in the dynamic test are obviously the external components: the coil, catch diode and output capacitor which have been defined for all regulators.

Shown below are the electrical diagrams of 5 devices that compose the family of this regulator complete with the value of the external components and with the relative pcb layout.

Output voltages higher than 5.1V are possible using an output resistive divider. For V_o > 24V, for safety reasons it must be avoided the zero load condition. In the application with high current, connected to the output divider are added two other resistances that permit the separation of sensing and forcing, in such way as to compensate the fall of voltage on the connecting cables between the output and the load.

Connecting directly the output to the feedback pin a 5.1V ±2% is obtained. The following table can be help for a rapid calculation of a resistor divider to obtain some of the most standard output voltage.

Figure 29: L4970A Typical Application Circuit.

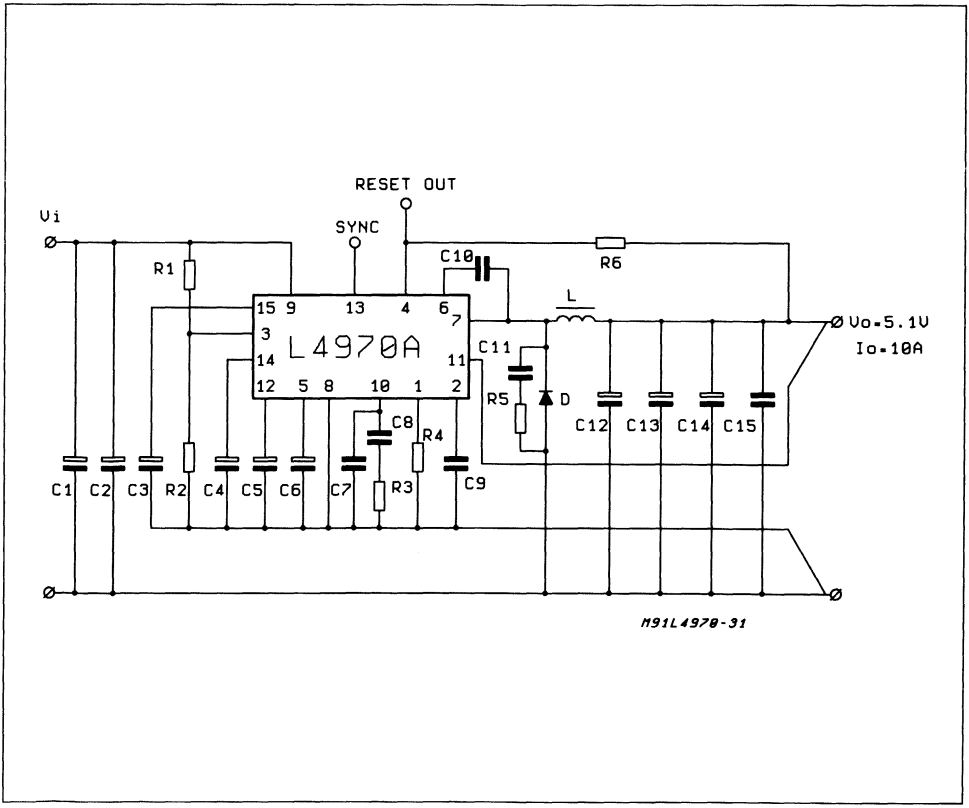
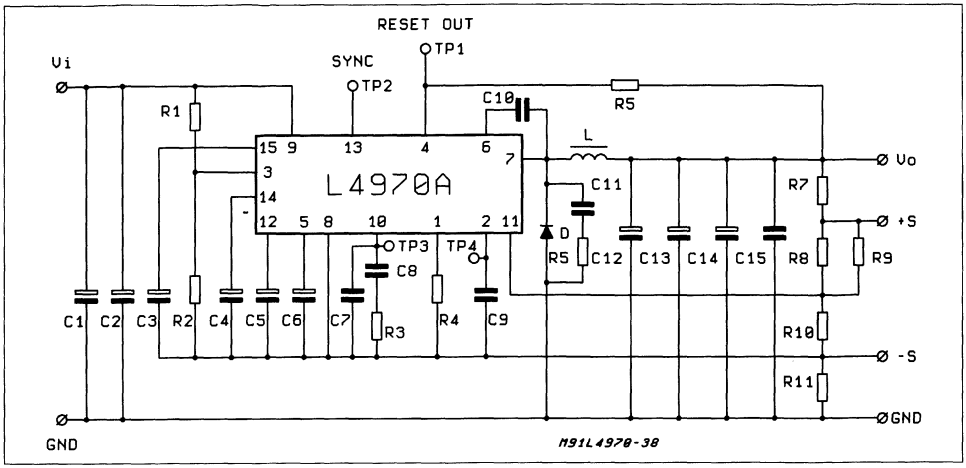


Figure 30: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 10A)
For component values, refer to test circuit part list.

PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 31: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 30. (1:1 scale)

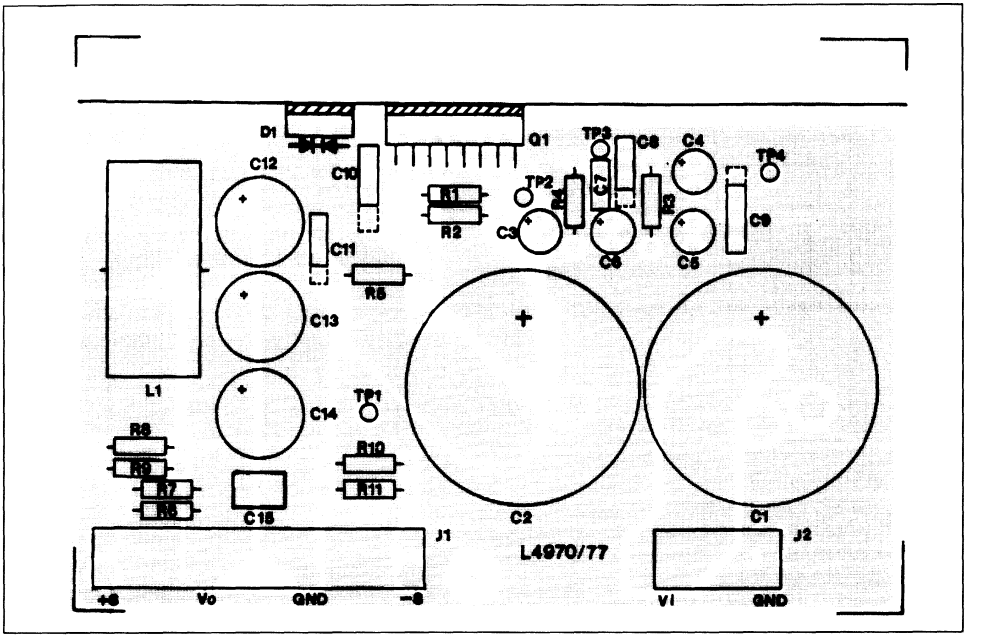


Figure 32: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 30. (1:1 scale)

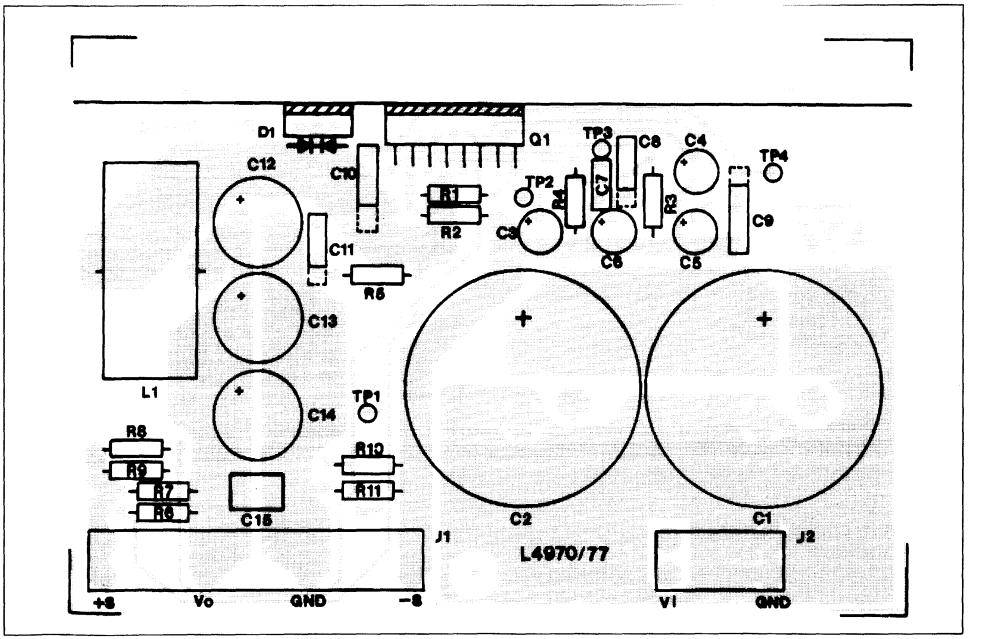
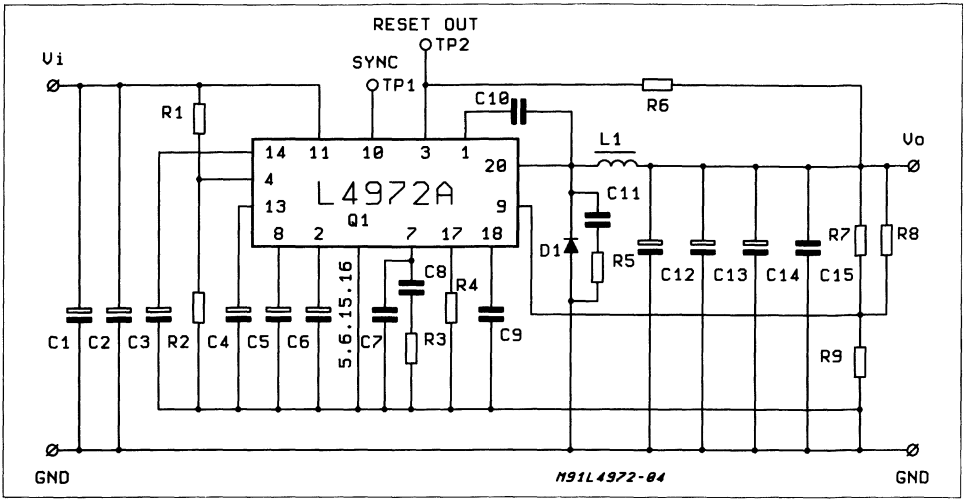


Figure 33: Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 2A ; f_{sw} = 100KHz)
$V_{o\ RIPPLE}$ = 30mV (at 1A)
Line regulation = 12mV (V_i = 15 to 50V)
Load regulation = 7mV (I_o = 0.5 to 2A)
for component values Refer to the fig. 32 (Part list).

PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film
D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B

SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Figure 34: Component Layout of fig. 33 (1:1 scale). Evaluation Board

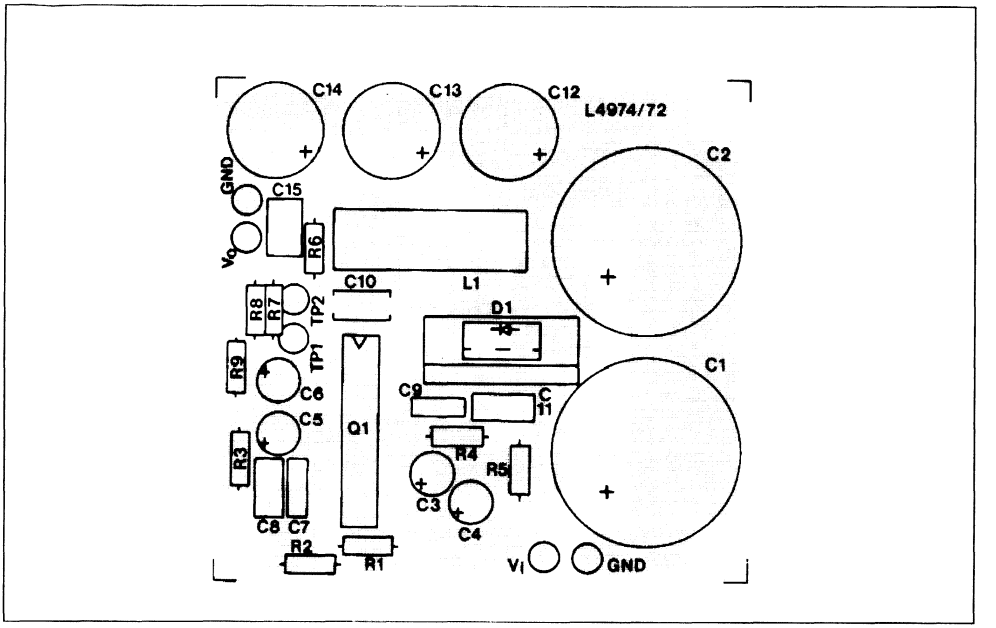


Figure 35: P.C. Board and Component Layout of the ciruit of fig. 33. (1: scale)

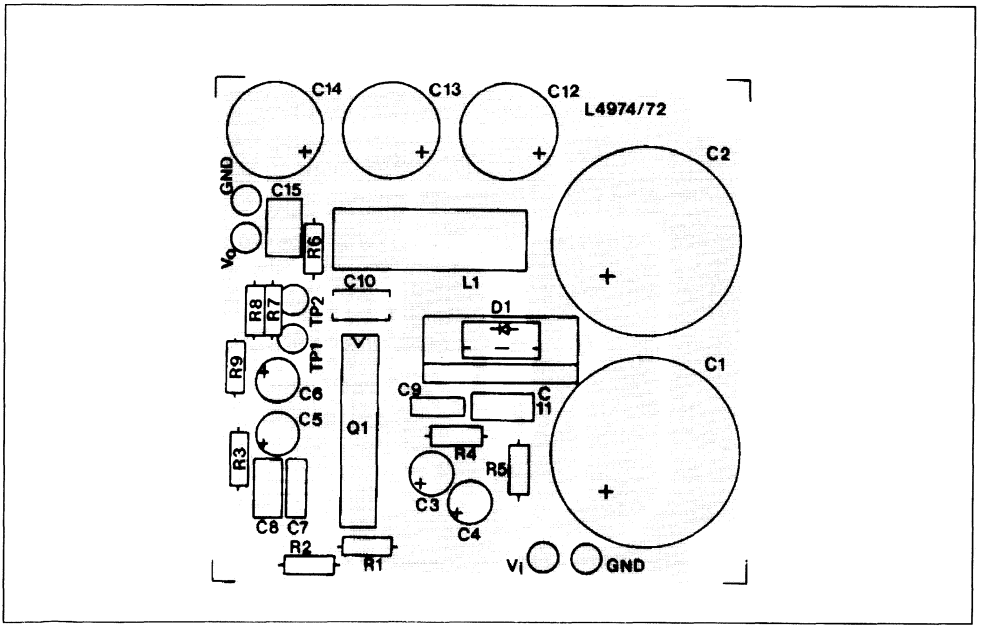
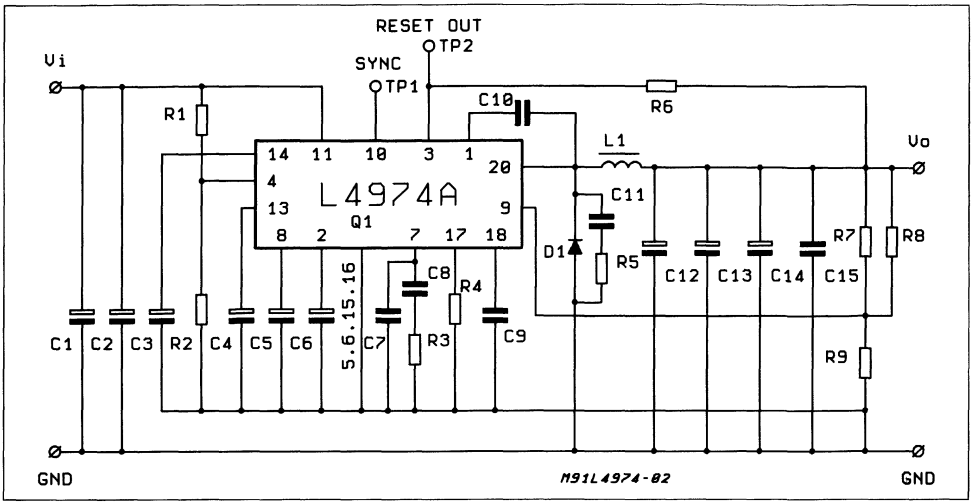


Figure 36: Test and Evaluation Board Circuit.



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 3.5A ; f_{sw} = 100KHz)
$V_{o\ RIPPLE}$ = 30mV (at 1A)
Line regulation = 12mV (V_i = 15 to 50V)
Load regulation = 7mV (I_o = 0.5 to 3.5A)
for component values Refer to the fig. 35 (Part list).

PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film
D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

* 2 capacitors in parallel to increase input RMS current capability.
** 3 capacitors in parallel to reduce total output ESR.

Figure 37: Component Layout of fig. 36 (1:1 scale). Evaluation Board

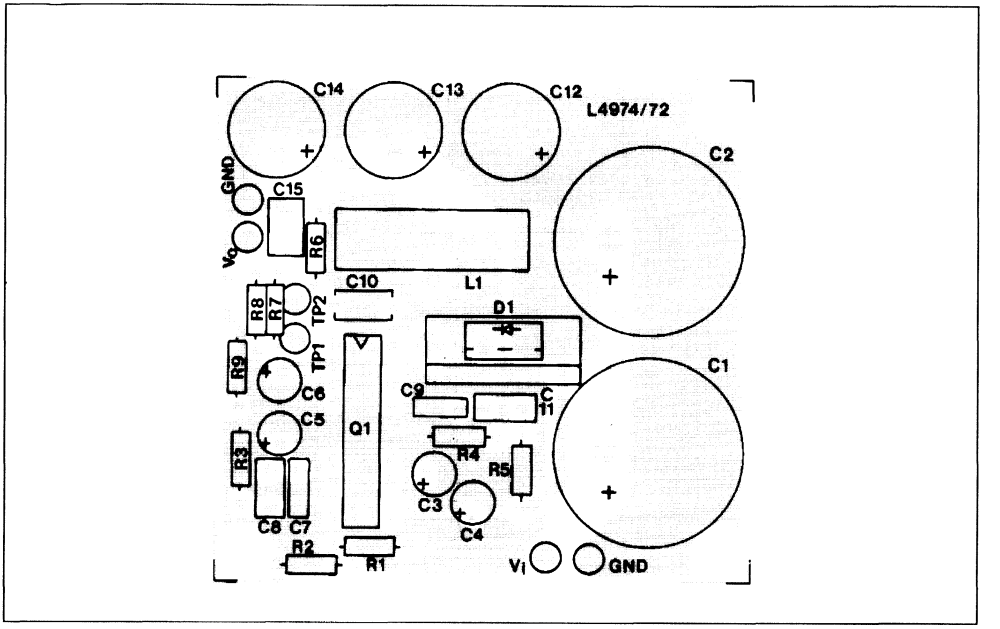


Figure 38: P.C. Board and Component Layout of the ciruit of fig. 36. (1: scale)

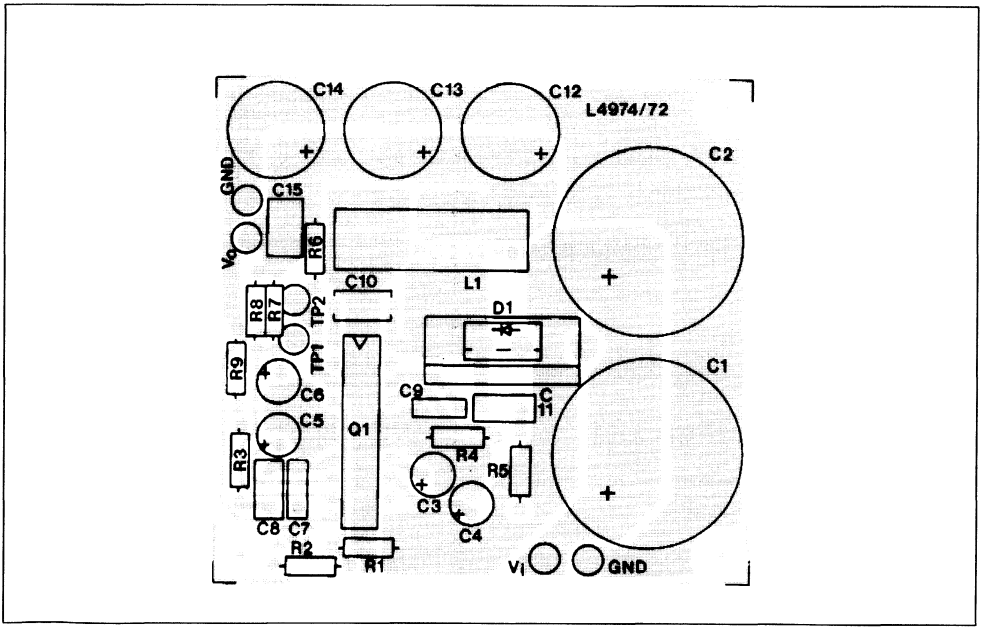
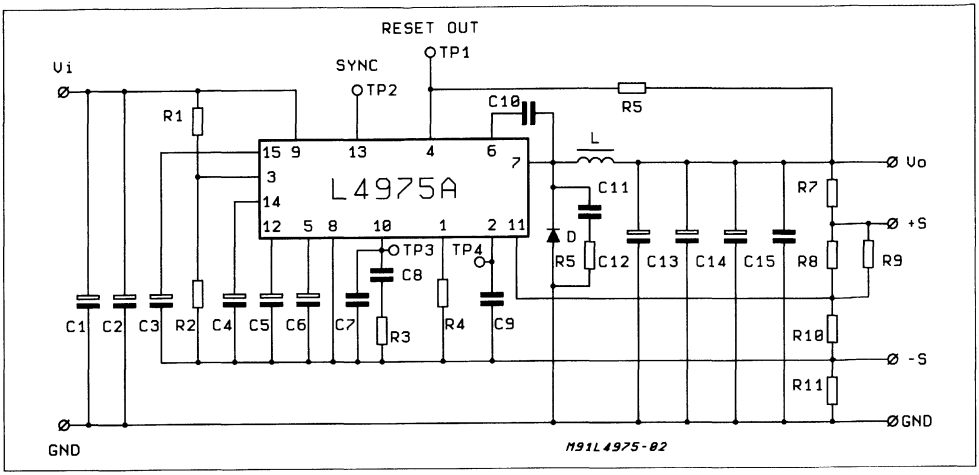


Figure 39: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 10A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 5A)
For component values, refer to test circuit part list.

PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 760CT (or 7.5A/60V or equivalent)	
L1 = 80µH	core 58930 MAGNETICS 47 TURNS Ø 113mm (AWG 76) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 40: P.C. Board (component side) and Components Layout of Figure 39. (1:1 scale).

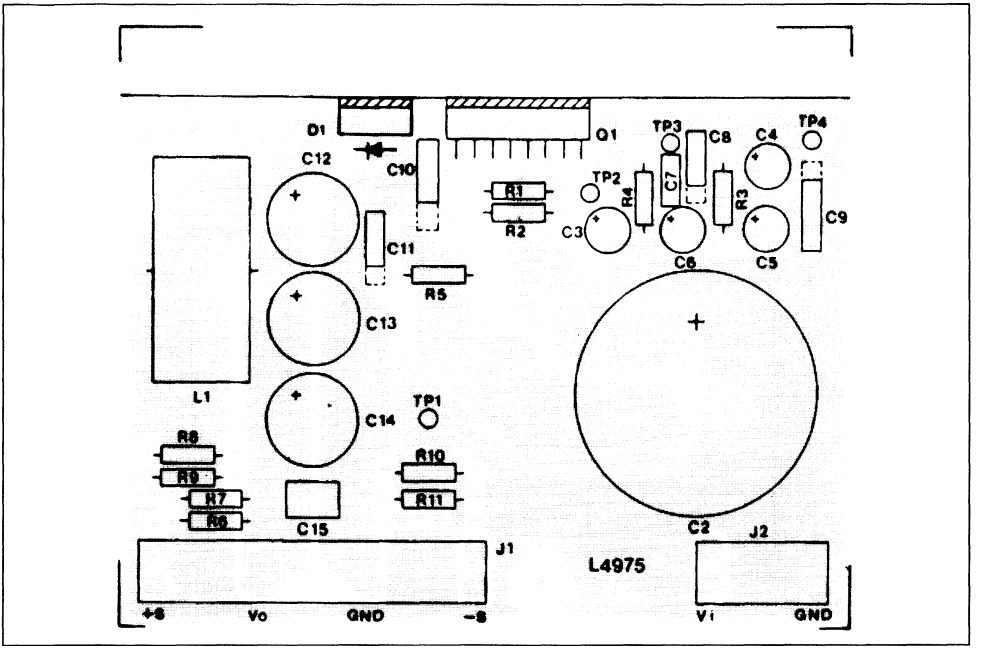


Figure 41: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 39. (1:1 scale)

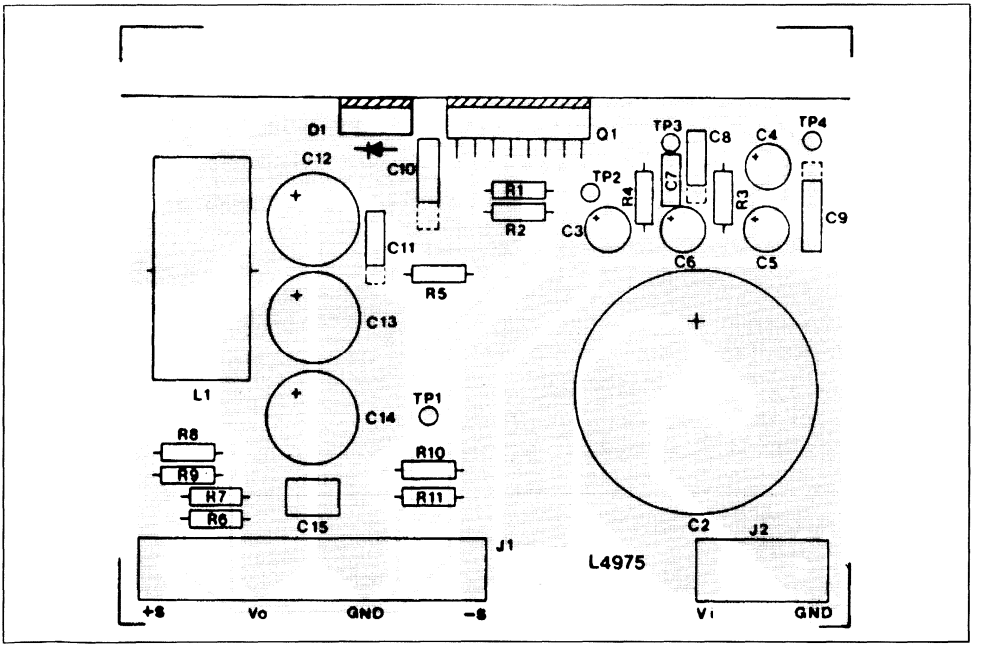
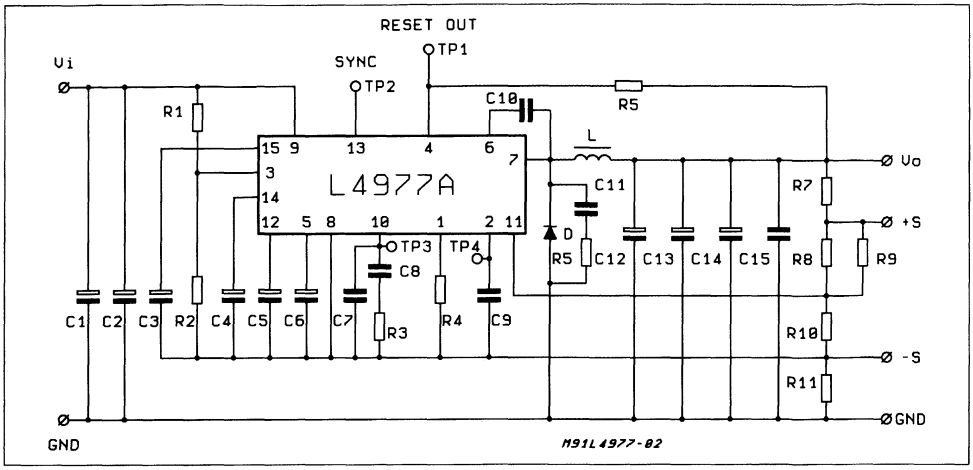


Figure 42: Test and Evaluation Board Circuit



TYPICAL PERFORMANCES (using evaluation board) :
n = 83% (V_i = 35V ; V_o = V_{REF} ; I_o = 7A ; f_{SW} = 200KHz)
$V_{o\ RIPPLE}$ = 30mV (at 7A) with output filter capacitor ESR ≤ 60mΩ
Line regulation = 5mV (V_i = 15 to 50V)
Load regulation = 15mV (I_o = 2 to 7A)
For component values, refer to test circuit part list.

PARTS LIST

R_1 = 30KΩ	C_1, C_2 = 3300µF 63V_L EYF (ROE
R_2 = 10KΩ	C_3, C_4, C_5, C_6 = 2.2µF
R_3 = 15KΩ	C_7 = 390pF Film
R_4 = 16KΩ	C_8 = 22nF MKT 1817 (ERO)
R_5 = 22Ω 0,5W	
R_6 = 4K7	C_9 = 2.2nF KP1830
R_7 = 10Ω	C_{10} = 220nF MKT
R_8 = see tab. A	C_{11} = 2.2nF MP1830
R_9 = OPTION	**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR
R_{10} = 4K7	C_{15} = 1µF Film
R_{11} = 10Ω	
D1 = MBR 1560CT (or 16A/60V or equivalent)	
L1 = 40µH	core 58071 MAGNETICS 27 TURNS Ø 1,3mm (AWG 16) COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Table B
SUGGESTED BOOTSTRAP CAPACITORS

Operating Frequency	Bootstrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 43: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 42. (1:1 scale)

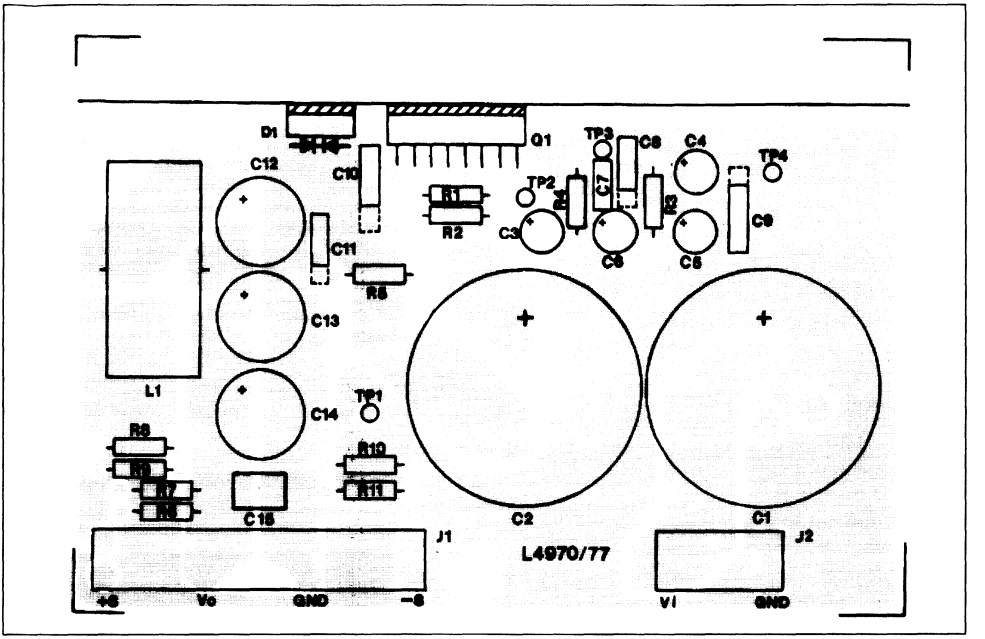
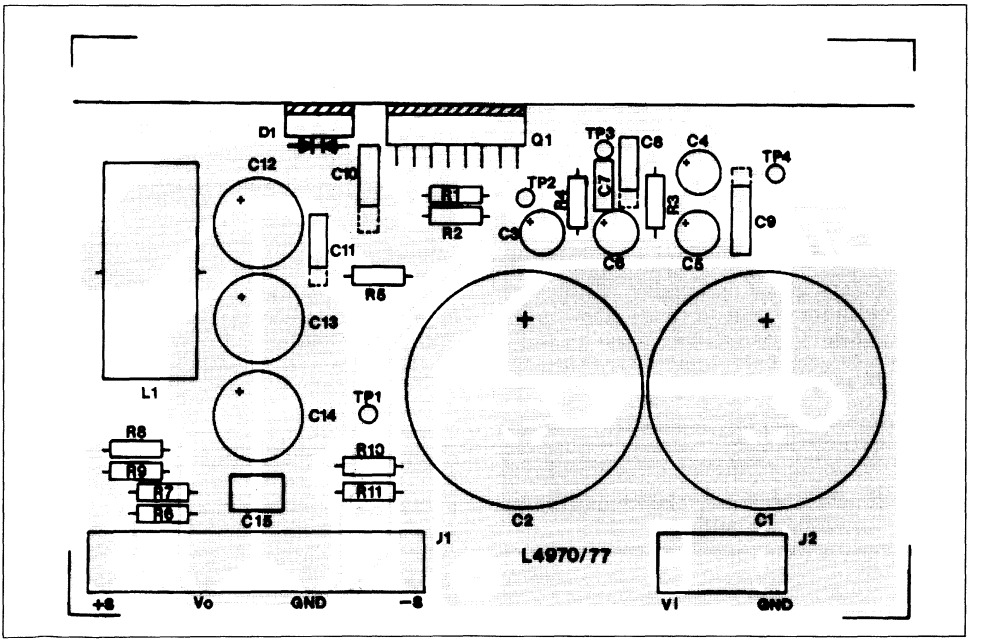


Figure 44: P.C. Board (Back side) and Components Layout of the Circuit of Fig. 42. (1:1 scale)



Resistors value for standard output voltages.

Vo (V)	Rx (kΩ)	Ry (kΩ)
12	4.7	6.2
15	4.7	9.1
18	4.7	12
24	4.7	18

Rx corresponds to R9 for L4974A and L4972A

Ry corresponds to R10 for L4970A, L4977A and L4975A

Rx corresponds to R7 for L4974A and L4972A

Ry corresponds to R8 for L4970A, L4977A and L4975A

The suggested switching frequency, and used in the dynamic tests, is 200KHz for the Multiwatt® package (MW) and 100KHz for the powerdip plastic package (PDIP). The maximum switching frequency allowed is 500KHz.

For the types in plastic package (Powerdip), the lower switching frequency suggested is only depended by the minor dissipating power of a plastic package versus a "power package" because it is well known that switching losses are directly proportional to the commutation frequency.

Higher switching frequencies are possible if limited output current is required and the operating ambient temperature are lower than 70°C. Infact the oscillator of the devices assembled in dual in line is completely equivalent to Multiwatt® package.

Figure 45: Oscillator waveform and sync. pulse for V_i = 35V

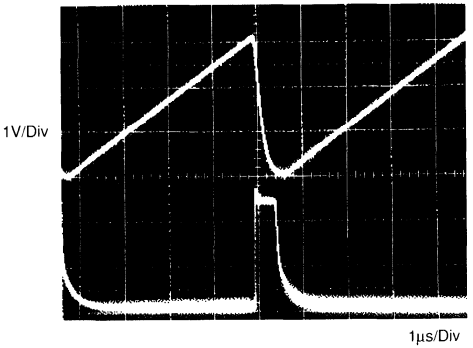


Figure 46: Oscillator waveform and sync. pulse for V_i = 15V

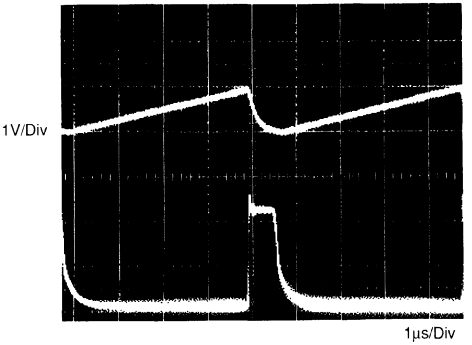
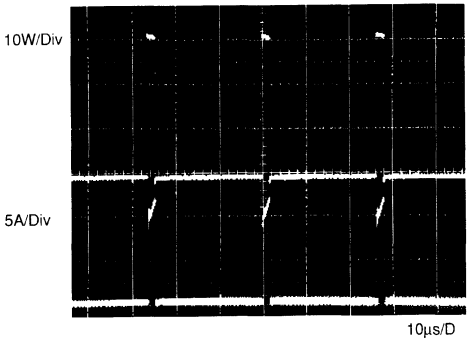


Figure 47: Oscilloscope photograph showing the short circuit output voltage and current waveforms.



The most important external components which need a little more attention (because a properly dimensioning affects on the performance of the application) are the input and output capacitors, the freewheeling diode and the coil.

INPUT OUTPUT CAPACITORS

The output voltage ripple ΔVo, essentially depends on the current ripple in the coil and the ESR of the output capacitor at the switching frequency.

The capacitor that present a low ESR are capable of supporting higher current ripples.

Today, the majority of the constructors of electrolithic capacitors offer in their data book also a wide range of "low ESR" types generally suggested for switching power supply application.

In our case EKR and EKE series (ROE) has been preferred.

Such a series capacitors are designed for applications at high frequency, 200KHz, and built to have a low ESR in order of supporting high current ripple.

In order to minimize the effects caused by the ESR of the capacitors on the output voltage ripple 3 capacitors of 220uF/40V (for high output current application) are connected in parallel.

It is necessary much attention also into the choice input capacitors. Also them be at low ESR, because they must sustain high current ripples. Such current ripples in presents of an inadeguate ESR, would produce a heating of the capacitor itself (which could affect on the reliability of the component, since in general it is sensitive to temperature. Therefore choosing input capacitor at low ESR is necessary for problems of reliability.

In fact such capacitors, when used in applications that make use a mains transformer, must support quite elevated peak current for short periods a double the mains frequency and the same time be capable to deliver the instantaneous peak of energy to the load at the switching frequency.

Some other considerations of a general nature can be done on low ESR capacitors. For example of equal value and type (i.e.: 220µF - EKR), the ESR of the capacitor decreases at the increasing of its value voltage rating, just like its RMS current.

Still, two capacitors of the same value, connected in parallel, withstand an RMS current higher then the only one of double value, and with the same voltage rating.

When however, more capacitors are connected together in parallel, it is important to design with care the layout of the printed circuit, in order to distribute as eventy as possible amongst between the different capacitors the total current ripple. This is used to avoid dangerous current unbalances in the distribution of the total current between the various capacitors charging some more others, that could damage the reliability of the system.

Often it is very difficult to know exactly the RMS current flowing throught the capacitors. To know if the operating condition is a "safe"operating condition or not, a measurement of the package temperature of the capacitor should be done.

The following table 1 and 2, included in the databook of electrical Roederstain, shows the maximum RMS current sustainable by the EKR and EKE capacitor versus the ambient temeperature and overtemperature allowed on the capacitor package.

Table 1.

Low-voltage electrolytic capacitors for switch-mode power supplies with low impedance values, radial, polarized styles.

(EKR)

Rated cap. (µF)	Rated volt. (V DC)	Dimensions D x L (mm) (nominal dimensions)	Dissipation factor tan δ (100Hz; 20°C) Lim. Values	Impedance Z (Ω) (10KHz; 20°C) (Lim. values)	Impedance Z (Ω) (10KHz; 20°C) (Lim. values)	Admissible ripple curr. (mA/100Hz) 85°C	Admissible ripple curr. (mA_{eff}/10-100Hz) 85°C
100	10	8.7 x 12.7	0.12	0.85	0.65	160	250
220	10	10 x 12.7	0.12	0.39	0.31	300	450
470	10	10 x 20	0.12	0.20	0.18	530	800
100	16	10 x 12.7	0.11	0.60	0.40	200	300
220	16	10 x 16	0.11	0.32	0.25	350	550
470	16	12.5 x 20	0.11	0.16	0.13	600	900
100	25	10 x 12.7	0.09	0.5	0.35	250	400
220	25	10 x 16	0.09	0.25	0.17	450	700
470	25	12.5 x 20	0.09	0.13	0.09	650	1000
100	40	10 x 16	0.08	0.4	0.23	450	700
220	40	12.5 x 20	0.08	0.17	0.13	650	1000
470	40	12.5 x 30	0.08	0.09	0.08	1000	1500

(EKE)

Rated cap. (μF)	Rated volt. (V)	Dimensions D x L (mm) (nominal dimensions)	Dissipation factor tan δ (100Hz; 20°C) Lim. Values	Impedance Z (Ω) (100KHz; 20°C) (Lim. values)	Impedance Z (Ω) (100KHz; - 10°C) (Lim. values)	Impedance Z (Ω) (10KHz; - 40°C) (Lim. values)	Admissible ripple curr. (mA)100Hz 105°C
22	10	5 x 11	0.19	1.30	3.90	20	154
33	10	5 x 11	0.19	1.30	3.90	20	154
47	10	5 x 11	0.19	1.30	3.90	20	154
100	10	5 x 11	0.19	1.30	3.90	20	154
220	10	6.3 x 11	0.19	0.60	1.80	9.80	260
330	10	8 x 11.5	0.19	0.33	0.99	5.80	400
330	10	8.5 x 12.5	0.19	0.33	0.99	5.80	400
470	10	8 x 11.5	0.19	0.33	0.99	5.80	400
100	16	6.3 x 11	0.16	0.60	1.80	9.80	260
220	16	8 x 11.5	0.16	0.33	0.99	5.80	400
220	16	8.5 x 12.5	0.16	0.33	0.99	5.80	400
330	16	8 x 11.5	0.16	0.33	0.99	5.80	400
470	16	10 x 12.5	0.16	0.25	0.75	3.20	510
100	25	6.3 x 11	0.14	0.60	1.80	9.80	260
220	25	8 x 11.5	0.14	0.33	0.99	5.80	400
330	25	10 x 12.5	0.14	0.25	0.75	3.20	510
470	25	10 x 16	0.14	0.19	0.57	2.20	635
100	35	8 x 11.5	0.12	0.33	0.99	5.80	400
100	35	8.5 x 12.5	0.12	0.33	0.99	5.80	400
220	35	10 x 12.5	0.12	0.25	0.75	3.20	510
330	35	10 x 16	0.12	0.19	0.57	2.20	635
470	35	10 x 20	0.12	0.14	0.42	1.50	860

Table 2: Admissible ripple current.

Ambient Temp. δ_u in °C	Admissible % of the 85°C value	Surface Temp. in °C	Admissible % of the 105°C value	Surface Temp. in °C
≤ 40	220 %	55	230 %	55
45	210 %	59	220 %	60
50	200 %	63	210 %	64
55	190 %	67	200 %	68
60	180 %	70	190 %	72
65	170 %	74	180 %	76
70	155 %	77	170 %	80
75	140 %	81	160 %	84
80	120 %	84	150 %	88
85	100 %	88	140 %	92
90	90 %	92	130 %	96
95	80 %	97	120 %	100
100	70 %	101	110 %	104
105	60 %	106	100 %	108

CATCH DIODE

Because of quickly rise and fall time of the current (about 40-50ns) the use Schottky diode is reccomanded. Ultra-fast diodes with 30-50ns of trr (reverse recovery time) are not considered sufficiently fast for this family of converters, since they would give too elevated peaks of current at the turn on of the internal power transistor, so high thatcould affect the reliability of the complete system, as well as drastically reduce the efficiency. The oscilloscope photographs show the Output Voltage and Output Current waveforms obtained with diode having different trr value.

Figure 48: Schottky Diode.

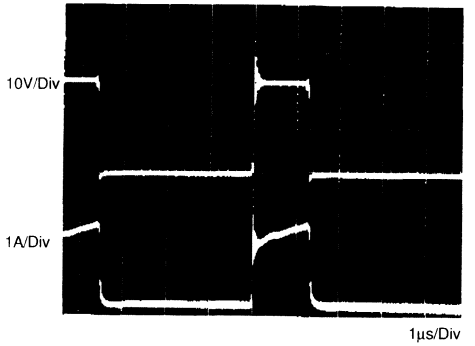
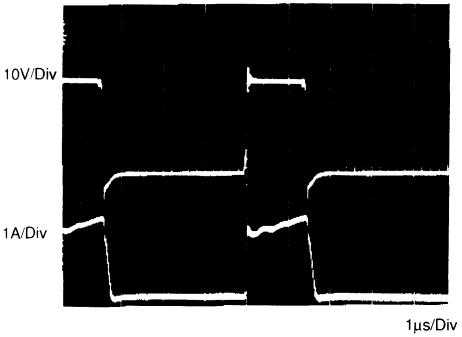


Figure 49: Ultra Fast Diode (trr < 100µs).



In the test circuits used for this family of converters, Schottky diodes from 60V (breakdown reverse voltage) are suggested since the device can support a max. input power voltage of 55V (for specific applications, Schottky diodes with a reverse breakdown voltage higher or equal to the maximum supply voltage should be used), with current rating and packaging to satisfy all the conditions of duty cycle, and therefore also of power dissipation.

COIL

Concerning the coil, a molypermalloy toroidal cores has been suggested, so that it would be easy for everybody to obtain samples, wrap them with a right number of turns in order to evaluate and correlate the measurements and performance of the devices.

In addition since the devices are dynamically tested 100% in production, with a "jig" of testing which uses the same coil suggested in the applications, in the case of contests for example on a guaranteed parameter like the efficiency, should be easier to solve the objections; in this case should be remembered that changing the magnetic material, the dimension, the wire and the number of the winding, also change the losses in the coil reducing the total efficiency of the application.

This can be easily verify using for example toroidal cores in iron powered rather that those suggested in molypermalloy.

Moreover, it is important to dimension properly the coil in order to avoid its saturation, a good choice is to dimension that its saturation; current is not equal to the maximum nominal current capable to deliver to the load, but rather higher by about 20% then the maximum guaranted current of the device, in short circuit condition.

Only in this way it is possible to guarantee that the coil never saturate in all the possible working conditions, i.e.: in presence of a load transient, in short circuit in output and in the case of elevated temperature of the magnetic part.

At last, it should be remembered that the suggested inductors values, are referred to the inductors values that the coil must have at the maximum output current of the application. Oscilloscope Photographs showing the device output voltage and current waveforms obtained with different inductor.

Figure 50: Waveforms for L = 50µH

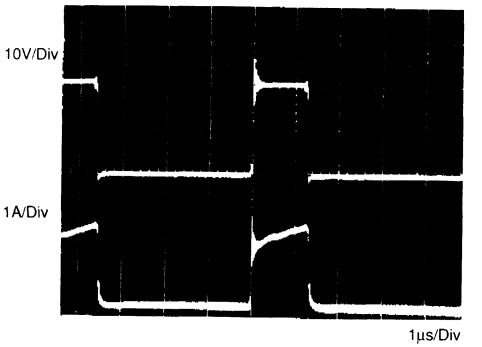


Figure 51: Waveforms for L = 230µH

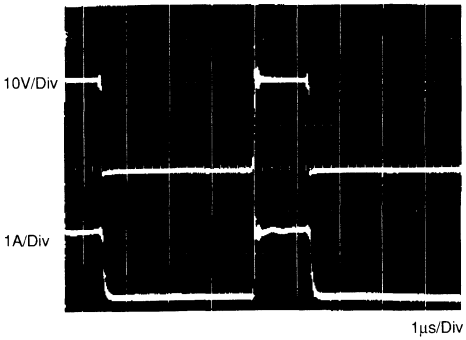
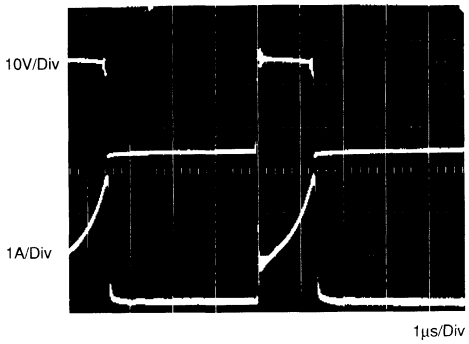


Figure 52: Waveforms for L = 230µH



Anyway some general rules should be observed in order to avoid any "poor functioning". These rules include:

a) the catch diode, that further to be the suggested type in the test circuit, it has to be assembled on the printed circuit very close to the output of the regulator, in order to minimize the leakage inductance and avoid over voltage due to the long connection:

b) The inductor, avoiding the saturation at the maximum current guaranted by the current limitation of the device.

If oscillations on the output voltage at low ambient temperature (i.e.: below 0°C) are originated an output low ESR capacitor has to be used.

Oscillations on the output al low frequency indicate instability of the control loop; in this case a changing of the network compensation is suggested (see Error Amplifier section).

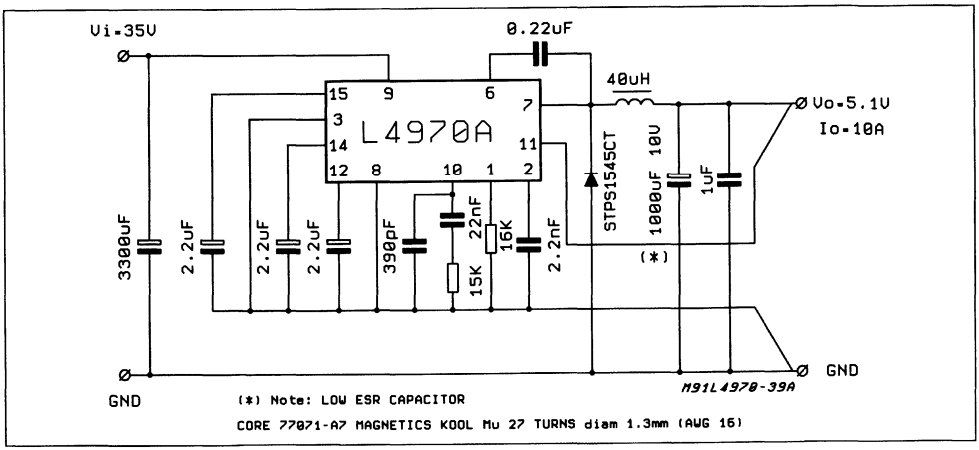
LOW COST APPLICATION

The fig. 53 shows the low cost application of a power supply of 10A and 5.1V.

In comparison of the complete application (and this is valid for all the devices of the family) the external components relative to the reset and power fail functions can be missed.

When a lower output voltage ripple is not required it is possible to eliminate the capacitors connected at the reference voltage pin of 5.1V (i.e.: pin 14 for Multiwatt package. pin 13 for plastic package)
The reset input pin is suggested to connect it to ground.
The soft start capacitor value can be reduced to 100nF for 5v output voltage.

Figure 53: Low Cost Application Circuit.



POWER SUPPLY COMPLETE WITH MAINS TRANSFORMER

The fig. 54 shown a power supply with mains 110/220Vac transformer, diode bridge and filter capacitor with output voltage adjustable between 5.1V. and 24V.

Output capacitors have to be chosen with low ESR in order to reduce the output ripple.Particular care has to be taken for input filter capacitors, in fact they have to support high current spikes at mains frequency and at the same time current peak bigger than the output current at the switching frequency.

Therefore they must be chosen with low ESR and able to substain high current ripple in order to guarantee a good reliability to all the system.

The trasformer can be chosen with a single winding and 4 diodes or a center tap with only 2 diodes with higher reverse voltage.

A cost reduction of the trasformer can be reached using an active power factor corrector.

It work at low voltage and the external components are relatively cheap, more details can be obtained looking on the power factor corrector application note.

POWER SUPPLY WITH MAINS HIGH FREQUENCY PREREGULATOR.

When it is necessary to eliminate the mains trasformer at 50/60Hz for reasons like weight, dimensions or cost, a high frequency preregulator can be used.

A ferrite trasformer reduces the rectifier and filtered mains voltage in a convenient voltage to supply directly the device, providing for the isolation requirements.

Using a free running solution or one of the voltage/current mode controller available, it is possible to compensate the input variation while the output voltage variations due to the load are usually very low. Some examples regarding how to use this regulator in off-line power supply are now showed:

Flyback Topology

Using a flyback topology with single or double transistors is possible to fix a single output voltage of 35-40V; it can be a bit increased if using a backup battery of 48 nominal Volts.
From this preregulator (±10%) tolerancevoltage is possible to get one or more indipendent outputs, with its own current limitation and thermal protection.

Moreover a possibility to syncronize more devices together is available, remembering to fix the master frequency at least 5% higher than the others device (working as slave) one.
In case of necessity is possible to synronize devices on the trasformer secondary with the swithcing frequency of the controller (See Fig. 55).

Figure 54: Typical power supply showing the mains transformer.

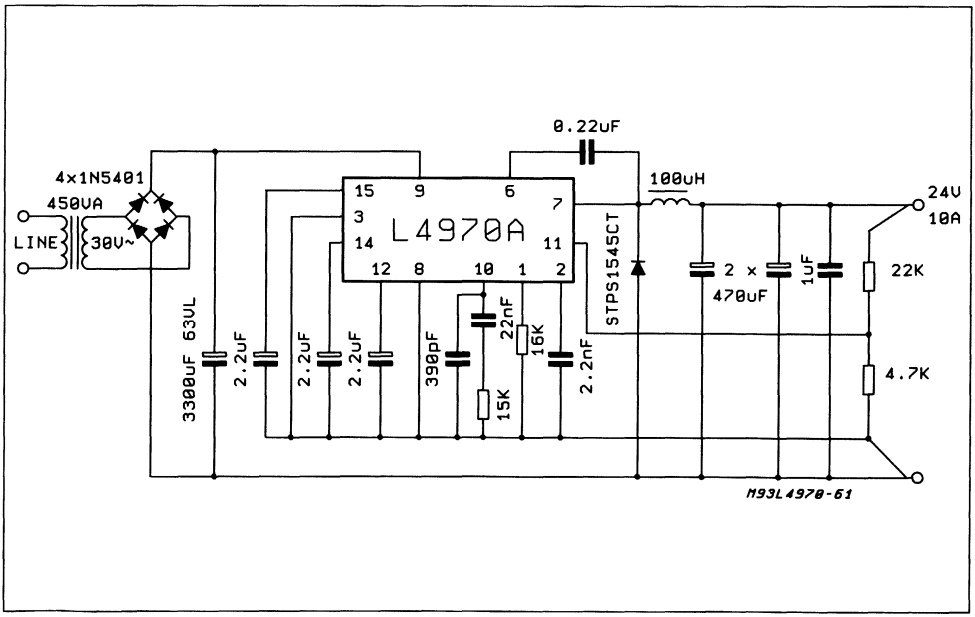
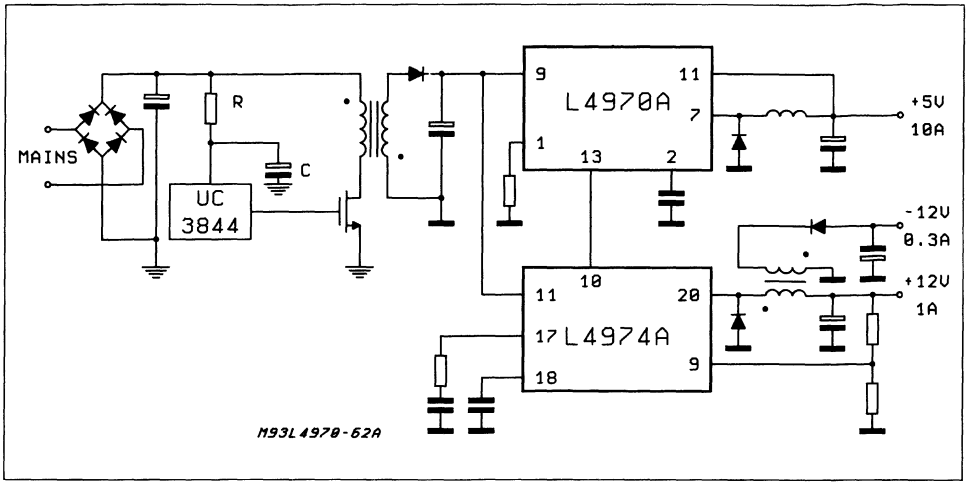


Figure 55.



Forward Topology

Further is showed an smps forward circuit, where the dc-dc converter is used as post-regulator for an auxiliary output, (35V.) while the main one (5.1V. or 3.3V) is controlled directly with the feedback (See Fig. 56).

Using a PFC preregulation

When an optimized power factor is required it is possible to use the following two pricinple diagram that make use of an active power factor corrector.

1) using the standard boost topology (Fig. 57)
2) using a flyback topology (Fig. 58)

The idea is that to generate a stabilized voltage, around 30V - 35V, already isolated, avoiding to use an isolation after the PFC section.

Figure 56.

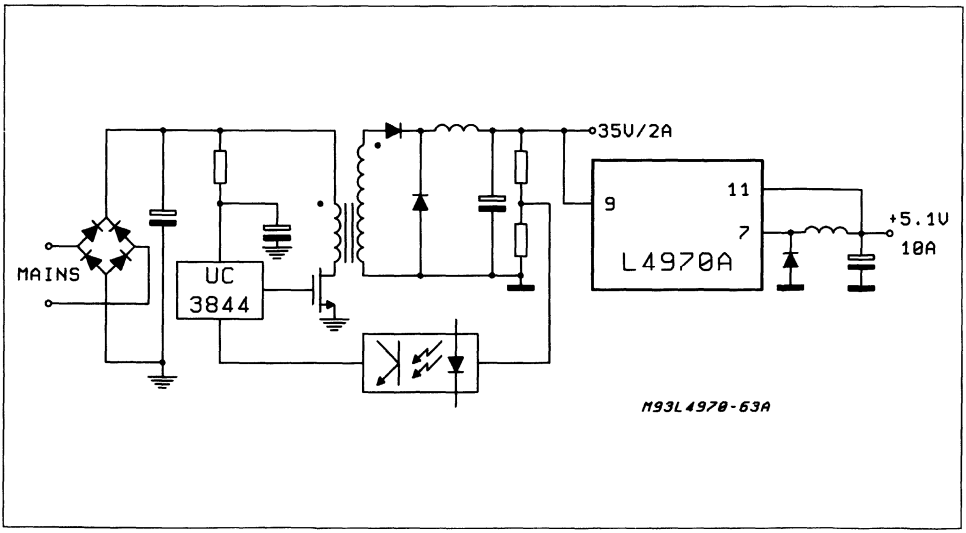


Figure 57.

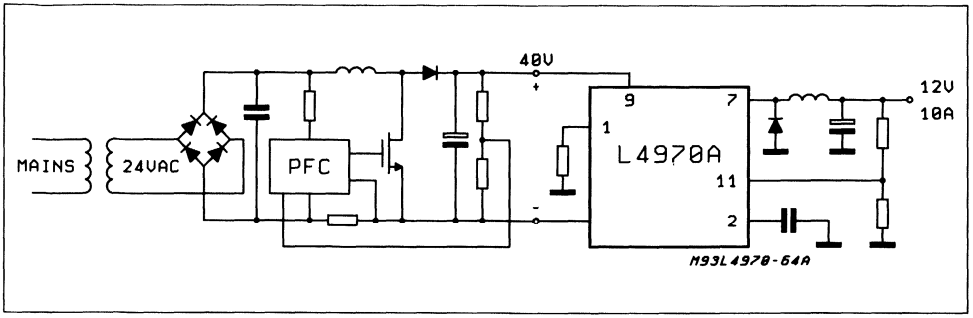
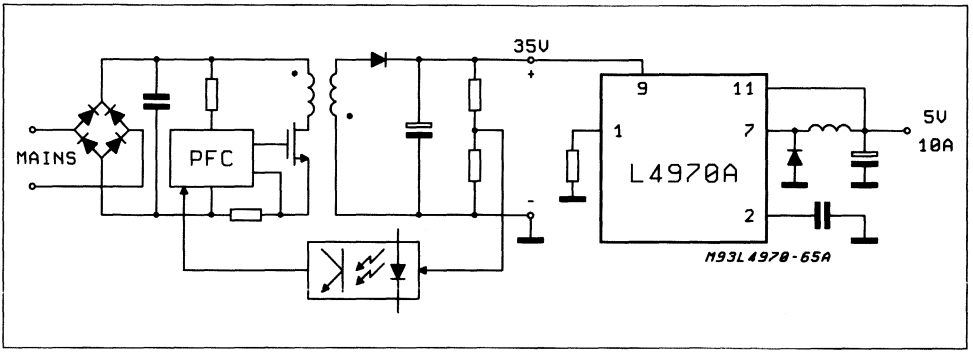


Figure 58.



POWER SUPPLY WITH 0 TO 25V ADJUSTABLE OUTPUT VOLTAGE

a) It is a classical solution with high performance that make use of a negative reference voltage equal to the value of the internal voltage of the device (5.1V).

To generate this negative reference voltage, it is useful to equip the mains trnsformer with another secondary winding at a low voltage of around 8Vac and capable of delivering a few dozen of mA.

During the phase of starting up and stopping of the mains, it is important to avoid generating oscillations around the value of the output voltage , including the zero voltage.

For this reason a network consisting of two NPN signal transistors TR1 and TR2 and some resistors has been introduced.

The transistor TR2 remains is saturation when TR1 is off, untill the output voltage of the negative regulator reaches 4.3V

At this point TR1 goes in saturation, sending off TR2. In this way the soft start is blocked and the device begins to work starting in soft start.

Switching off the mains voltage, the regulator generating the negative volatge is still in regulation when the input voltage of the switching converter has already dropped below the turn on threshold.

Carefull attention must be given therefore to calculate the input capacitor of the two sections in order to avoid possible malfunctioning during the turning on and turning off.

b) a solution that presents a cheaper costs and tha doesn't use a negative reference voltage is the following:

Setting the cursor "P" to the adjustable resistance at 0V, using R1 and R2 the maximum output voltage can be fixed.

In this case we set R1 = 24Kohm and R2 = 4K7ohm.

In R1 the maximum flowing current will be limited at 1mA; with 1mA flowing in R1, Vo = 30V.

Now by reducing the current in R1 the output voltage Vo can be adjusted till to 0V.

Figure 59: 10A Switching Regulator, Adjustable from 0V to 25V

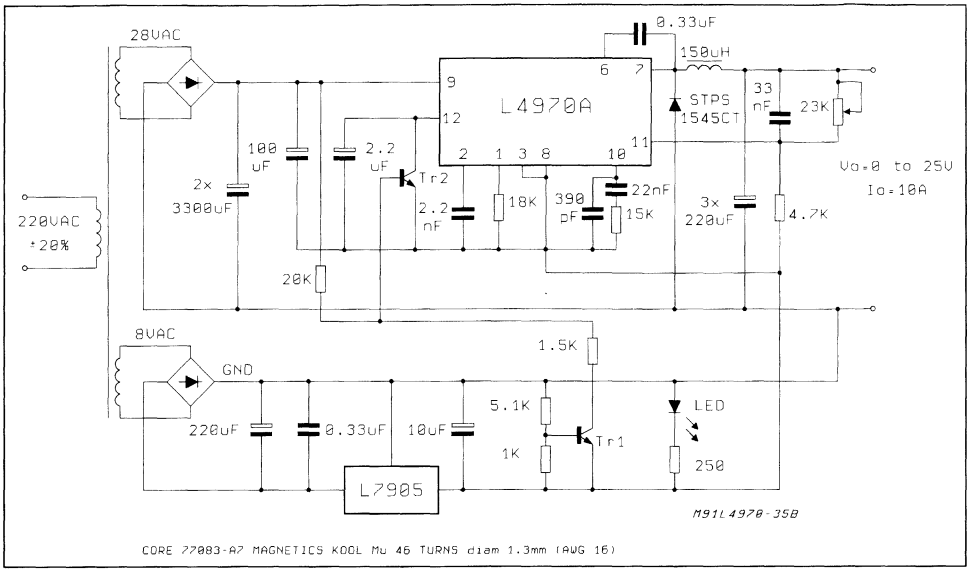
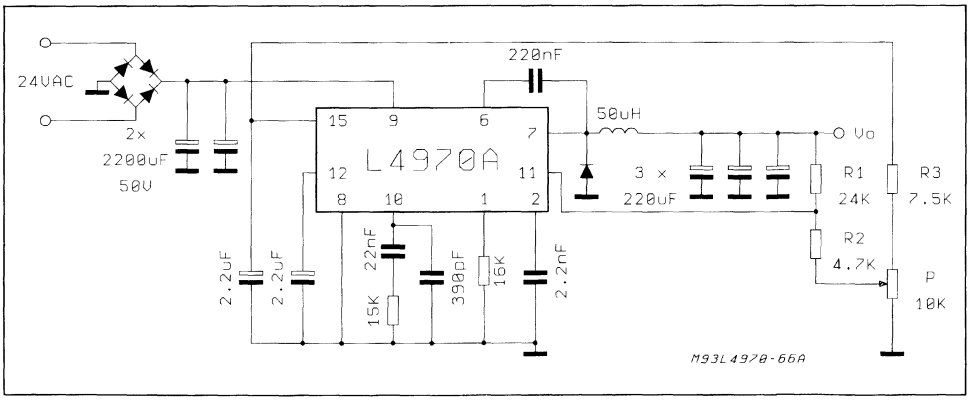


Figure 60.



The current, flowing in backward, to have 0V it will be:

$$I1 = \frac{V_{ref}}{R1} = \frac{5.1V}{24K} = 0.21mA$$

$$\Delta V_{R2} = R2 \cdot 0.21 = 4.7k \cdot 0.21 = 1V$$

Therefore, when the cursor "P" reaches Vref + 1V the output voltage goes to zero.

At this point we are able to define as well the values of P1 and R3.

When the "P" cursor is completely moved to high, there should be 6V of dropping to "P", and in this way 0.6mA will flow.

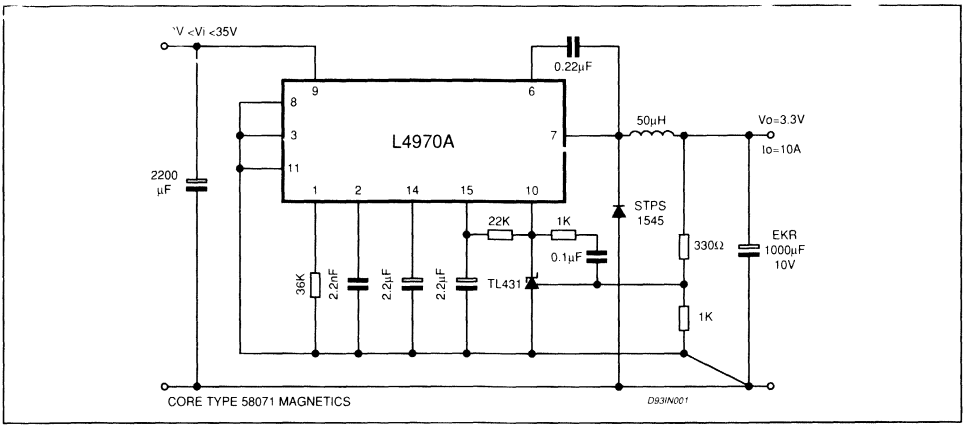
The current flowing in R3, considering that the voltage at pin 15 has a typical value of 12V, it will be of 0.8mA.

In this case the R3 value will be 7K5ohm.

3.3V / 10A DC-DC CONVERTER

When an output voltage lower to the reference voltage of 5.1V must be stabilized with a good result from stability and regulation point of view, and

Figure 61.



not having available the not-inverting input of the error amplifier, it is possible to use an external reference.

In this case a TL431C reference has been chosen, which is cheaper and widespread used.

In this case more than a simple reference, it is a true shunt regulator, containing a reference, an error amplifier and a transistor capable of absorbing a max current of 100mA.

Such component can be compensated like a common OP/AMP, and therefore in our application can substitute both the internal reference and the error amplifier.

The fig. 61 represents the electrical diagram of the application at 3.3V.

The operating input voltage is between 12V (due to the internal UVLO) and 35V, with a minimum operating switching frequency of 100KHz.

The maximum operating input voltage is limited only 35V because the minimum "ON" time, which should not be reduced below 1 microsecond.

At input voltage of 35V, output voltage of 3.3V and fs=100KHz the Ton time is already about of 1 microsecond.

Infact we have:

$$V_O = V_i \frac{T_{on}}{T} \quad \text{therefore:} \quad T_{on} = \frac{V_O}{V_i} T$$

The inductor can be calculated using the usual formula, that is:

$$L = \frac{(V_i - V_o) \cdot V_o}{V_i \cdot \Delta I_L \cdot fsw}$$

with ΔI_L = 10% I_{omax}, L = 30µH

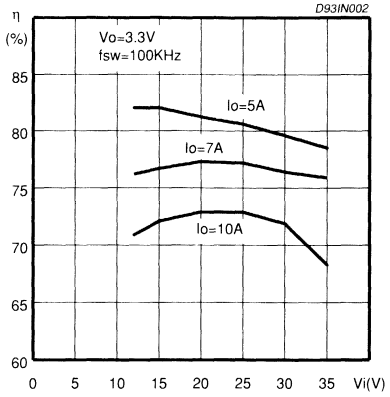
When one operates with input voltage below of 5V, it' very difficult to obtain a good efficiency. In our case having the conduction losses and switching losses of the internal power transistor fixed by both external operating electrical condition and the electrical characteristics of the itself power transistor, since integrate, it's necessary to optimize the losses of the catch diode, using new type at lower forward voltage drop, as soon as available on the market or by appropriately overdimensioning.

In some case a Power MOS used as a synchronouos switch can contribute to elevate the overall efficiency of the system.

Following are citated the principle results obtained by using our evaluation board:

The same solution, obviously can be applied also to the other types of the family, adjusting if needed the compensation network and the coil.

Figure 62: Efficiency vs. Input Voltage



Efficiency vs. Input Voltage

V_i (V)	I_o = 10A η%	I_o = 7A η%	I_o = 4A η%
12	70.9	76.2	82
15	72.1	76.7	82
20	72.9	77.3	81.2
25	72.9	77.2	80.6
30	71.9	76.4	79.6
35	68.3	75.9	78.5

Figure 63: Load Transient Response

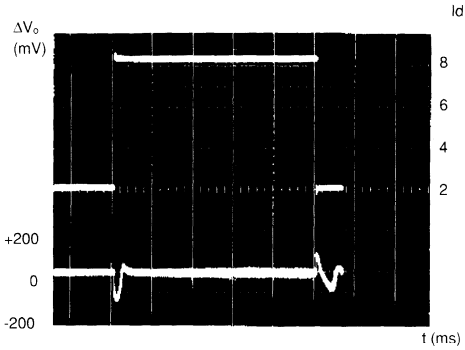
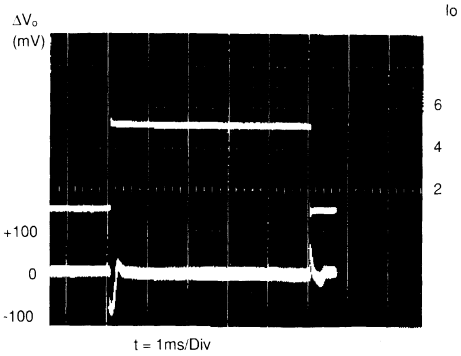


Figure 64: Load Transient Response



Output voltage ripple vs inductor value.

C_o = 1000µF/10V - EKR; ESR = 10mΩ

L	L = 30µH	L = 50µH	L = 60µH	L = 100µH
ΔV_{Omax}	80mV	60mV	40mV	25mV

CURRENT GENERATOR

Often it is required to generate constant current , fixed or adjustable, for various applications, such as chemical process, lamp powering, battery charger for lead acids, ni-cd and ni-me-hyd batteries.

Figure 65: Constant Current Generator and battery chargers.

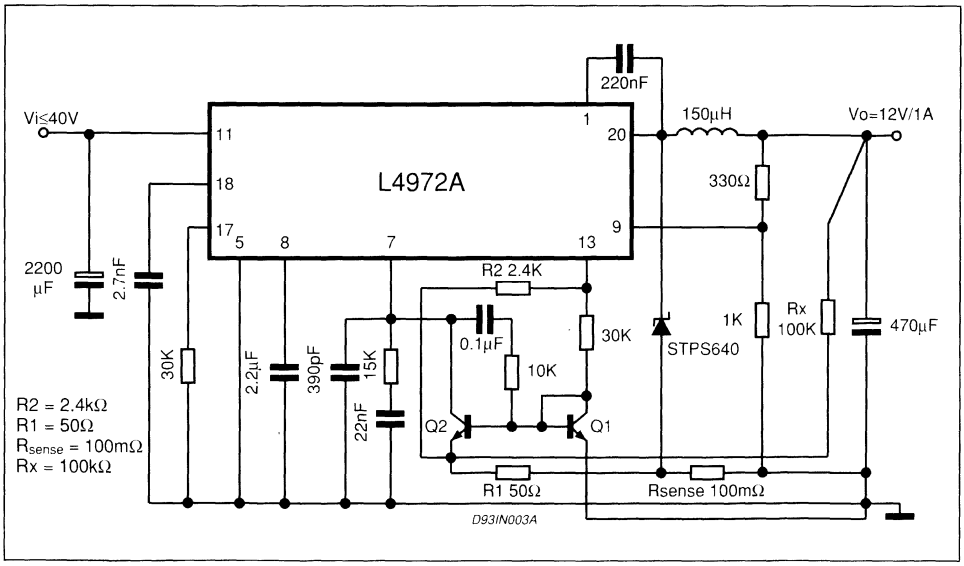
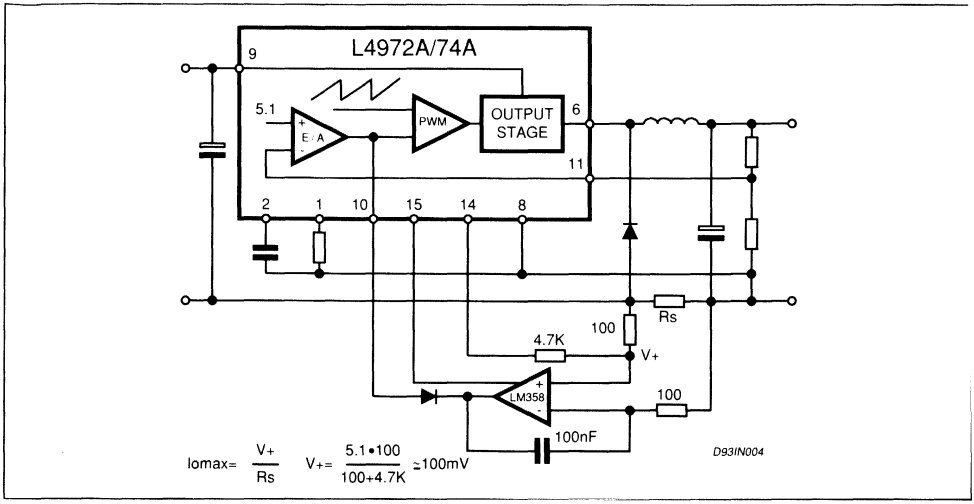


Figure 66.



In this paragraph some suggestions will be given for how to abtain generators of constant current, more or less sophisticated according to the need.

The examples given are time by time applicable to the different devices of this family of regulators, with the necessary adjustement according to the current required by the application.

The diagram of fig. 66 propose a simple solution that makes use of two esternal small signal-transistor best if matched in Vbe, and some other passive components. For a cost reduction Q1 can be substitute by a simple diode 1N4148.

The divider composed by R2 and R1 fixes a voltage at the whished voltage value (for example 50 -100mV) on the Q2 emitter.

Q2 will be reversed bias untill the emitter voltage of Q1 will raech the same value as itself.

At this point Q2 will be direct bias and will begin to absorb current from its collector; in the moment in which Q2 will enter into conduction, a variation ΛVsc at the current sense resistor will give a variation of the Q2 current equal to:

$$\Delta I_{CQ2} = \frac{\Delta V_{SC}}{R1}$$

When the current absorbed by Q2 will reach the maximum current delivered by the error amplifier output (or by the current of the soft-start if this pin is prefered to use), the error amplifier will fall out of regulation and its output voltage will begin to decrease reducing, conseguentely, the duty cycle; then the regulator will begin in this way to behave as a generator of current instead of voltage. The emitter voltage of Q2 is fixed by the following formula:

$$V_{EQ2} = \frac{V_{REF}}{R1 + R2}\ R1 = 5.1V\ \frac{R1}{R1 + R2}$$

A general criterium, is that of fixing the divider "R1R2" in such way as to make a current flow that is greater than the necessary lowering the outputvoltageoftheerroramplifier.

The maximum current delivered by the output of thetransconduttanceerroramplifieris200μA; the current that has to flow in the divider R1R2 should be around of 2-3mA to have a very precise intervation or around only 1mA for slightly more soft interventions.

By varying the value of R2, the point of intervention of the current limitation will be moved.

The resistor Rx contributes to introducing a more or less accentuate foldback effect, on the output current.

In the following table suggest a few values of Rsense according to the nax output current.

R_{sense} (mΩ)	I_o (A)	Device
10	10	L4970A
15	7	L4977A
30	5	L4975A
50	3.5	L4974A
100	2	L4972A

The criterium used to defined the value of the sense resistor is essentially tied to the max power dissipated by the resistance, as well as to the market availability.

If the mains objective is to maximize the efficiency

when (delivering for example 10A), it is convenient to use two current transformers instead of a dissipative resistor, one in series to the source of the internal DMOS and one in series to the catch diode.

Using such solution, a quite simple and fine regulation of the current is possible to implement.

Figure 66 shows a current generator solution with high precision on the current, using an op/amp instead of two small signal transistors.

Higher input voltage.

Since the maximum operating input voltage of this family is 50V, when one of these devices must be supplied with more elevated voltages, it is necessary to introduce a preregulator.

Fixing the output voltage of the preregulator of 45V, the power dissipation of the preregulator is:

$P_d = I_i \cdot V_{CE} \cdot = I_i \cdot (V_i - 45)$

In the buck converter, the average input current is:

$$I_i = I_o \cdot \frac{T_{on}}{T} = I_o \cdot \frac{V_o}{V_i}$$

DESIGN EXAMPLE FOR L4974A

(a)	(b)
Vo = 5.1V Io = 3.5A Po = 17.85W	Vo = 12V Io = 3.5A Po = 42W
Ii = 0.388A	Ii = 0.933A
With an operating input voltage of 60V the preregulator will dissipate:	
Pd = 5.82W	Pd =13.4W
The overall efficiency will be:	
n = 68%	n = 70%

Up Down Converter

In some applications it is required to stabilize a voltage starting from an input voltage which can be lower or higher then the output regulated voltage.

In this case a well known buck-boost topology is suggested.

The fig. 68 which shows the electrical diagram of the up-down converter, makes use of the L4974A to generate an output voltage of 12V at 3A.

For output current lower or higher than 3A other devices of this family can be used. For input voltage less than 20V the zener diode can be avoided.

Such circuit can also be used as a simple step-up. In this case there is a structure of the "asymmetrical two transistor converter" type, that in the case of a short circuit is automatically protected since the internal transistor turn-off, disconnecting the power supply.

This doesn't happen in the classical step-up converter topology, in which, during the short circuit only the power transistor is protected, but the current in the coil and the freewheeling diode is not limited.

Negative Output Voltage

Often it becomes necessary, in the multioutput power supplies, to generate negative voltages with current higher than 1A maintaining an elevated efficiency of the system.

Such outputs must have a good precision and stability and must be protected from short circuiting.

With the application circuit suggested below, one the aime is to satisfy the performance listed above, and to contributing to the simplification of

Figure 67: Design Example for L4974A

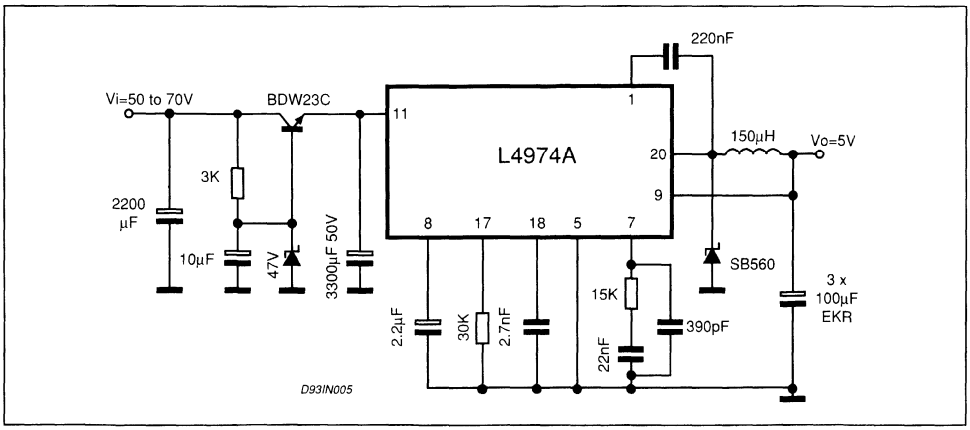


Figure 68.

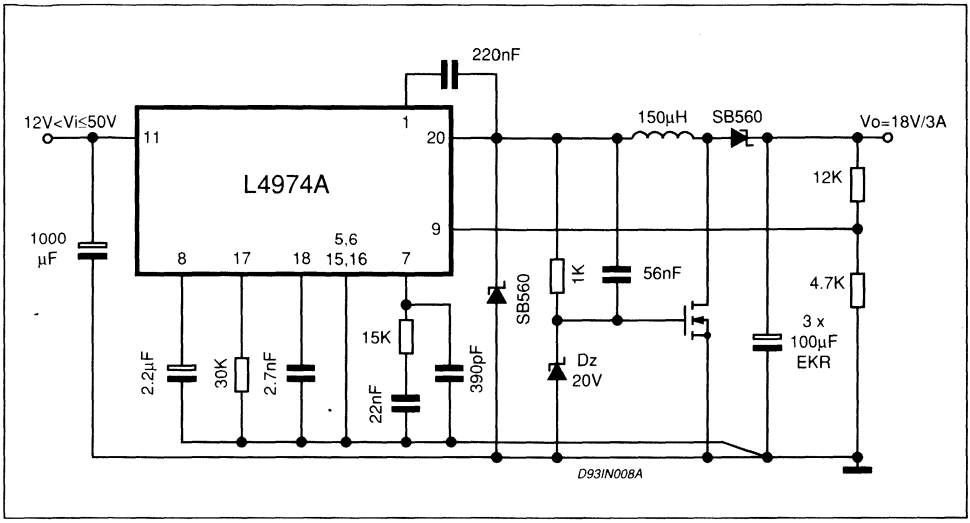
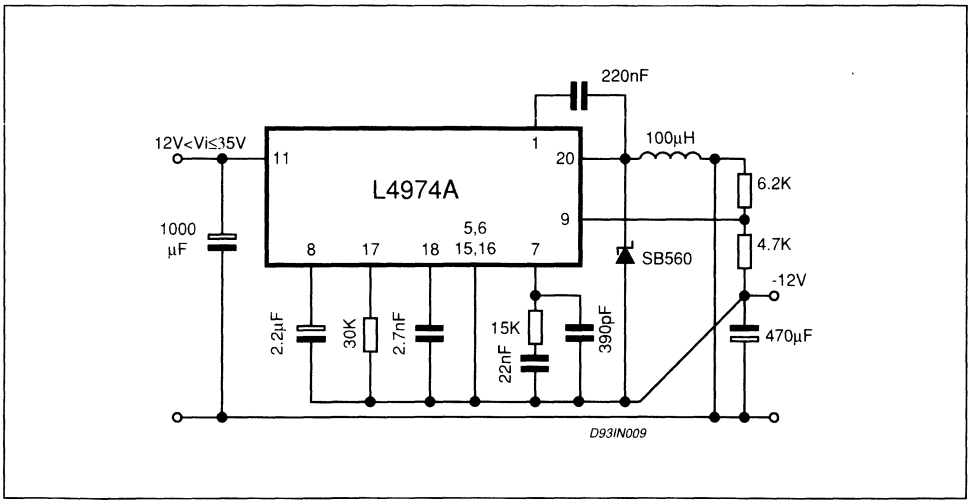


Figure 69: Circuit for negative output voltage



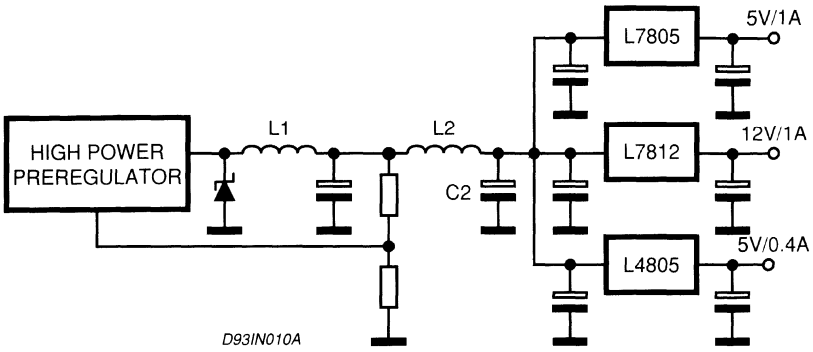
the power trasformer, both at 50Hz and at high frequency.

It's important to remember not to exceed the absolute maximum voltage ratings of the device. In this case the differential voltage applied to the device is the sum of the maximum input voltage (positive) and of that controlled output negative.

Linear low drop post regulation

In some application it becomes necessary to generate stable, precise fixed or adjustable output voltages at high efficiency and with a truly negligible output ripple. Summarizing a regulator that offers the quality of a linear type of control with the efficiency of a switching regulator. The fig. 70 shows the diagram of a swithcing preregulator at high efficiency followed by one or more series regulators of the type very "low drop", or in the case of elevated current, by a discret low drop solution.

Figure 70.



L2 and C2 are necessary to reduce the switching frequency spikes

LAYOUT CONSIDERATIONS

Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path lenght becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to output pin, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig 71 shows the structure of a power device. As demonstrated in thermo-dynamics, a thermal circuit can be considered to be an electrical circuit where R_1, R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 72).

C1, C2	are the thermal capacitance (expressed in °C/W).
I	is the dissipated power.
V	is the temperature difference with respect to the reference (ground).
This circuit can be simplified as shown in fig. 74, where:	
C_C	is the thermal capacitance of the die plus that of the tab.
C_h	is the thermal capacitance of the heatsink
R_{jc}	is the junction case thermal resistance
R_{th}	is the heatsink thermal resistance

Figure 71.

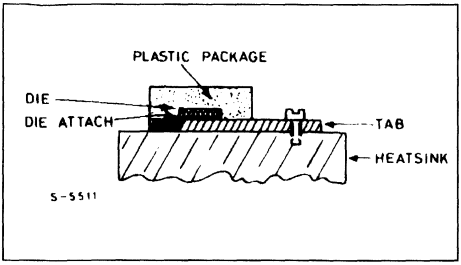


Figure 72.

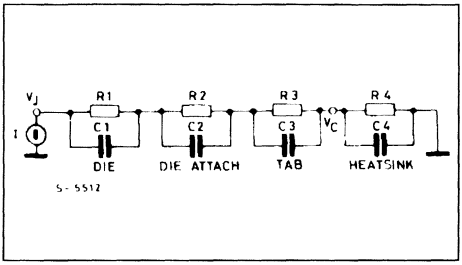
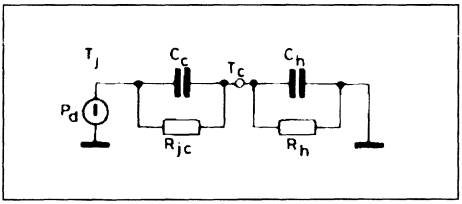
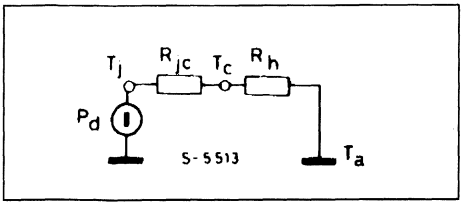


Figure 73.



But since the aim of this section is not that of studing the transistors, the circuit can be further reduced as shown in figure 74.

Figure 74.



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_{th})\, P_d \qquad a)$$

$$R_{th} = \frac{T_j - T_a - R_{jc}\, P_d}{P_d} \qquad b)$$

$$T_C = T_a + R_{th}\, Pd \qquad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5°C/W;; with silicone grease roughly 0.3°C/W and with silicone grease plus a mica insulator about 0.4°C/W. See fig. 75. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperature can be calculated by solving the circuit shown in fig. 75. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig.77 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 77 refers to specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Figure 75.

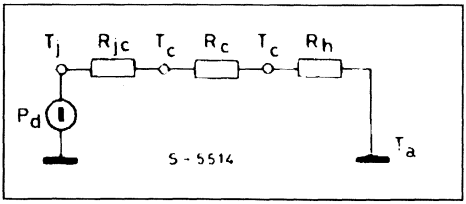


Figure 76.

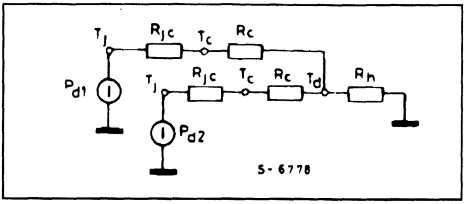


Figure 77.

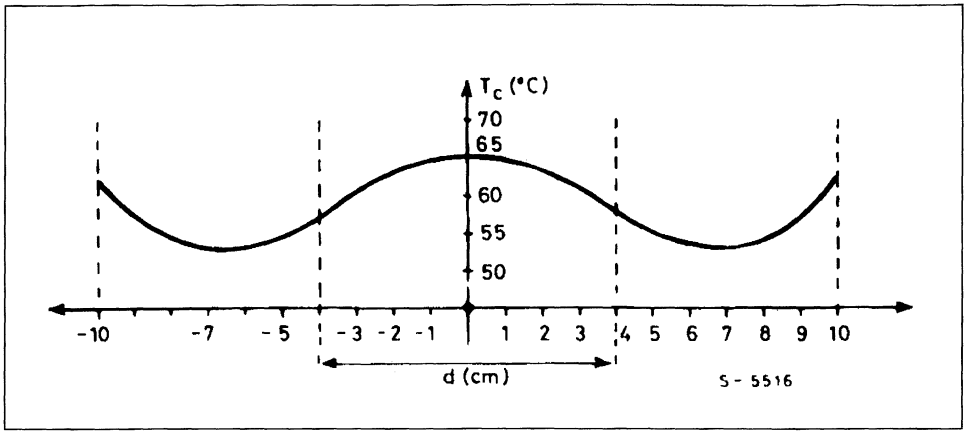


Figure 78.

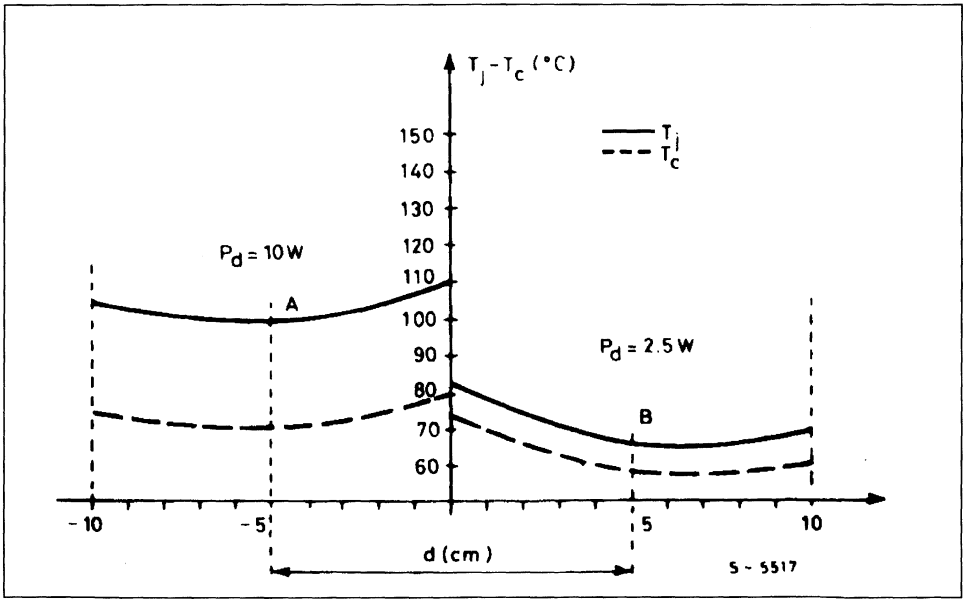


Fig. 78 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in applications with two devices in MTW package are synchronized.

REFERENCES:

1) ***AN244*** *"Designing with the L296 monolithic power switching regulator" (Ref. Designer' Guide to Power Products Application Manual).*

2) ***Table1*** *(see page 31-32/46) – EKR & EKE Roederstein Low Voltage Electrolytic Capacitors.*

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING WITH THE L4963 MONOLITHIC DISCONTINUOUS MODE POWER SWITCHING REGULATOR

by M Roncoroni

The L4963 is a new switching regulator designed to operate in discontinuous mode, reducing the number of the external components, giving a very cost effective solution. This application note explains how the device operates and how it can be used. Typical application circuits are also described.

The L4963 is a new monolithic stepdown switching regulator IC operating in discontinuous mode. This device, able to deliver 1.5A to the load at a voltage of 5.1V and up to 36V with derated current, is designed to satisfy very low cost applications due to the fact that the number of the external components are dramatically reduced.
Moreover the inductor value is reduced by a factor of three or four in comparison with a corresponding continuous mode solution. Also the plastic package (Powerdip 12+3+3), that needs no heatsink, contributes to decreasing the cost of the overall application.

Although the L4963 is intended for very low cost applications, it integrates features like remote inhibit, reset and power-fail outputs for microprocessor.

In the following we will explain in detail its principle of operation and the criteria that regulate the choice of the external components.

CIRCUIT OPERATION

The L4963 operates in discontinuous mode. In principle in this kind of operation the energy stored in the inductor is fully discharged to the load before to start a new cycle.
To operate in this way, the device contains, in its regulation loop, additional blocks compared to the usual Error/Amplifier, Oscillator and Pulse Width Modulator used in the continuous mode devices.

Figure 1: L4963 Block Diagram

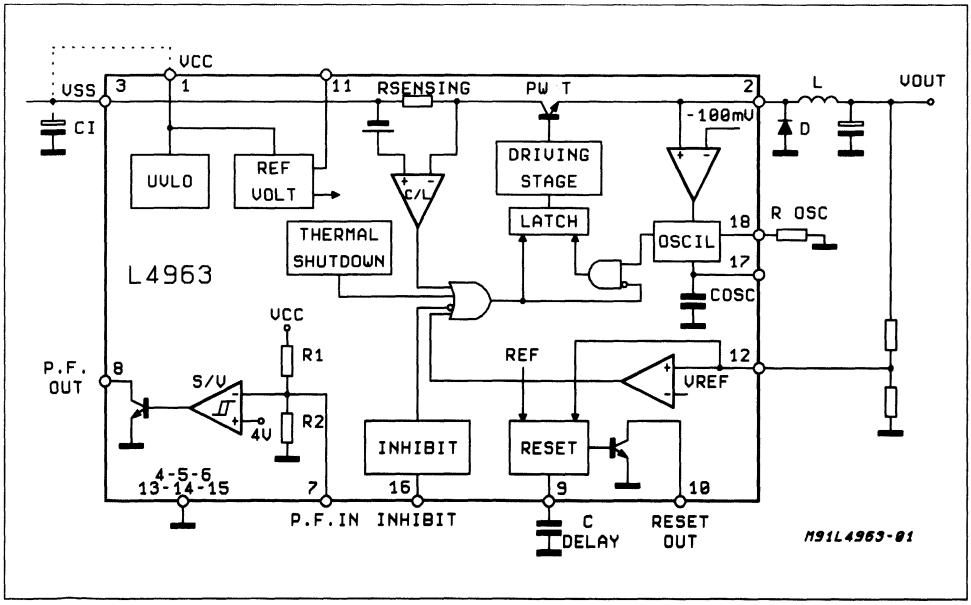
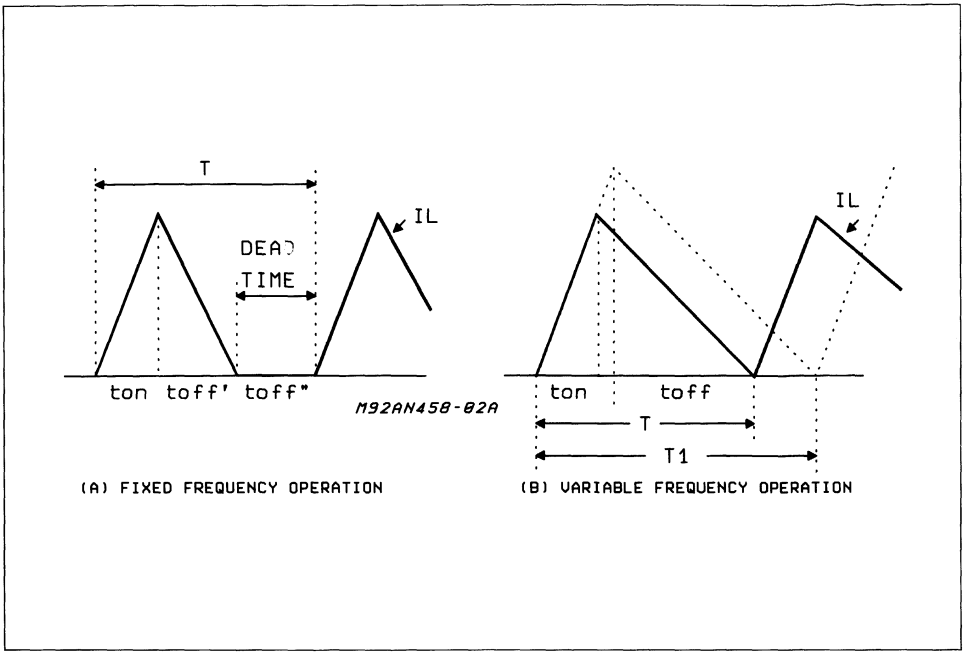


Figure 2: Waveforms



The L4963 control loop is shown in the block diagram of fig.1 and the blocks that take part to the regulation loop, are determined by the system operating conditions.

For a given value of the inductor L (that will be further calculated), if we examine the current across the inductor (I_L), we can have two different situations that modify the device operation. This two different conditions depend on the load current value that device has to deliver: changing the load current (I_O), the current through the inductor can have one of the shapes shown in fig. 2.

In both the waveforms, the current in the coil goes to zero during the T_{off} period of the power stage, but in the case shown in fig. 2A there is a "Dead Time" during which, both the Power stage and the Free-Wheeling diode are not conducting. The dead-time period ("T_{off}") increases lowering the load current. The system will start with a new cycle at the next set pulse coming from the clock. In this way the system operates in fixed frequency mode, set by the External resistor RT connected between pin. 17 and ground.

In fixed frequency mode, the current in the inductor reaches the peak value, determined by the load current, following the law:

$$I_{L+} = \frac{V_{in} - V_{cesat} - V_{out}}{L} \cdot t_{on} \quad (1)$$

When the output voltage reaches its nominal value, the E/A output resets the power stage and the discharge period starts.

When the power transistor turns off, the inductor will try to mantain the forward current constant, and the voltage at pin.2 will fly negative until the diode D is brought into conduction. The current in the inductor L will now continue to circulate in the same direction as before, decreasing linearly from the peak value to zero following the law:

$$I_{L-} = I_{peak} - \frac{V_{out} + V_F}{L} \cdot t_{off} \quad (2)$$

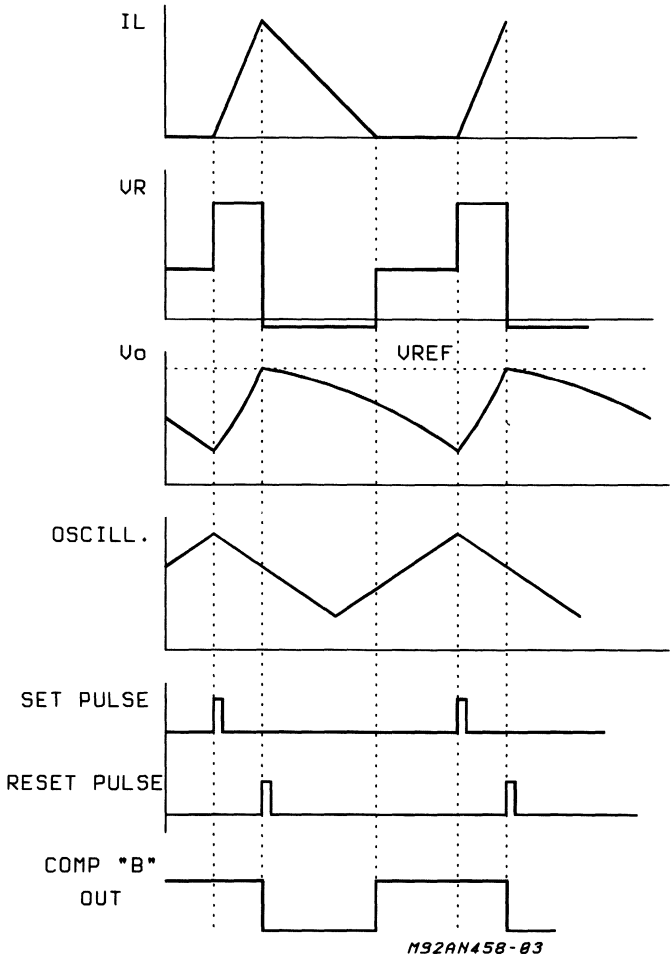
It follows, then, a third period $t_{off"}$ (dead time) during which there is no current neither across the power transistor, nor in the diode D, nor in the inductor L (the inductor runs 'DRY'). This period ceases when the next set pulse from the clock circuit enables again the power stage repeating the cycle.

The operation frequency is equal to the clock frequency, that is determined by the resistor R_t, connected between pin. 17 and ground:

$$f_{osc}\,(KHz) = \frac{0.033}{R_t\,(K\Omega)}$$

In fig.3 are shown the voltage and current waveforms associated to this mode of operation.

Figure 3: Fixed Frequency Operation



Referring again to the block diagram in fig. 1, and with a given inductor L, we suppose to have a load current that reduces the Dead Time toff" to zero. At this point we suppose that the clock send a set pulse to the latch and the power stage turns on. The current in the inductor grows from zero up to its peak value ($I_{peak}=2I_{out}$) following the law stated in Eq. 1.
If the peak current is below the Current Limitation threshold, it is again the Error Amplifier that turns off the power stage and the inductor will discharge following the eq. 2.
If the system is not able to discharge completely the inductor during the maximum toff time allowed by the fixed frequency operating mode an internal comparator, (which compares the voltage on the free-wheeling diode cathode with a precise internal reference Vr = -100mV) will mantain the power stage off until the inductor will be completely discharged.
This comparator prevents the discharge of the internal timing capacitor C_t, until the Energy in the inductor is completely discharged and the diode D ceases to conduct (see fig.4).

The system is working in a variable frequency mode, with a switching frequency that is depending on the current delivered to the load.
Bigger is the load current higher is the stored energy and longer is the time during which the comparator will block the discharge of the timing capacitor C_t, decreasing the system operating frequency. In fig.4 are shown the waveforms associated with this mode of operation.

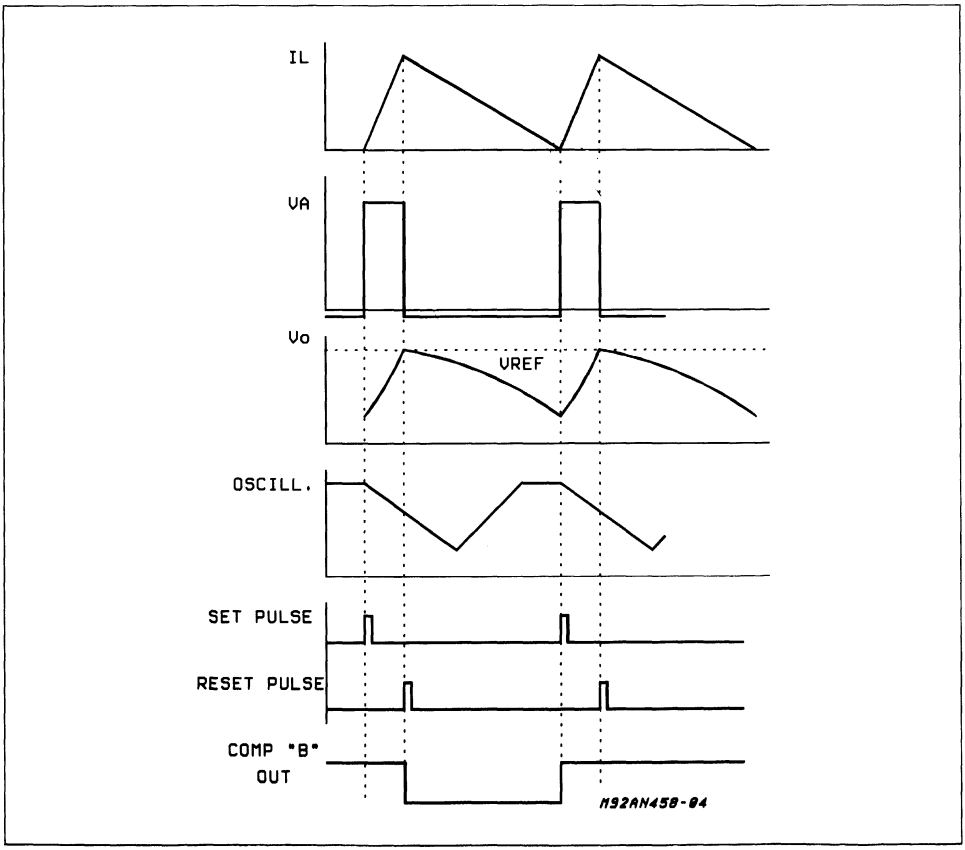
CALCULATION OF THE INDUCTANCE VALUE, L

To calculate the inductance, that is a critical element in the circuit, we have to consider that:

- The switching frequency increases reducing the load current I_{out} and increasing V_{in}.
- The switching frequency decreases increasing the load Current I_{out} and decreasing V_{in}.

So to calculate the inductor value we have to

Figure 4: Self-oscillating Operation



specify the minimum operation frequency (higher than 20KHz to avoid audible noise), for the minimum input voltage V_{in} at full load.
The equation to calculate the maximum inductor value is:

$$L \leq \frac{(V_{in(min)}) - V_{cesat} - V_o) \cdot D}{2 \cdot I_{out(max)} \cdot f_{min}}$$

$$\text{where: } D = \frac{V_o + V_F}{V_{in(min)} - V_{cesat} + V_F}$$

In overload or in short circuit conditions, the switching frequency decreases below the minimum limit fixed in standard operative conditions (f_{min}). For this reason is important to select a f_{min} with margin to avoid values inside the audible range in worst case.
Too low inductance values are not suitable because the increased ripple current in the core may generate too high ripple voltage in the output.

Example:

We want to use the L4963 in an application in the following conditions:
V_i = 15V to 35V
V_o = 5V
I_o = 1.5A (max)
f_{min} > 25KHz
V_{cesat}= 1.5V
V_F = 1V
The right inductance for this application is calculated as follows:

$$D_{max} = \frac{5 + 1}{15 - 1.5 + 1} = 0.41$$

$$L \leq \frac{(15 - 1.5 - 5) \cdot (0.41)}{2 \cdot 1.5 \cdot 25 \cdot 10^3} = 46\mu H$$

Suggested value for L is in this case 40µH that corresponds to about a 15% less the max. allowed inductance.

OUTPUT CAPACITOR SELECTION

All the considerations for the choice of the filter capacitor in a system working in continuous mode are still valid in a discontinuous mode operation (Ref. L296 Appl.note). Let summarize the results with some useful suggestion for this specific system.

The Ripple Voltage imposed on the D.C. output voltage is given by the sum of two terms. The first term (V_c), depends from I_{Lpeak}, Switch. Frequency and C_{out} values and the second (V_{ESR}) is due to Equivalent Series Resistance (ESR) of the capacitor multiplied by the I_{Lpeak} current.

$$V_o = V_c + V_{ESR} \quad (6)$$

Where:

$$V_c = \frac{I_{Lpeak}}{8 \cdot C_{out} \cdot f} = \frac{2I_{out}}{8 \cdot C_{out} \cdot f} = \frac{I_{out}}{4 \cdot C_{out} \cdot f} \quad (7)$$

$$V_{ESR} = I_{Lpeak} \cdot ESR = 2 \cdot I_{out} \cdot ESR \quad (8)$$

Once fixed the amount of ripple voltage desired for the application, with the first term we determine the minimum suitable capacitor value and with the second one we determine the maximum ESR acceptable.
Normally, for frequencies above 20KHz, the maximum ESR defines the choice of the filter capacitor value. In general, lower capacitor values have higher ESR ratings, so higher output capacitors than is calculated in eq. (7) should be used.

To guarantee a proper operation of the internal Error Amplifier, the minimum ripple voltage in the output must exceeds 15mV, to ensure a minimum voltage difference across its input terminals.

POWER DISSIPATION

It can be considered as the addition of three values:

Ptot = Psat + Pq + Psw where:

Psat: Saturation losses of the power transistor plus the sensing resistor power dissipation.

$$Psat = V32 \cdot I_o \cdot \frac{ton}{T} = V32 \cdot I_o \cdot \frac{V_o}{V_i}$$

V32 = dropout voltage between input (pin 3) and output (pin 2).

For worst case (for I2 = 3A switch current) the V32 = 2V

Pq: Losses due to the stand-by current and to the power driving current.

$$Pq = Vi \cdot I'3q + Vi \cdot I''3q = \frac{t_{on}}{T} = Vi \cdot I'3q + Vo \cdot I'' 3q$$

In fig. 6 and fig. 7 are showed these two typical values of quiescent current.

For the we worst case we can considered:

I'3q (0% d.c.) =13mA

I''3q (100% d.c.) = 17mA

Psw: Power transistor switching losses:

$$Psw = V_i \cdot I_O \cdot \frac{tr + tf}{2T}$$

Figure 5: V32 Voltage vs. Output Current

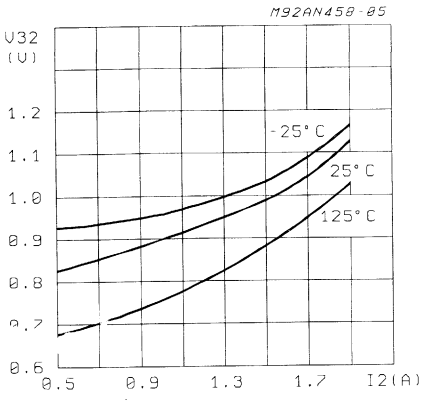


Figure 6: Quiescent Drain Current vs. Supply Voltage (0% Duty Cycle)

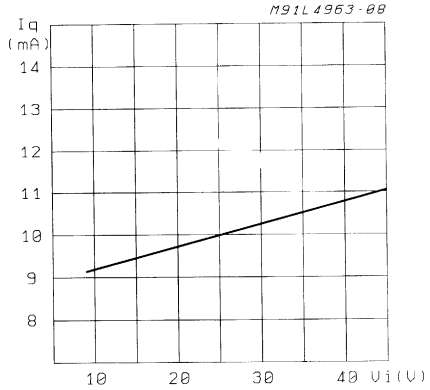
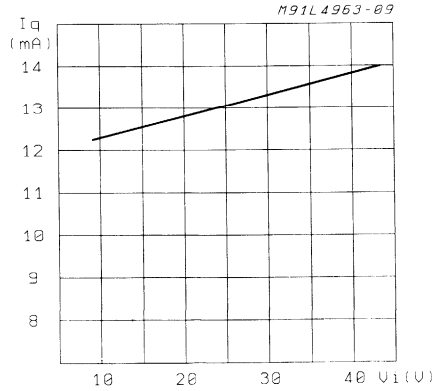


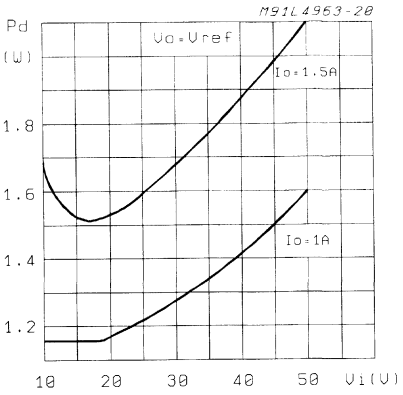
Figure 7: Quiescent Drain Current vs. Supply Voltage (100% Duty Cycle)



The fig. 8 shows the total power dissipation of the device.

For V_{out} > 5V the output current can be less then 1.5A. In fact we have to consider that the maximum power dissipation for this device is 2W at T_{amb} of 70° and is this value that limits the output current value.

Figure 8: Power Dissipation vs. Input Voltage.



EFFICIENCY

The system efficiency is expressed by the following formula.

$$\eta\% = \frac{P_O}{P_i} \; 100$$

where $P_O = V_O \; I_O$ (with $I_O = I_{load}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_O plus all the other system losses. The expression of the efficiency becomes threfore the following.

$$\eta = \frac{P_O}{P_O + P_{sat} + P_q + P_{sw} + P_D + P_L}$$

The three terms concerning the device power losses have already been discussed in the previous paragraph.
We examine now the last two terms concerning the external components losses.

PD – Losses due to the recirculation diode

These losses increase as V_i increase, as in this case the ON time of the diode is greater.

$$PD = VF \cdot I_O \cdot \frac{V_i - V_O}{V_i} = VF \cdot I_O \cdot \left(1 - \frac{V_O}{V_i}\right)$$

where VF is the forward voltage of the recirculation diode at current I_O.

Figure 9: Efficiency vs. Output Voltage

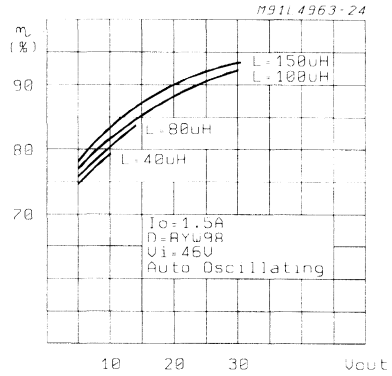
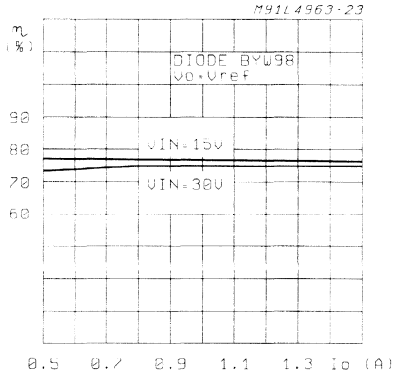


Figure 10: Efficiency vs. Output Current



PL – Losses due to the coil

Wecan divide these losses in two parts: core losses and copper losses.

The core losses for molypermalloy powder cores are given by the following formula.

$$W = 0.568 \cdot f^{1.23} \cdot B^{2.56}$$

where W = watt/lb

f = KHz

$$B = KGauss = \frac{(V_i - V_O) \cdot V_O \cdot 10^8}{N \cdot Ae \cdot f \cdot V_i}$$

N = number of turns

Ae = core cross section (cm^2)

copper losses:

$$P - \rho I^2_o \, MLT.N$$

N = number of turns

MLT = lenght/turn for 20% of winding factor

ρ = copper resistivity (1.72 10E-6Wcm)

Refer to table 1 for some ρ/Aw suggest values.

Table 1

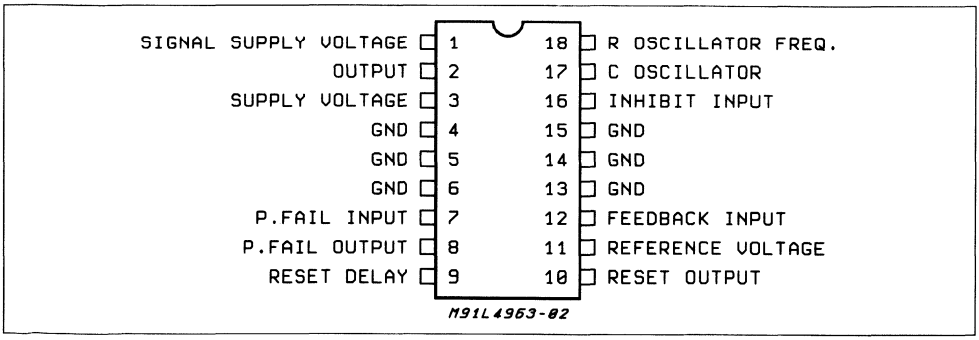
AWG	Diameter Copper (cm)	OHMS/CM 20C	OHMS/CM 100C
18	.102	.000209	.000280
19	.091	.000264	.000353
20	.081	.000333	.000445
21	.072	.000420	.000561
22	064	000530	000708

Typical efficiencies obtained with the test and application circuit of fig. 20 are shown below.

DEVICE DESCRIPTION

Fig.11 shows the pin connection of the Powerdip 12+3+3 plastic package. The internal block diagram of the device is shown in fig.1. Each block will now be examined in detail.

Figure 11: Powerdip 12+3+3 Pin Connection



POWER SUPPLY

The device has two separate pins dedicated for the supply source. Pin.1 is for the Signal (Vcc) and Pin.3 for the Power (Vss) source; normally these two pins are connected together (see the typical application circuit Fig. 18). The L4963 is provided with an internal stabilized power supply that feeds the precise internal voltage reference 5.1V (±2%) and the internal analog blocks.

UNDER VOLTAGE LOCK OUT (UVLO)

The UVLO circuit ensures that Vcc is adequate to make the L4963 fully operational before enabling the output power stage. The UVLO turn-on and turn-off thresholds are internally fixed at 8.4V and 7.9V respectively.

This function acts also on the Power Fail and Reset Circuits; their output voltages pin.8 and pin.10 respectively, remain low state until the turn-on threshold is reached.

OSCILLATOR

The oscillator circuit behaves in a completely different way compared to the usual Step-Down regulator operating at fixed frequency and variable duty cycle. In fact, usually, the oscillator generates a fixed frequency sawtooth waveform that is compared with the Error Amplifier output voltage, generating the PWM signal to be sent to the power output stage.

In the L4963, the oscillator function is quite different. In the following we will describe briefly its operation referring to the simplified internal schematic shown in fig.12.

It is composed of a comparator (with inputs compatible to ground) with an hysteresis whose thresholds are 1V and 4.1V respectively.

The oscillator uses an external resistor RT on pin.18 to establish the charging and discharging current of the internal timing capacitor CT = 50pF, fixing in this way the maximum switching frequency:

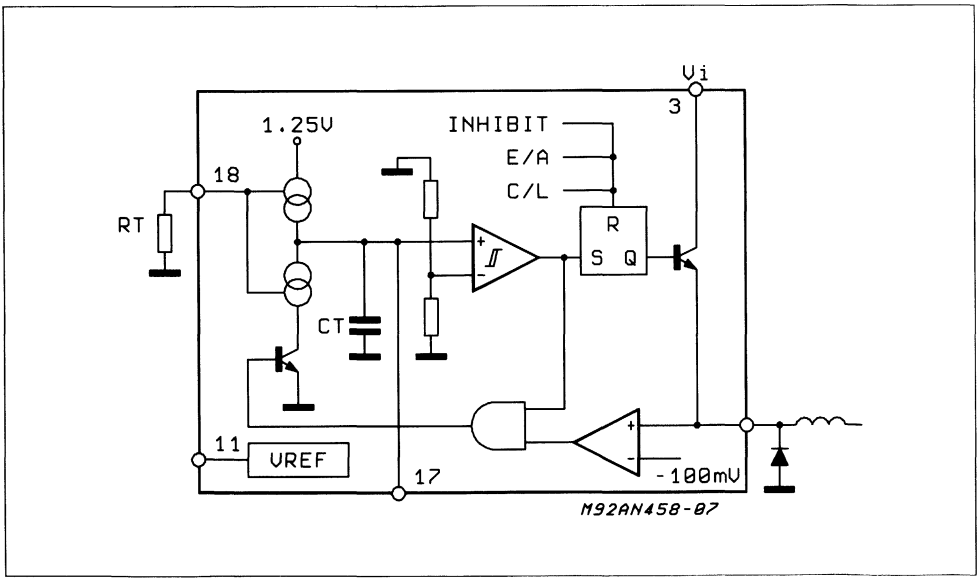
$$f_{osc}(KHz) = \frac{0.033}{Rt\ (K\Omega)}$$

It is also possible to increase the internal timing capacitor value, connecting an external capacitor between pin.17 and ground. The oscillator circuit, as we have seen in the "CIRCUIT OPERATION" paragraph, sends a set pulse to the latch that enables the power stage.

This set pulses train is at fixed frequency imposed by the external resistor when the device operates for low output currents (Dead time present in the inductor current I_L).

When we are operating in self-oscillating mode, the comparator that senses the free-wheeling status disables the oscillator pulses output until the inductor is fully discharged, varying in this way the switching frequency. It is also possible to disable the oscillator forcing the system to operate always in self-oscillating mode, connecting-together the internal oscillator capacitor (pin.17) with the voltage reference pin.11.

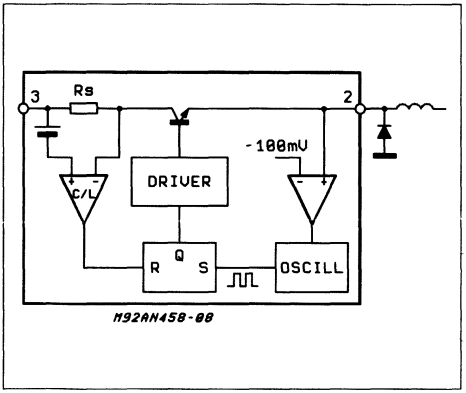
Figure 12: Oscillator Circuit



CURRENT LIMITATION

Output overload protection is provided by a current limiter circuit. The load current is sensed by an internal metal resistor (Rs) in series to the power transistor. When the voltage drop on the sense resistor, reaches the current comparator offset voltage, the current comparator generates a reset pulse for the latch, disabling the power stage.
Typical current limiting threshold is around 4.5A.
The power stage will be enabled again only when the energy stored in the inductor will be completely discharged, this due to the free-wheeling sense comparator (see Circuit operation paragraph for details).
The current limiting circuit operates also as soft-start during the device turn-on preventing over-currents on the load.
In fig.13 is shown the simplified internal schematic circuit of the current limiter.

Figure 13: Current Limiter



RESET

The reset circuit accomplishes a very important function when the L4963 is used in applications where it feeds microprocessors and logic devices. The function block diagram is shown in Fig.14. The Reset circuit monitors the output voltage and generates a logic signal when the output voltage is within the limits required to supply correctly the microprocessor.
This function is realized through three pins:

- Feedback input (pin.12)
- Reset delay (pin.9)
- Reset output (pin.10)

When the monitored voltage on pin.12 is lower than 5V, the comparator (A) output is high and the reset delay capacitor is not charged because the transistor Q1 is saturated, also the transistor Q2 is saturated, mantaining the voltage on pin.10 at low level.
When the voltage on pin 12 exceeds 5V, the transistor Q1 switches off and the delay capacitor (Cd) starts to charge through an internal current generator of about 110µA. When the voltage on pin 9 reaches 4.5V, the output of the comparator (B) switches low and pin 10 goes high.
As the output is an open collector transistor (Q2), a pull-up external resistor is required.

On the contrary, when the Reset input voltage goes below 5V, with an hysteresis of 100mV, the comparator (A) triggers again and sets istantaneously the voltage on pin 10 low, therefore forcing to saturation the Q1 transistor, that starts the fast discharge of the delay capacitor.
As shown in the block diagram, the Reset output is low when the UVLO or The INHIBIT signals are present.
Inside the chip there is a digital filter that prevents the Reset circuit activation if V_{out} drops below the reset threshold for less than 2s.
In this way the Reset circuit neglects very fast drops in the output voltage.
In fig.15 and Fig.16 are shown respectively the Reset circuit Waveforms and a typical application.

Figure 14

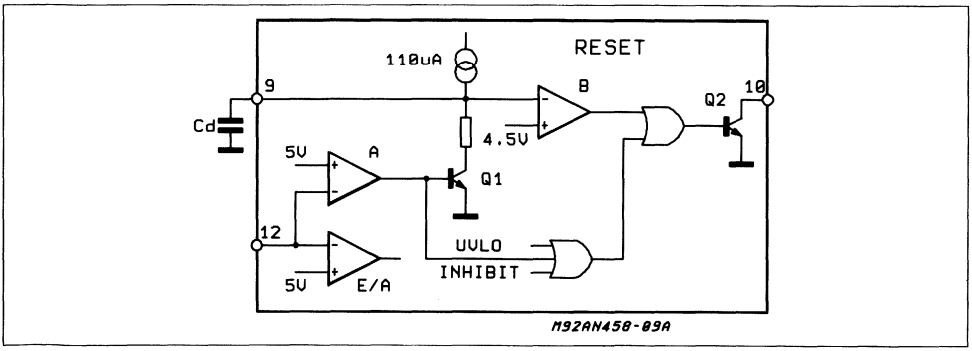


Figure 15

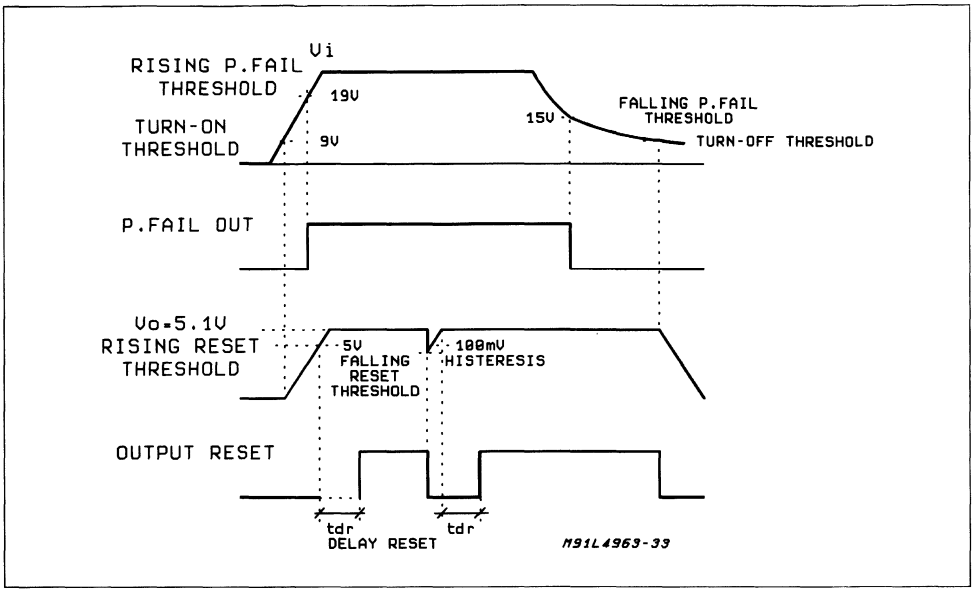
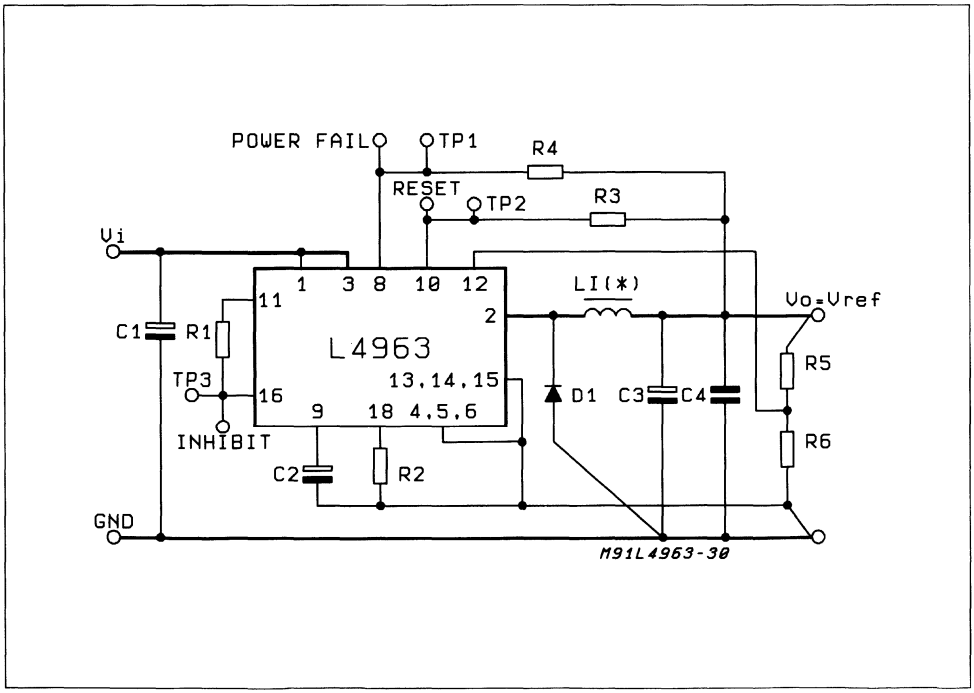


Figure 16



POWER FAIL

The Power-Fail circuit monitors the supply voltage (V_{SS}) via an internal voltage divider (R1=115KΩ, R2=35KΩ) as shown in Fig.17. When the supply voltage reaches the typical rising threshold voltage of 22V, set by the internal voltage divider, the Power Fail comparator output voltage goes low, turning off the output transistor Q1. This gives an high level on pin.8. As the power Fail output is an open collector transistor (Q1), an external pull-up resistor is required.

The Power Fail output goes low, giving an alarm signal, when the input voltage decreases reaching the internal typical Falling threshold voltage level of 18V. It is possible to change the rising and the falling threshold voltages, connecting a proper external voltage divider on pin.7.
In fig. 15 are shown the power fail waveforms.

INHIBIT

The INHIBIT function, available on pin.16, disables the regulator with a TTL logic signal. An high level at this pin (above 2.2V) switches off the power stage and forces low the output reset.
This useful feature, is normally used for supply sequencing and remote control ON-OFF.

THERMAL PROTECTION

The thermal protection function, operates when the junction temperature reaches 150°C; it acts directly on the power stage, turning it immediately off.
The thermal protection is provided with hysteresis and therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

The L4963, thanks to the reduced external component count represents a very low cost effective solution in many applications.

In Fig.18 the complete typical application circuit is shown, where all the functions available on the device are being used.
In fig.19 is shown the same application circuit for reduced filter capacitor count and its PCB. As evident the PCB dimensions are reduced.
Below we will describe the design procedure to follow and some suggestion regarding the external components to use.

Figure 17

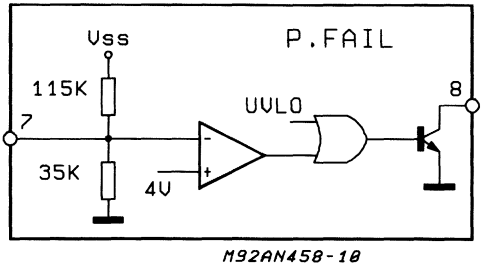
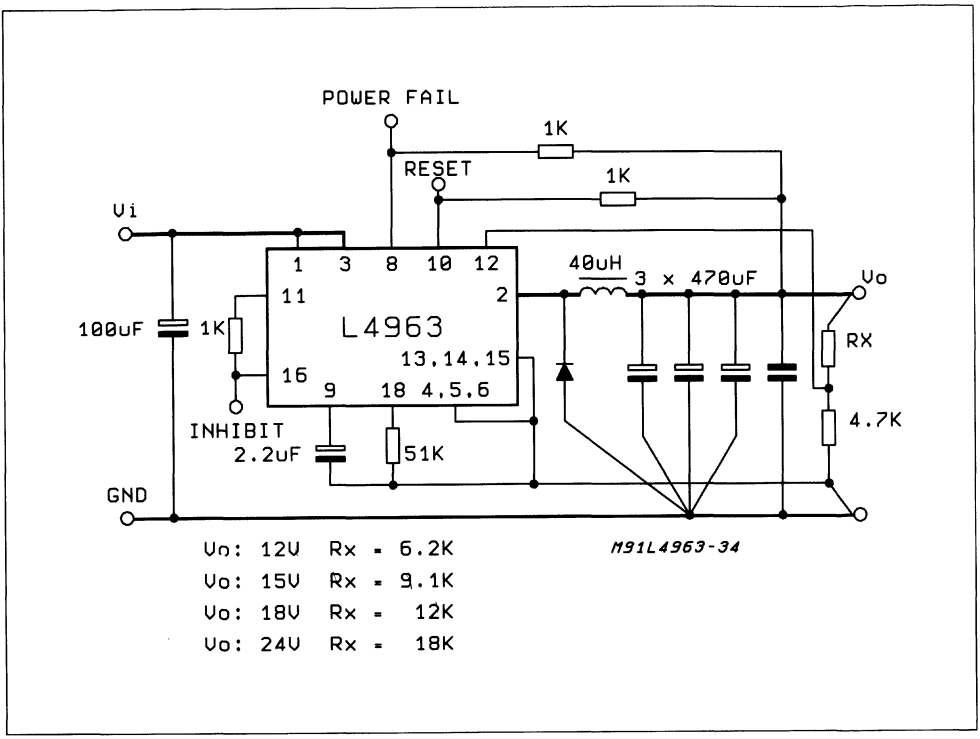


Figure 18: Test and Application Circuit



PART LIST

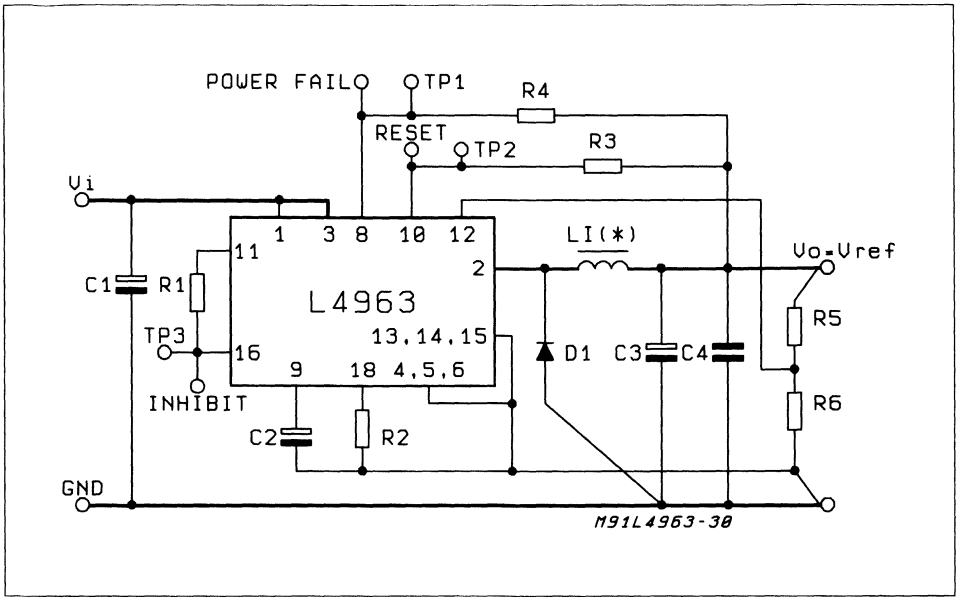
CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2µF 16V
C3, C4, C5	4700µF 40V EKR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
Vo	R6	R5
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP
34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 29: Typical Application Circuit



PART LIST

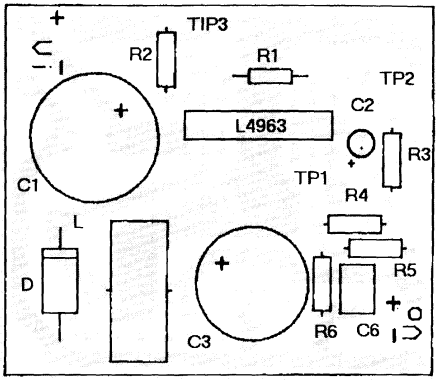
CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2µF 16V
C3	4700µF 40V EKR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
Vo	**R6**	**R5**
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP
34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 20: P.C. Board and Component Layout of the Circuit of fig. 21 (1:1 scale).



L4963 Step-Down Regulator Design Example

Referring to the complete typical application circuit shown in fig.19, and defined the following conditions:

- V_{out} = Regulated output voltage
- $V_{in(min)}$= Minimum input voltage
- $V_{in(max)}$ = Maximum input voltage
- $I_{out(max)}$ = Maximum load current
- f_{min} = Minimum switch freq. in self-oscillating mode.

We calculate the value of the external components.

1. OUTPUT VOLTAGE SETTING:

The output voltage is established by the voltage divider constituted by R5 and R6. To select the right R5 value use the following formula:

$$R5 = \frac{(V_{out} - V_{ref})}{V_{ref}} \cdot (R6)$$

where: V_{ref} = 5.1V
R6 = Is normally set at 4K7Ω

For a Quick calculation of some standard output voltages, the following table is useful:

Resistor Values for Standard Output Voltages		
Vo	**R6**	**R5**
12	4.7KΩ	6.2KW
15	4.7KΩ	9.1KΩ
18	4.7KΩ	12KΩ
24	4.7KΩ	18KΩ

To obtain V_{out} = V_{ref}, the pin.12 is directly connected to the output, therefore eliminating both R5 and R6.

2. INDUCTOR SELECTION:

The max. duty cycle is determined by the following formula:

$$D_{max} = \frac{V_{out} + V_F}{V_{in(min)} - V_{ce(sat)} + V_F}$$

Where: $V_{ce(sat)}$ = 1.5 V
V_F = Catch diode forward drop

The maximum inductor value is then calculated:

$$L\,max = \frac{(V_{in(min)} - V_{ce(sat)} - V_{out})}{2 \cdot I_{out(max)} \cdot f(min)} \cdot D\,max$$

where:
f(min) 20KHz to be out of the audible range.

In discontinuous mode operation, the inductor current may reach very high peaks ($I_{Peak} = 2I_{out}$), so it is important to verify that the coil will not saturate in overload or short circuit conditions damaging the output power stage due to the high dI/dt ratio.
Therefore, a correct dimensioning requires a saturation current above the maximum current limit threshold ($I_{2max\,-\,peak}$ = 6A).

3. Output Capacitor Selection:

The output voltage ripple depends on the current ripple in the inductor and on the performance of the output capacitor at the switching frequency .The minimum value of the output filter capacitor is obtained from:

$$C_{out(min)} = \frac{I_{out(max)}}{4 \cdot V_{ripple(p-p)} \cdot fmin}$$

where $V_{ripple(p-p)}$ is the amount of ripple voltage desired.

Clearly this formula doesn't take care of the capacitor Equivalent Series Resistance (ESR) value, that is the dominant factor to define the output ripple voltage at switching frequencies greater than 20KHz.

So we suggest to use also the following formula:

$$ESR(max) = \frac{V_{ripple(p-p)}}{2 \cdot I_{out(max)}}$$

Where the ESR(max) requirement is not satisfied by the capacitor value given by the first formula, use an higher value or, better, put in parallel several capacitors in order to reduce the total ESR.

The capacitors' voltage rating should be at least 1.25 times greater than the given output voltage.

The big advantage of this system is to greatly reduce number of external components compared to the continuous mode solution.

The only drawback is a higher ripple voltage on the output that can be up three times larger than in continuous mode.

A proper choice of low ESR filtering capacitors can solve this problem greatly reducing the output ripple.

4. CATCH DIODE SELECTION:

The catch diode must comply with several requirements and its choice requires special care.

The current rating must be at least 1.2 times greater respect the maximum load current, but this is not enough because in short circuit conditions, the maximum current limiter threshold is 6A to which correspond an average output current of I_{out} = Ipeak/2 = 3A. This is the current requirement to useto choose the right diode.

The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

The diode recovery speed is not so important because the power stage is turned-on only when the inductor is fully discharged and the diode is definitely off. So there is not simultaneous conduction between them.

This allows a reduction of the disturbances with respect to the continuous mode, because they are mainly radiated during the transistor switch on, for the steep slopes during the simultaneous conduction of transistor and reverse conduction-diode.

!.OW COST APPLICATION

If the remote inhibit, the reset and the power fail functions are not used we can reduce further the external component count.

It is possible in this case, to have a very efficient-switch mode power supply for very low cost applications.

Two examples of minimal component count regulators are shown in fig.21 and fig.22.

Figure 21: A Minimal 5.1 Fixed Regulator – Very Few Components are Required

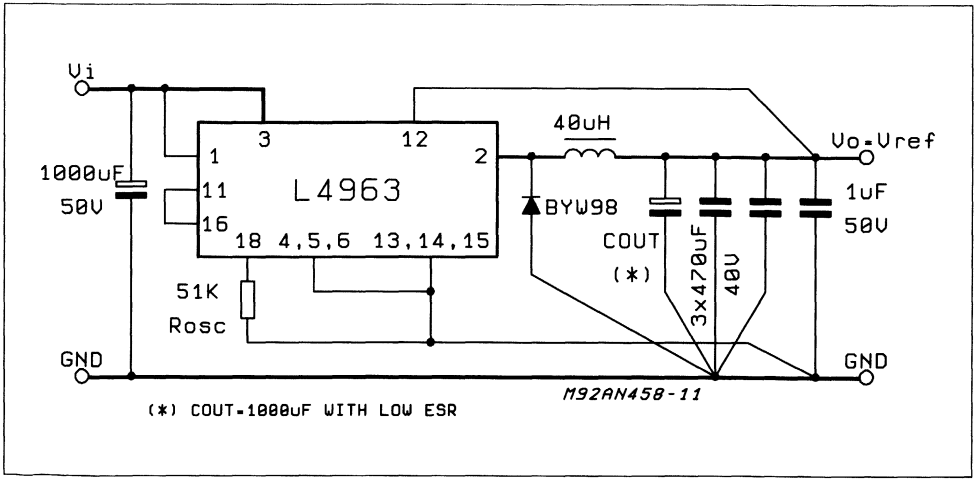
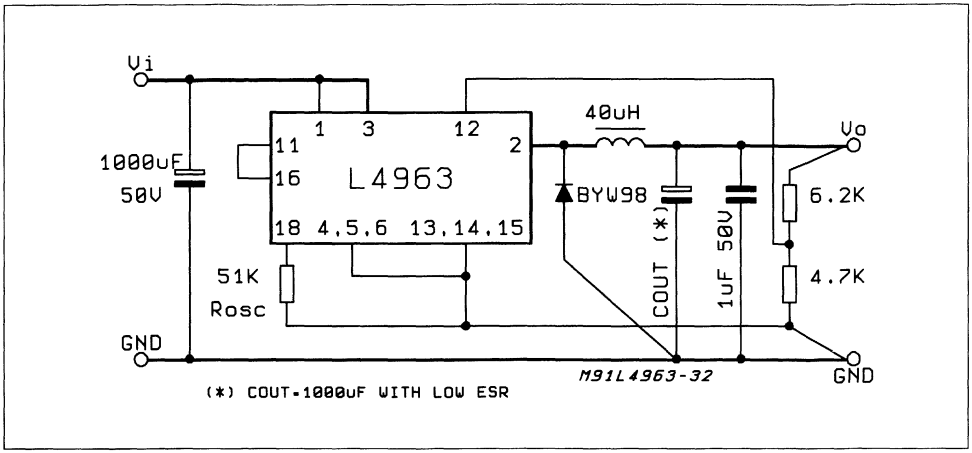


Figure 22: A Minimal Components count for V_O = 12V



DUAL OUTPUT POWER SUPPLY

The application shown in fig.23 is interesting because it provides two output voltages. The main voltage, is directly controlled by the feedback loop, the second voltage is obtained through an auxiliary winding. As the auxiliary voltage is obtained through a completely separated winding, it is possible to obtain either a positive or a negative voltage. Where isolation is not required between the two outputs, we can reduce the number of the auxiliary turns improving also the tolerance of the secondary output using the configuration illustrated in fig.24.

For both this configurations, the discontinuous mode is ideal because we have a good energy transfer between primary and secondary windinngs, due to the high energy stored in the coil that is function of the ripple current in the inductor.

Figure 23: Multioutput isolated.

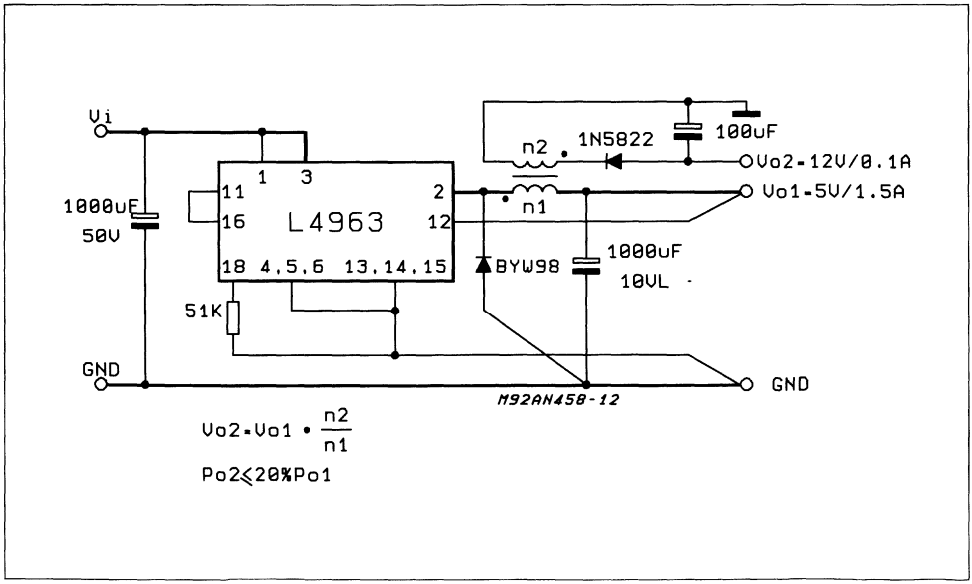
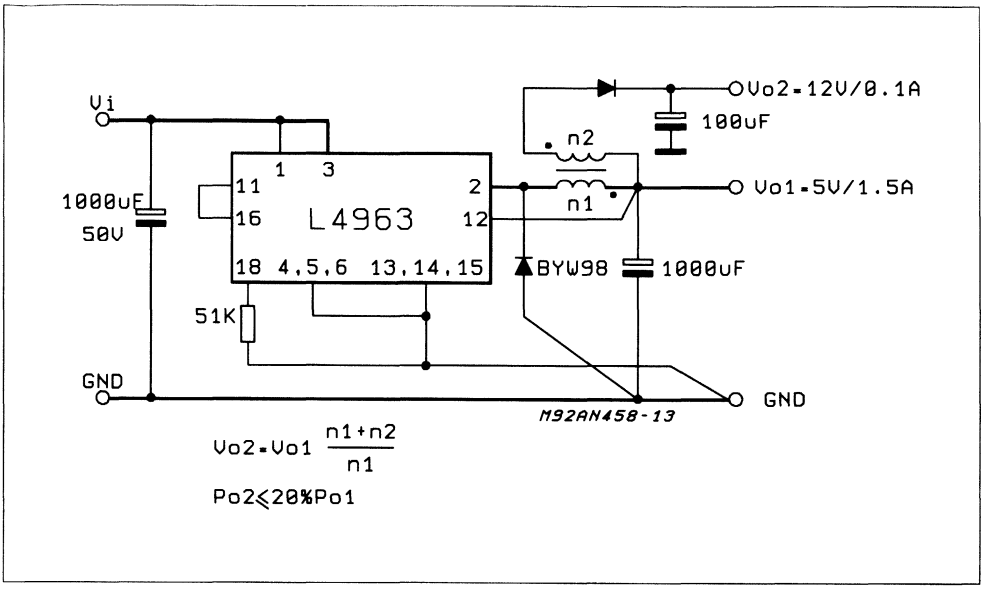


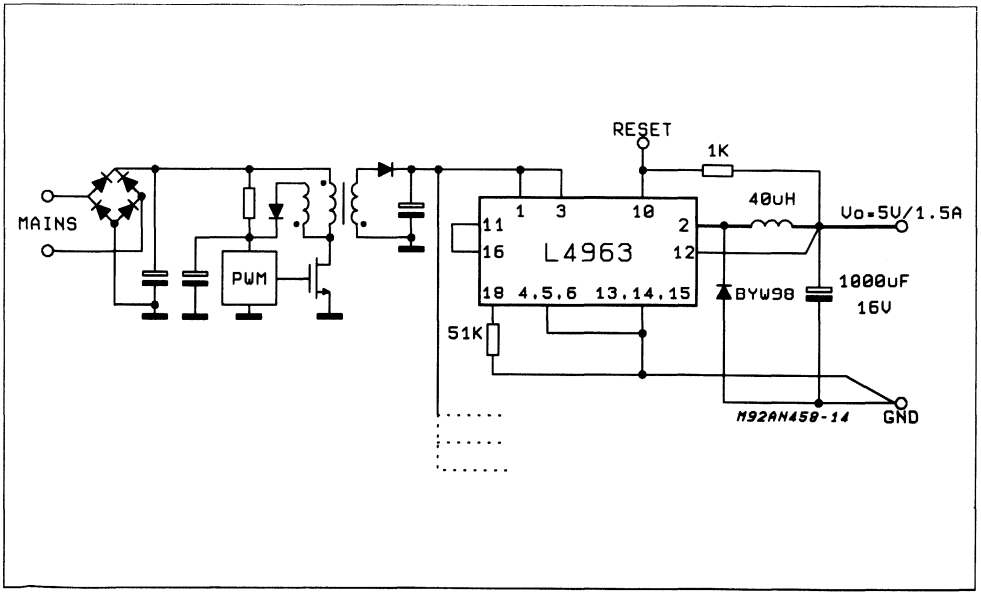
Figure 24: Multioutput not isolated.



L4963 IN OFF-LINE POWER SUPPLY

The L4963 can be useful as post regulator in off-line power supplies, where it can sobstitute the usual linear post regulation increasing the efficiency and reducing the complexity of the transformer, if the distributed power supply approach is used (see fig.25).

Figure 25: Typical off-line solution using L4963 as post regulator.

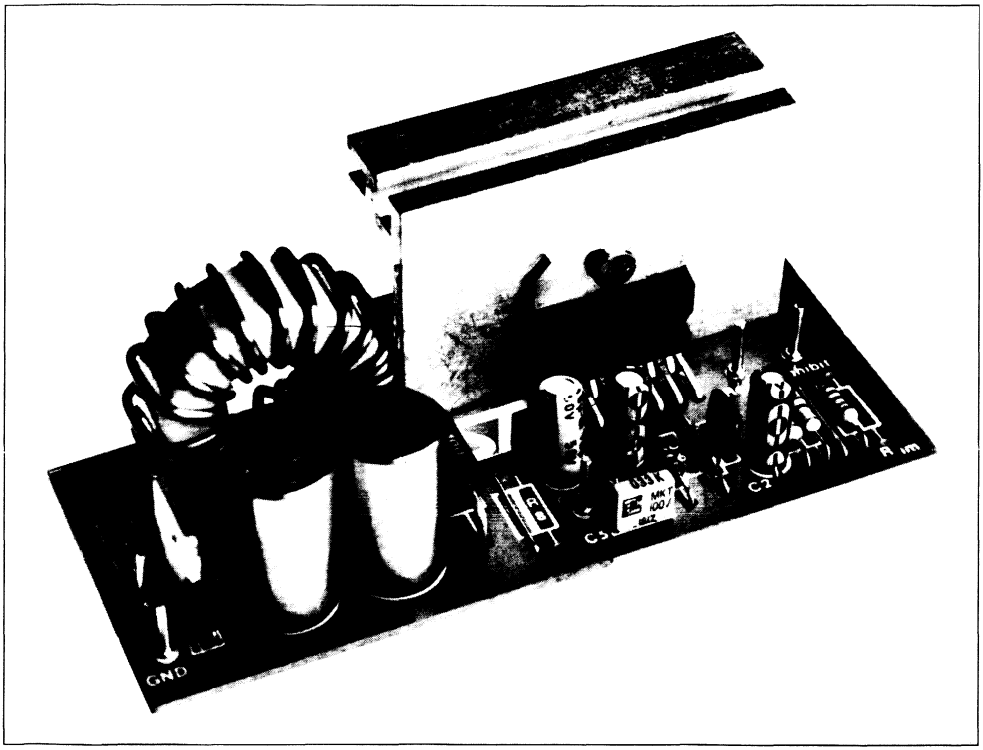


SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

A cost-effective replacement for costly hybrids, the L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.



The SGS THOMSON L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven be integrated PWM regulator circuits (giving a maximum output current of 300 to 400mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequencies in the 20kHz to 40kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100kHz. At 200kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4 A to the load, at an output voltage adjustable from 5.1 to 40V ; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10mA/Mil^2 are achieved.

In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3°C/W between junction and package and of 35°C/W between junction and ambient. This thermal resistance (inclucing the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows : Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component super-imposed on it, ΔI_L, due to the voltage across L.

Figure 1 : The Basic Step-down Switching Regulator Configuration.

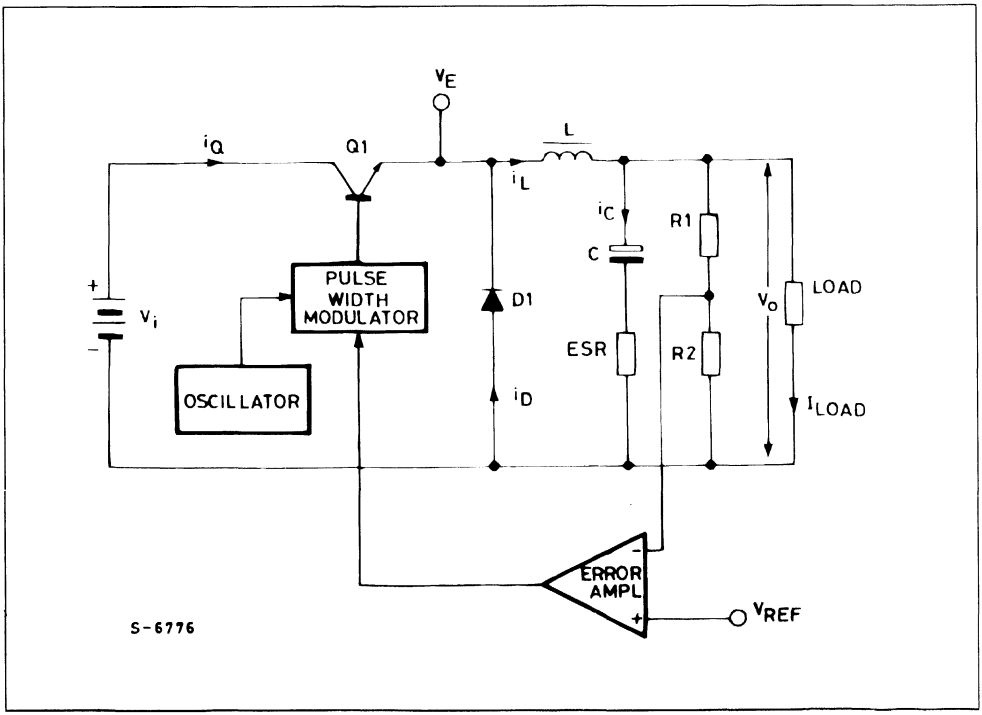


Figure 2 : Principal Circuit Waveforms of the figure 1 Circuit.

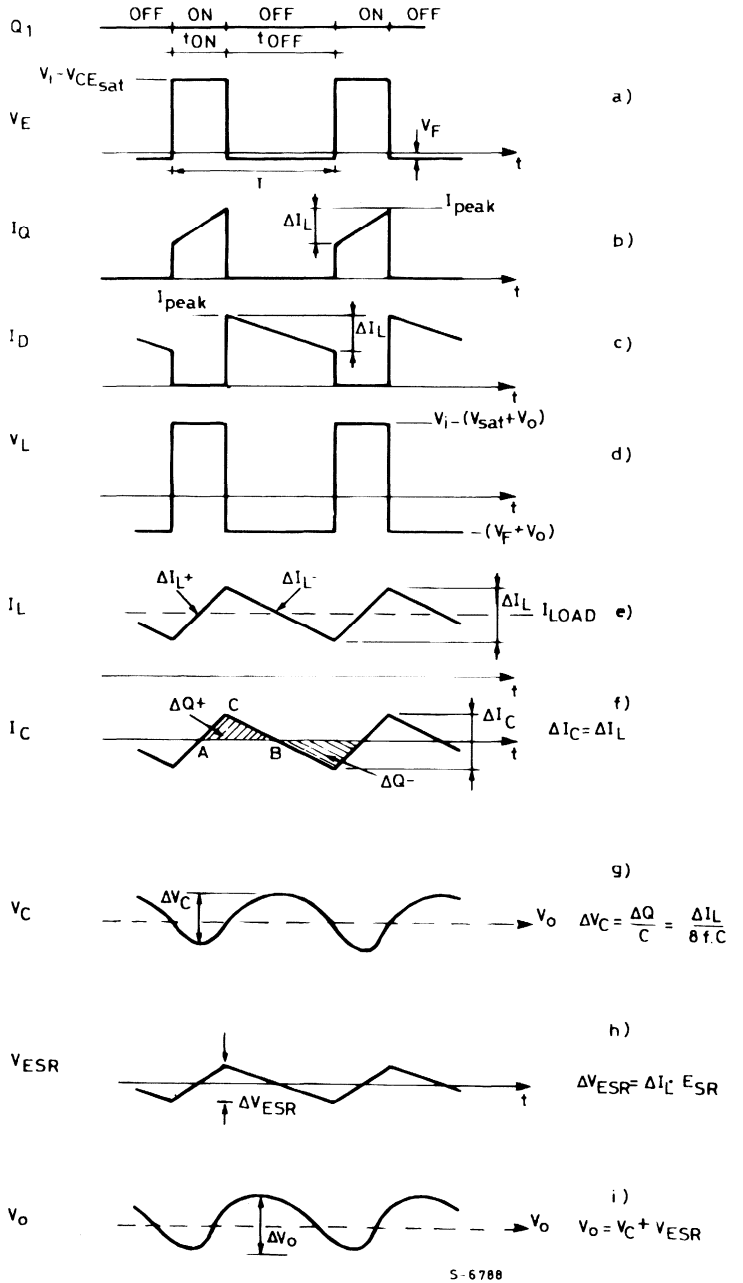


Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode era taken into account.

The ON and OFF times are established by the following expression :

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occuring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula :

$$\Delta I_L^+ = \Delta I_L^- = \frac{(V_i - V_{sat}) - V}{L} T_{ON} =$$

$$= \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect to $I_{OMIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.
This ripple consists of two components : a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f :

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives :

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is V_{ESR} (t) = i_C (t) · ESR. Fig. 2i shows the overall ripple V_o, which is the sum of the two previous components. As the frequency increases (> 20kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where Q = ON, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression :

$V_i = v_L + v_C$ (V_{sat} is neglected against V_i).

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \qquad (1)$$

which gives :

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \qquad (2)$$

The current through the inductance is given by :

$$I_L = \frac{(V_i - V_o)}{L} t \qquad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that :

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \qquad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot very instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present :

$v_C(t) = V_o$, $i_L(t) = i_D(t) = I_{peak}$

And the equation associated to the following loop may be written :

$$V_F + L\frac{di_L}{dt} + v_C = 0 \quad (5)$$

where :

$v_C = V_o$

$$\frac{di_L}{dt} = -(V_F + V_o)/L \quad (6)$$

It follows therefore that :

$$i_L(t) = -\frac{V_F + V_o}{L}\ t \quad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs :

$$I_L = \frac{V_o}{L}t \quad (8)$$

therefore :

$$\Delta I_L^- = \frac{V_o}{L}\ T_{OFF} \quad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$ if follows that :

$$\frac{(V_i - V_o)\ T_{ON}}{L} = \frac{V_o\ T_{OFF}}{L}$$

which allows us to calculate V_o :

$$V_o = V_i\frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i\frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relationship between the currents is the following :

$$I_{iDC} = Io_{DC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula :

$$\eta\ \% = \frac{P_o}{P_i}\ 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o, plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \quad (12)$$

DC LOSSES

P_{sat} : saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o\frac{T_{ON}}{T} = V_{sat}\ I_o\frac{V_o}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current Io.

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F\ I_o\frac{V_i - V_o}{V_i} = V_F\ I_o\left(1 - \frac{V_o}{V_i}\right) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S\ I_o^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current :

$$P_q = V_i\ I'_{3q} + V_i\ I''_{3q}\ \frac{T_{ON}}{T} \quad (16)$$

where being :

$\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ it follows that :

$P_q = V_i\ I'_{3q} + V_o\ I''_{3q}$ in which :

$I'_{3q} = I_{3q}$ at 0 % duty cycle

$I''_{3q} = I_{3q(100\ \%\ d.c.)} - I_{3q\ (0\ \%\ d.c.)}$

SWITCHING LOSSES

P_{sw} : switching losses of the power transistor :

$$P_{sw} = V_i\ I_o\frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculation T_{ON} and T_{OFF} through (4) and (9) respectively it follows that :

$$T_{ON} = \frac{\Delta I_L^{+} \cdot L}{V_i - V_o} \qquad T_{OFF} \quad \frac{\Delta I_L^{-} \cdot L}{V_o}$$

But because :

$T_{ON} + T_{OFF} = T$ and $\Delta I_L^{+} = \Delta I_L^{-} = \Delta I_L$,

it follows that :

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, \Delta I_L}\, T \qquad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that :

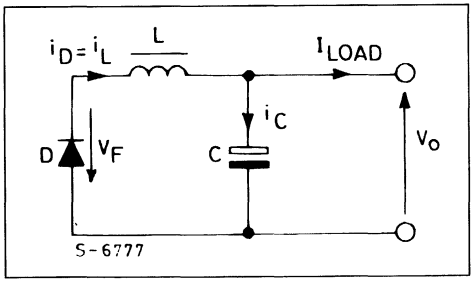
$$L = \frac{(V_i - V_o)\, V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$$ where L is in Henry and f in Hz

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by :

$i_C(t) = i_L(t) - I_o$

Figure 3 : Equivalent Circuit Showing Recirculation when Q1 is Turned Off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that :

$$\Delta V_C = \frac{\Delta I_L}{4C}\,\frac{T}{2} = \frac{\Delta I_L\, T}{8C} = \frac{\Delta I_L}{8fC} \qquad (19)$$

but, remembering expression (4) :

$$\Delta I_L^{+} = \frac{(V_i - V_o)\, T_{ON}}{L}$$ and $$T_{ON} = \frac{V_o}{V_i}\, T$$

therefore equation (19) becomes :

$$\Delta V_C = \frac{(V_i - V_o)\, V_o}{8\, V_i f^2\, L\, C}$$

Finally, calculating C it follows that :

$$C = \frac{(V_i - V_o)\, V_o}{8\, V_i\, \Delta V_C\, f^2\, L} \qquad (20)$$

where : L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true :

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \qquad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C\,(dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.
Moreover, the following is true :

$$v_L = L\,\frac{di_L}{dt} \qquad (23) \qquad \text{where } di_L = \Delta I_o.$$

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and (23) and equalizing, it follows that :

$$L\,\frac{di_L}{v_L} = C\,\frac{dv_c}{i_c}$$

Calculating dv_c and equalizing it to ΔV_o, it follows that :

$$\Delta V_o = \frac{L \Delta I_o^2}{C(V_i - V_o)} \qquad (24) \qquad \text{for } + \Delta I_o$$

$$\Delta Vo = \frac{L \Delta I_o^2}{CV_o} \qquad (25) \qquad \text{for } - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments.

The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks.

Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zenze-zap trimming, the voltage is within ± 2% limits.

Figure 4 : Pin Assignments of the L296.

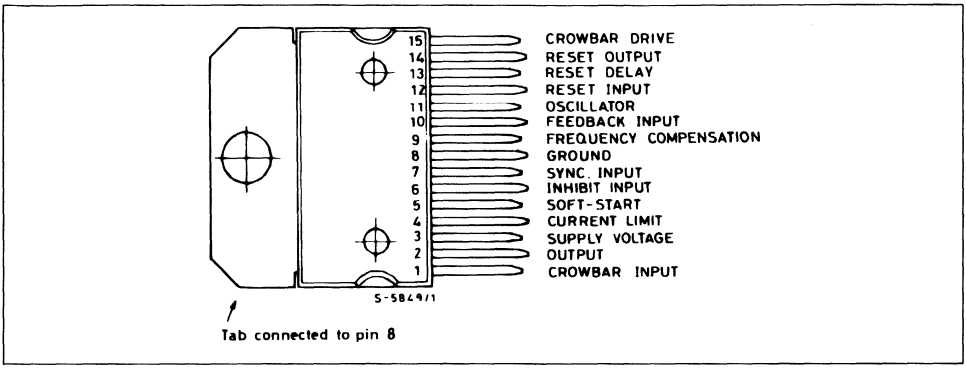
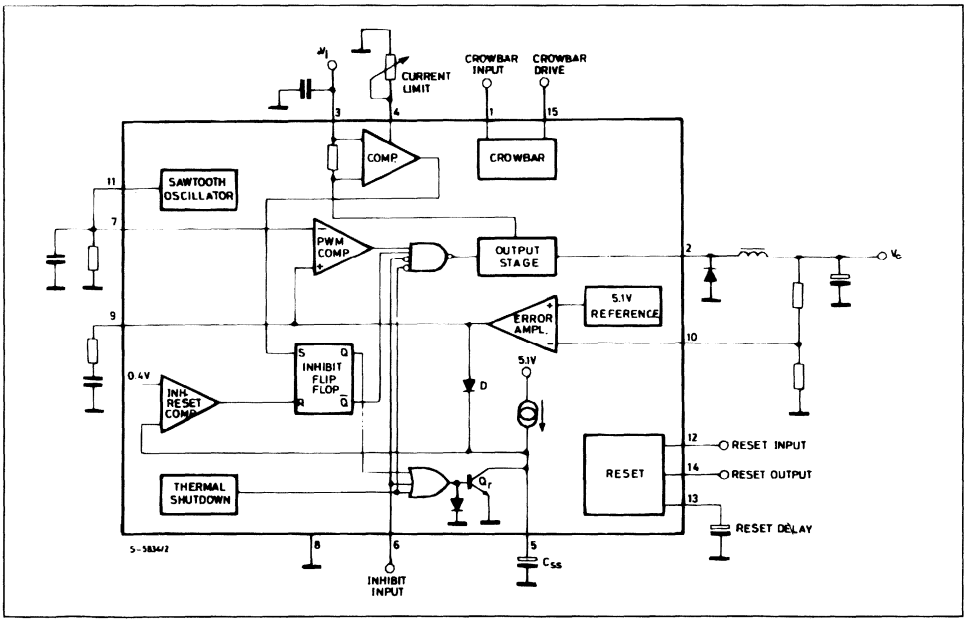


Figure 5 : Block Diagram of the L296. In Addition to the Basic Regulation Loop the Device includes Functions such as Reset, Crowbar and Current Limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{osc} capacitor which then discharges across the R_{osc} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{osc} capacitor and the R_{osc} resistance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{osc} capacitor rapidly ; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1, too) ; the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{osc} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{osc} and R_{osc}. For this reason the capacitor charging current (when S_1 is ON) is typically around 10mA. For example, with a 2.2nF capacitor to switch from 1.2V to 3.2V about 400ns is required, which is negligible compared to the 10µs period that occurs when the operation is performed at 100kHz. The diagrams shown in fig. 8 allow the calculation of the R_{osc} value (R_1 in fig. 8) with C_{osc} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Figure 6 : Internal Schematic of the Oscillator.

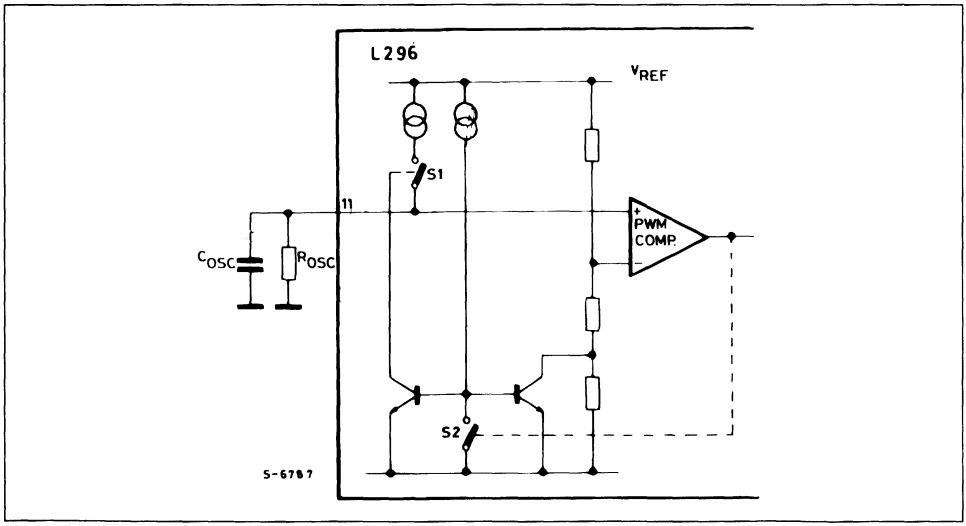


Figure 7a : Oscillator Waveform at Pin 11 with f = 100Khz (R_{osc} = 4.3KΩ, C_{osc} = 2.2nF).

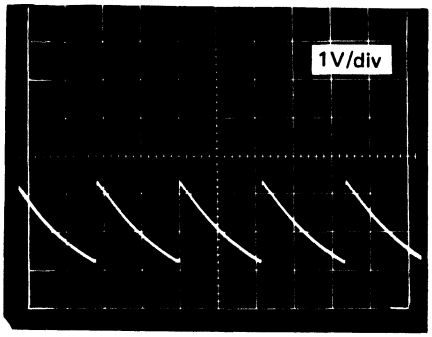


Figure 7b : Oscillator Waveform at Pin 11 with f = 50Khz (R_{osc} = 9.1KΩ, C_{osc} = 2.2nF).

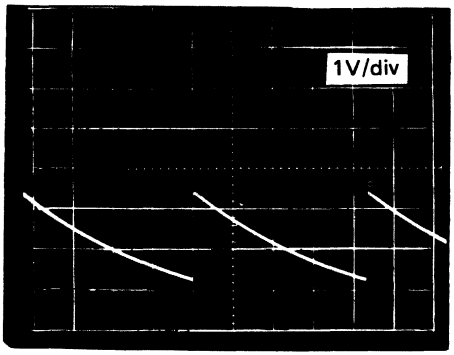


Figure 8 : Nomogram for the Choice of Oscillator Components.

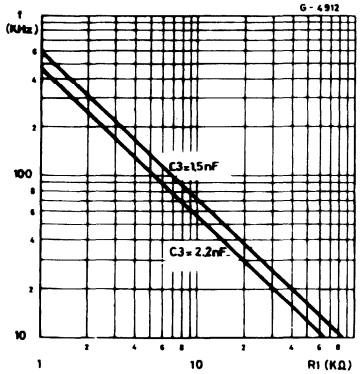


Fig. 8 shows two suggested values for the C_{osc} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold due to the switching delays of the comparator. This inaccuracy in caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula :

$$f_{osc} = \frac{1}{R_{osc}\, C_{osc}} \qquad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output ; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.
in particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current (≅ 100μA) up to a value of about V_{REF}. During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp ; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF}.

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.

Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Figure 9 : Partial Internal Schematic Showing PWM and Soft Start Blocks.

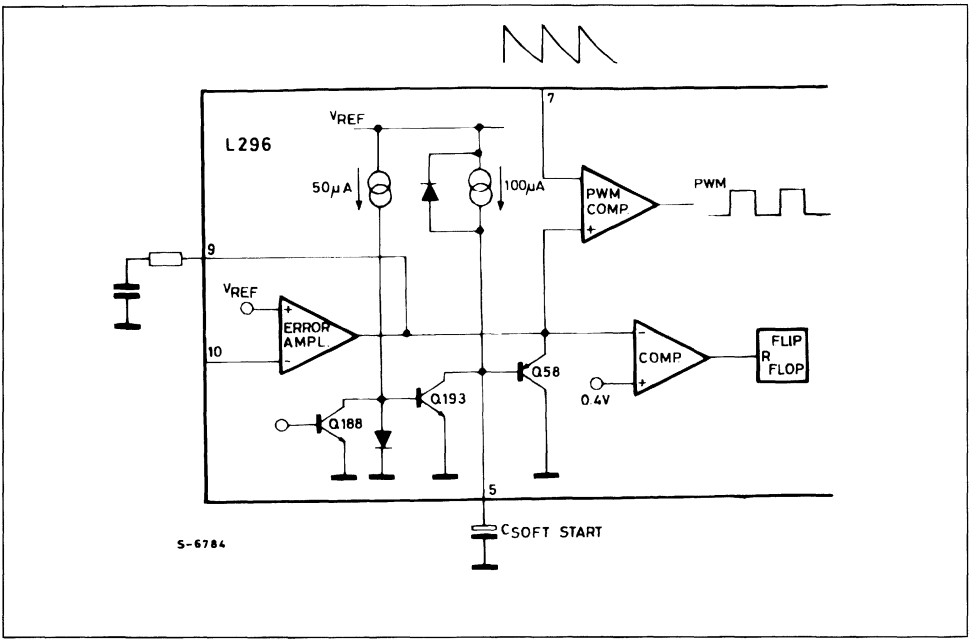


Figure 10 : Soft Start Waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.

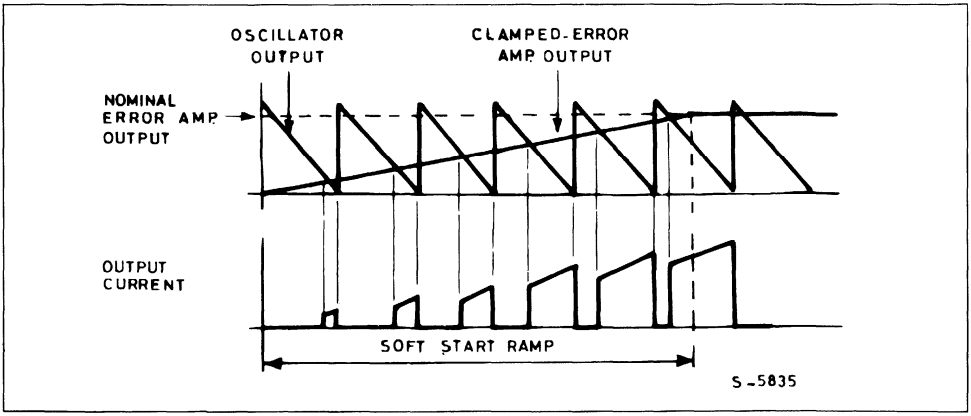
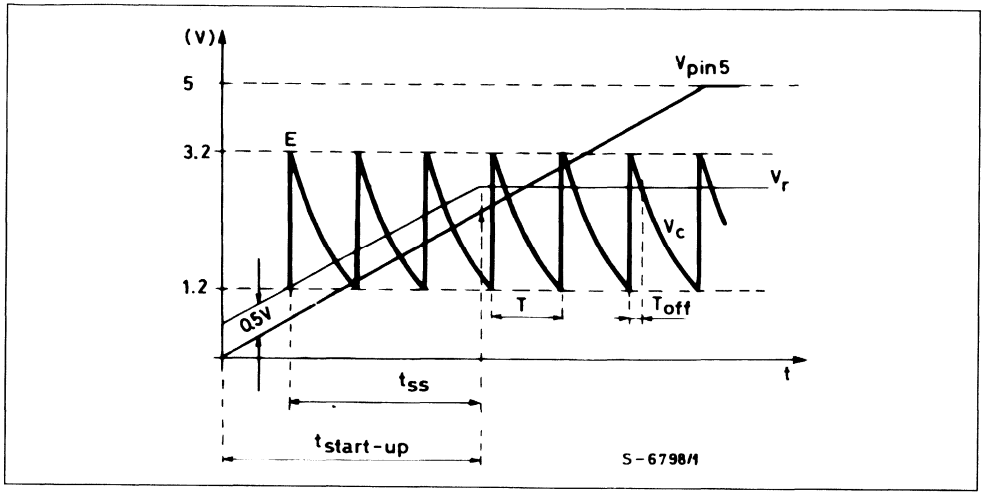


Figure 11 : Waveform for Calculation of Duty Cycle and Soft Start Time.



CALCULATING THE DUTY CYCLE AND SOFT-START TIME

Assume, for simplicity, that the rising edge of the ramp is instantaneous ; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see fig. 11). The PWM comparator block switches when $V_r = V_c$; therefore :

$$V_r = V_c = E\, e^{-\frac{t}{R_{osc} C_{osc}}}$$

Consequently :

$$t = R_{osc} C_{osc} \ln \frac{E}{V_r}$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by :

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc} C_{osc} \ln \frac{E}{V_r}}{T} = \quad (27)$$

$$= 1 - \ln \frac{E}{V_r} = \frac{Vo}{Vi}$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t_{start\text{-}up} = \frac{C_{ss} (V_r - 0.5V)}{I_{5so}}$$

where C_{ss} is the soft-start capacitor and I_{5so} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from (1.2 V – 0.5V) to $V_r - 0.5V$, gives :

$$t_{ss} = \frac{C_{ss} (V_r - 1.2)}{I_{sso}}$$

substituting V_r from (27) gives :

$$V_r = E\, e^{-\left(1 - \frac{V_o}{V_i}\right)}$$

substituting into (28) gives :

$$t_{ss} = \frac{C_{ss}}{I_{sso}} \left(E\, e^{\left(\frac{V_o}{V_i} - 1\right)} - 1.2\right)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number if mutually synchronizable devices is obviously much greater than the three devices shown in the figure. It is anyway diffi-

cult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming C_{osc} = 2.2nF and R_{osc} = 4.3KΩ, it follows that :

$$\frac{1.2V}{4.3K\Omega} = 280\mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by :

$$N = \frac{28\mu A}{I_{bias\ max}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

In the presence of a great number of devices to be synchronized, the lenght of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be with in 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

CURRENT LIMITATION

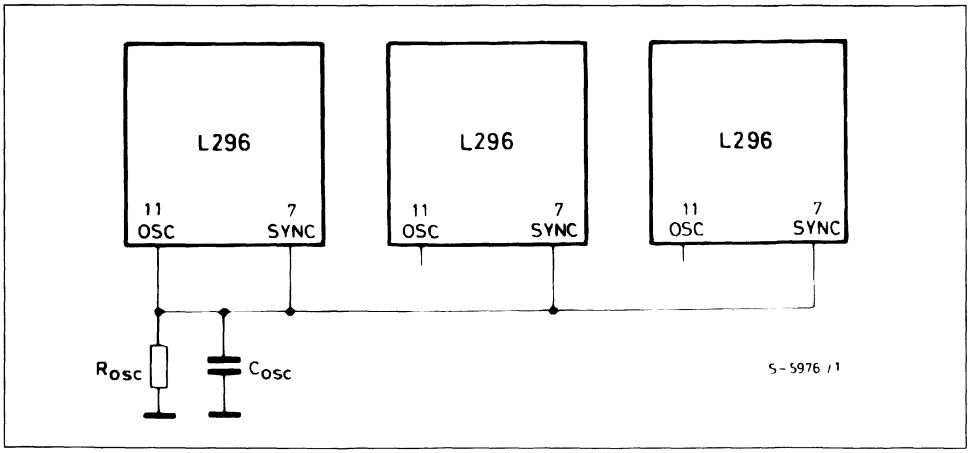
The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described.

Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S. When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1μsec. The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output Q goes low and the power stage is immediately switched off, while the output $\overline{Q}$ goes high and acts directly on the soft-start capacitor dischargng the soft-start capacitor at a constant current (about 50μA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop ; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

Figure 12 : In multiple supplies several l296's can be synchronized as shown here.



From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about 3.3V is present ; by connecting a resistance a constant current, given by 3.3/R, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Figure 13 : Partial Schematic Showing the Current Limiter Circuit.

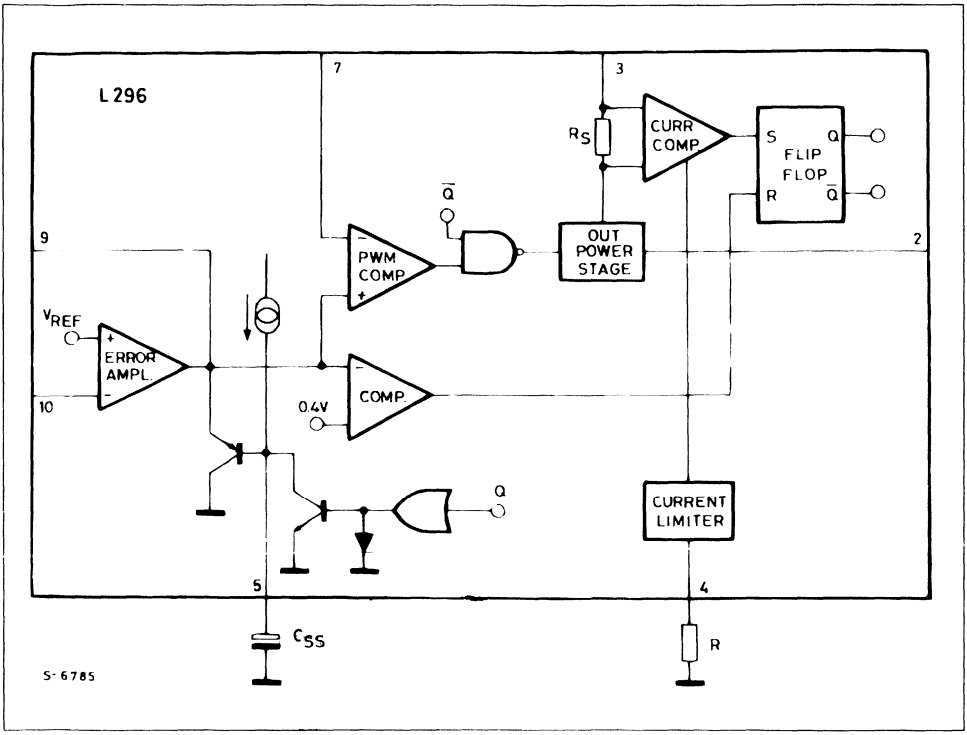


Figure 14a : Current Limiter Waveforms.

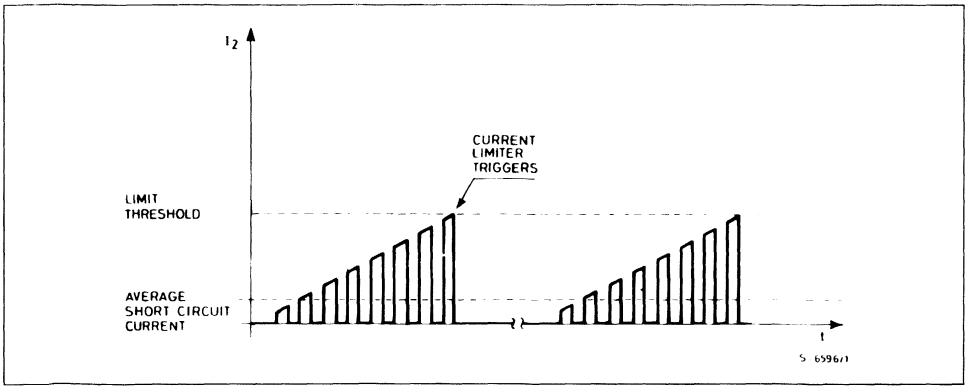
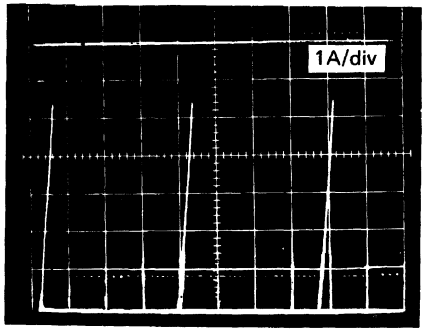


Figure 14b : Load Current in Short Circuit Conditions (V_i = 40V, L = 300µH, f = 100KΩ).

t: 5ms/div

Figure 14c : Current at Pin 2 when the Output is Short Circuited.



t: 5ms/div

RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins : the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about 100µA. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset" ; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarizes the reset function operation.

Figur 5 : Partial Schematic Showing Reset Circuit.

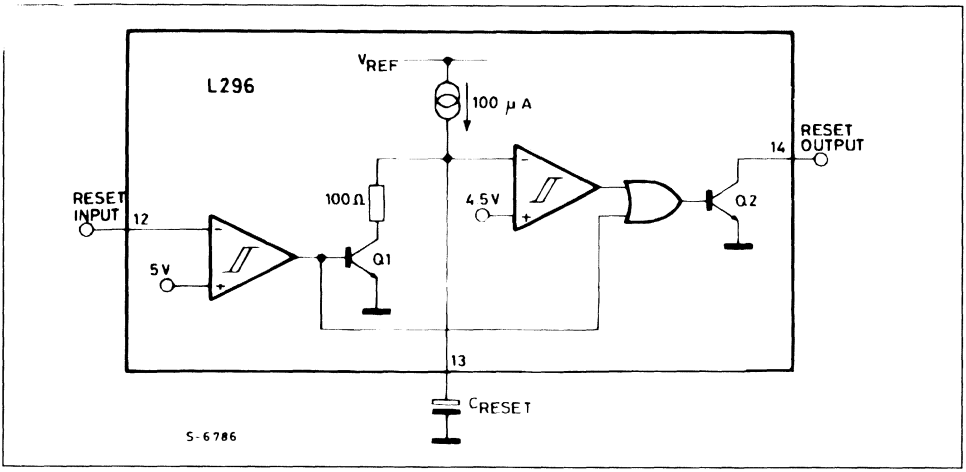


Figure 16 : For Power - On reset the reset block is connected as shown here.

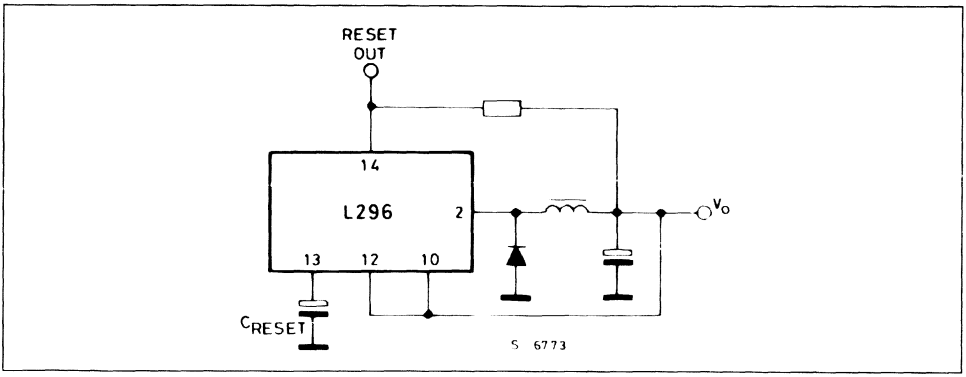


Figure 17 : To obtain a power fail signal, the reset block is connected like this.

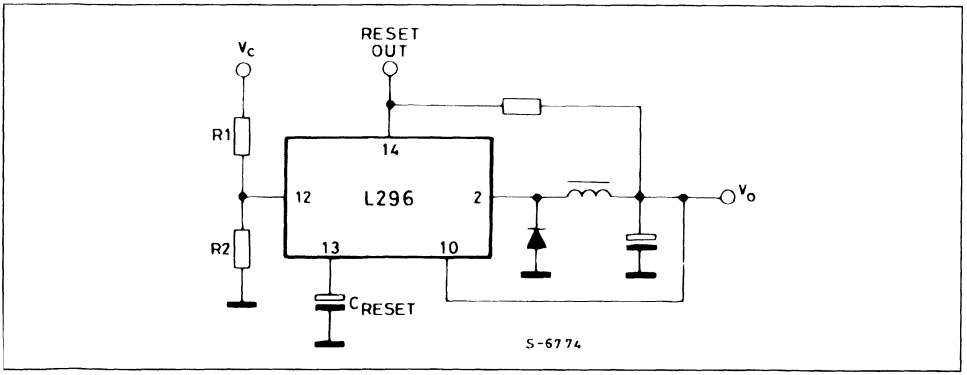
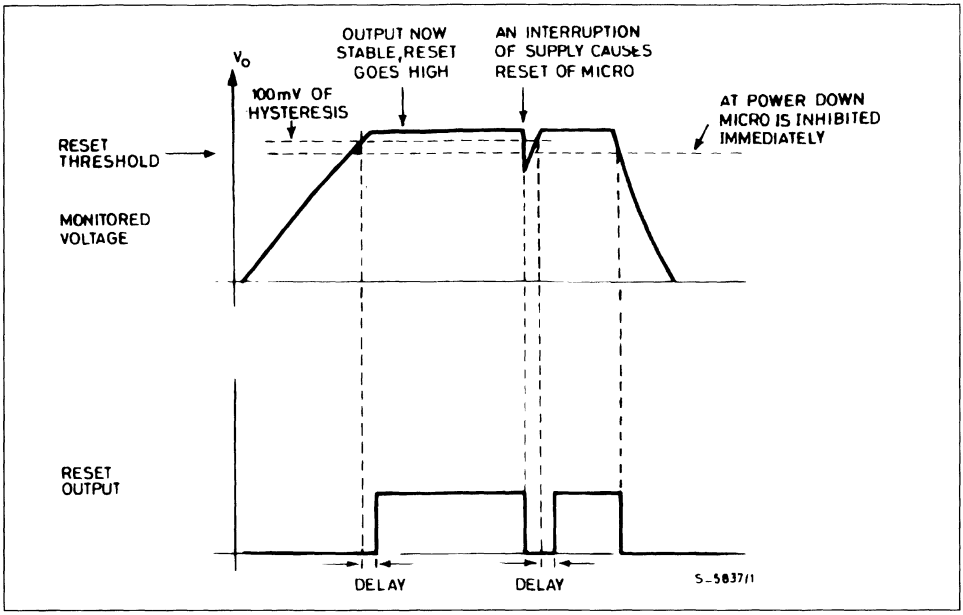


Figure 18 : Waveform of the Reset Circuit.



CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and 21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5µsec to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA ; when not activated, it drains about 5mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Figure 19 : Connection of Crowbar Circuit at Output for 5.1V Output Applications.

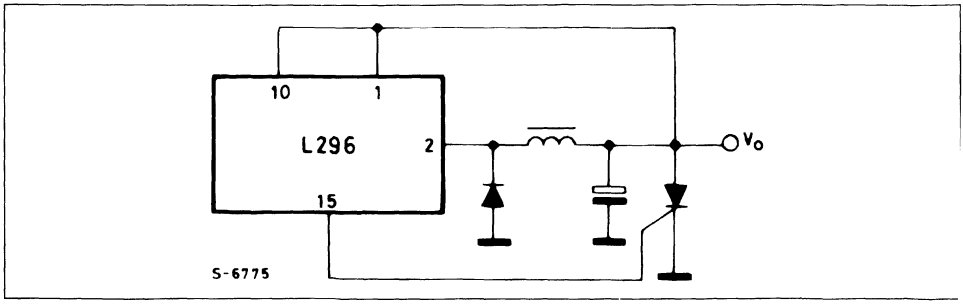


Figure 20 : Connection of Crowbar Circuit at Output for Output Voltages above 5.1V.

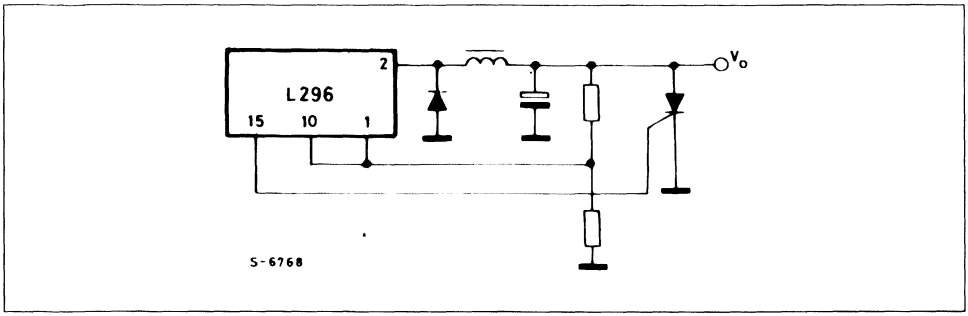
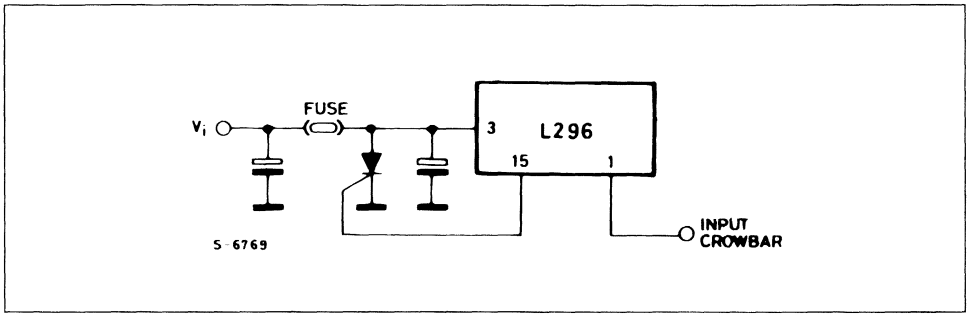


Figure 21 : Connection of Crowbar Circuit to Protect Input. When triggered, the scr blows the fuse.



INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C ; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

Though the L296 is designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

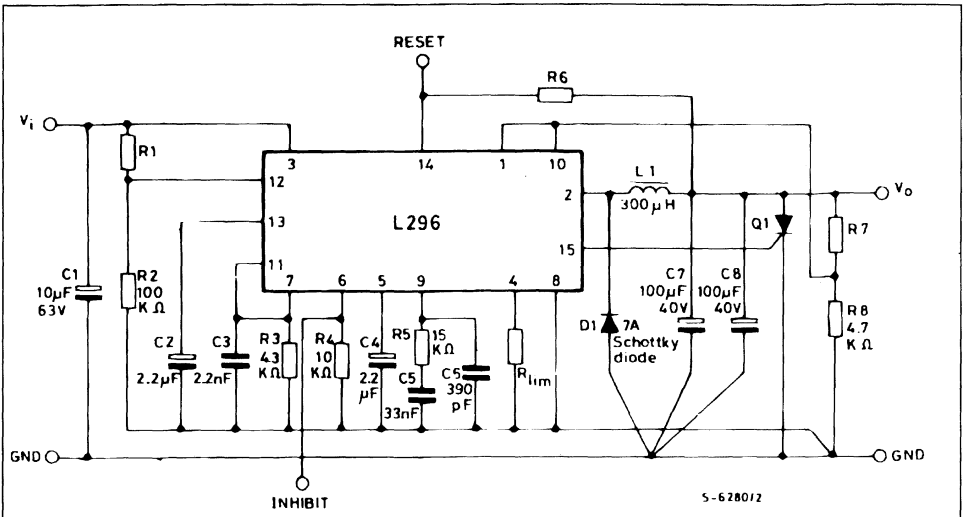
In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages :

Resistor Value for Standard Output Voltages

V_o	R_8	R_7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ
24 V	4.7 kΩ	18 kΩ

To obtain $V_o = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8. The switching frequency is 100kHz.

Figure 22 : Schematic, PCB Layout and Suggested Component Values for the Evaluation Circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.



C7, C8 : EKR (ROE)

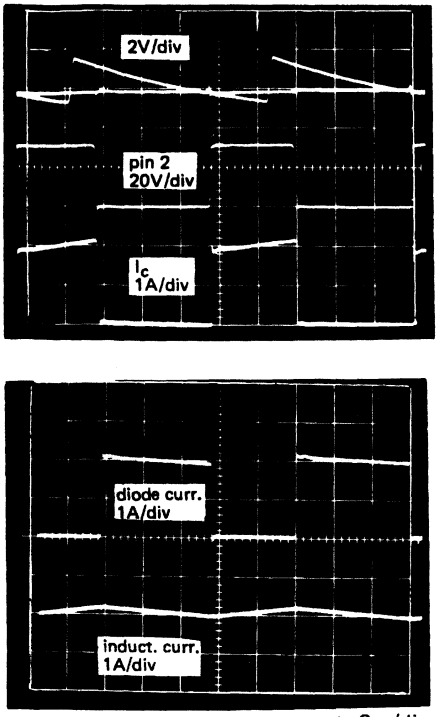
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.

SUGGESTED INDUCTOR (L1) (continued)

Core Type	No Turns	Wire Gauge	Air Gap
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.	
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Figure 23 : Oscilloscope Photographs Showing Main Waveform of the Figure 22 Circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_o depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (> 200kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100μF/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use super fast siodes with 35 to 50ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with trr = 100ns or more is not recommended ; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing trr greater than 35-50ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.

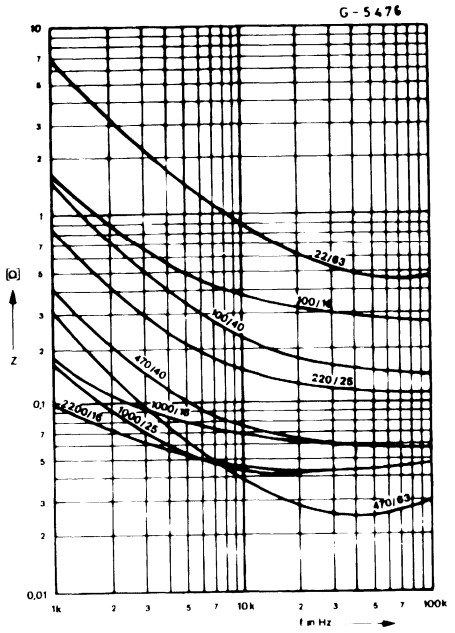
Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L}, the current limit threshold.

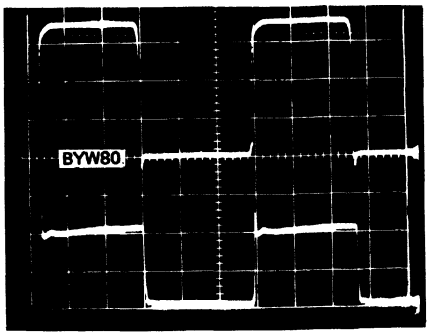
To achieve high saturation with ferrite cores an air gap between the two core halves must be provided ; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.

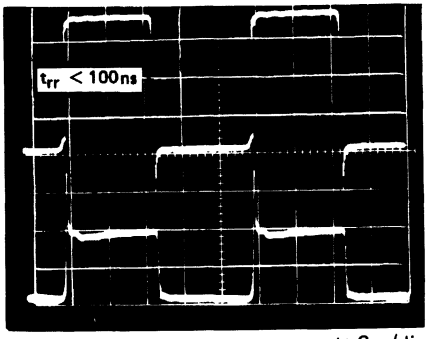
Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer that the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core ; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Figure 24 : Typical Impedance/Frequency curves for EKR Capacitors.

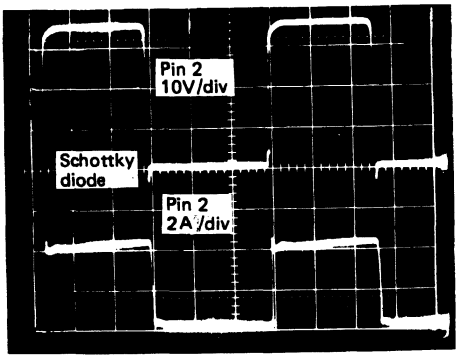






t: 2μs/div

Figure 25 : Oscilloscope Photographs Showing the Waveform obtained with Diodes having Different t_{rr} Values.



t : 2μs/div

LOW COST APPLICATION AND PRERE-GULATOR

Fig. 26 shows the low cost application of a 4A and V_O = 5.1V power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a microprocessor.

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain ?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4 A/5 V supply.

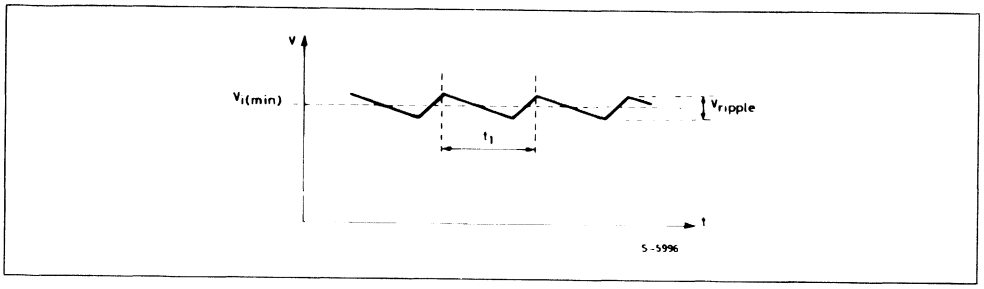
Linear

For a good linear regulator the minimum dropout will be at least 5V at 4A. The minimum input voltage is given by :

$$V_{i\,min} = V_o + V_{drop} + \frac{1}{2} V_{ripple}$$

where :

$$V_{ripple} \cong \frac{I_o\, t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2\ V$$



(a good approximation is 8ms for t_1 at mains frequency of 50Hz and 10.000µF for C, the filter capacitor after the bridge). Therefore $V_{imin} \cong 1.6V$. Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be :

$$V_{nom} = \frac{V_{i\,min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

To allow even a small margin we have to choose :

$V_{nom} = 14V$

The power that the series element must dissipate is therefore :

$P_d = (V_{nom}\ V_o)\ I_o = 36W$

and a heatsink will be necessary with a thermal resistance of :

$R_{th\ heats.} = 0.8°C/W$

and the transformer must supply a power of :

$P_{diss} = 14 \times 4 = 56W$

It must therefore be dimensioned for :

$$PD = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements ; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11°C/W.

	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 °C/W	11 °C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower - particularly when the circuit is enclosed in a box - with all the advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

Figure 26 : A Minimal Component Count 5.1V / 4A Supply.

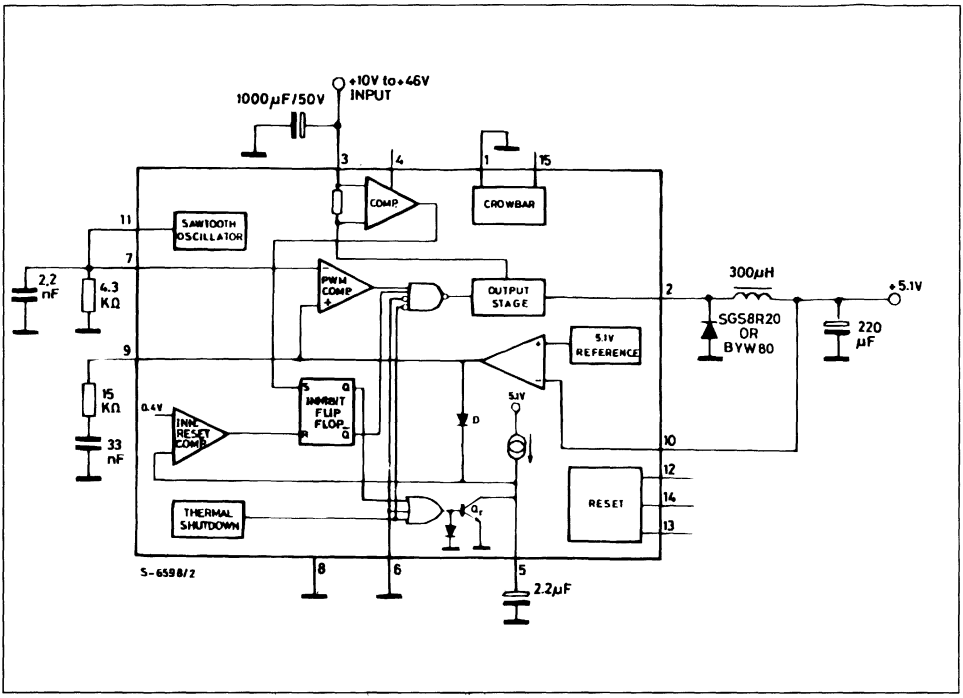
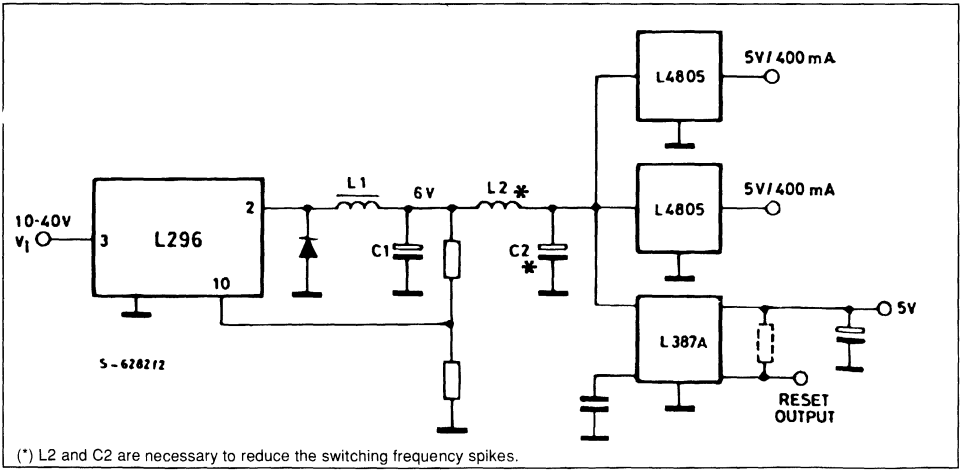


Figure 27 : The L296 may also be used as a preregulator in distributed supply systems.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some speciale features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300µF/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

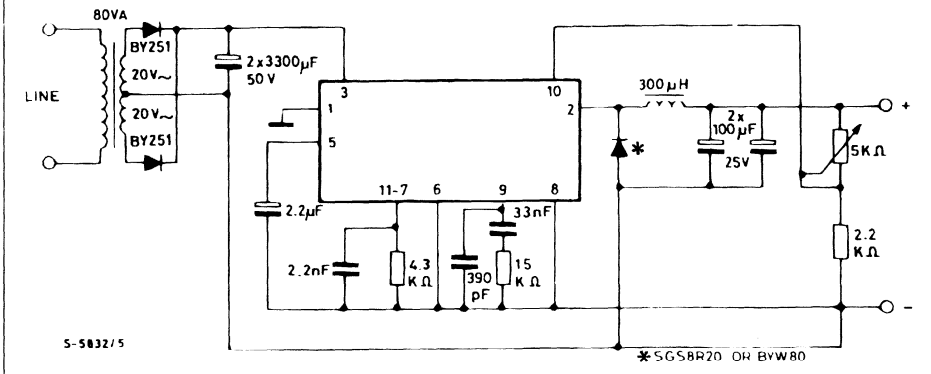
When it is desirable to eliminate the 50/60Hz transformer - in portable or volume-limited equipment-a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

Using a UC3840 which includes the feed-forward function it is possible to compensate mains variation within wide limits. The secondary voltage is therefore only affected by load variations. Using one or more L296s as postregulators, feedback to the primary is no longer necessary, reduces the complexity and cost of the transformer which needs only a single secondary winding.

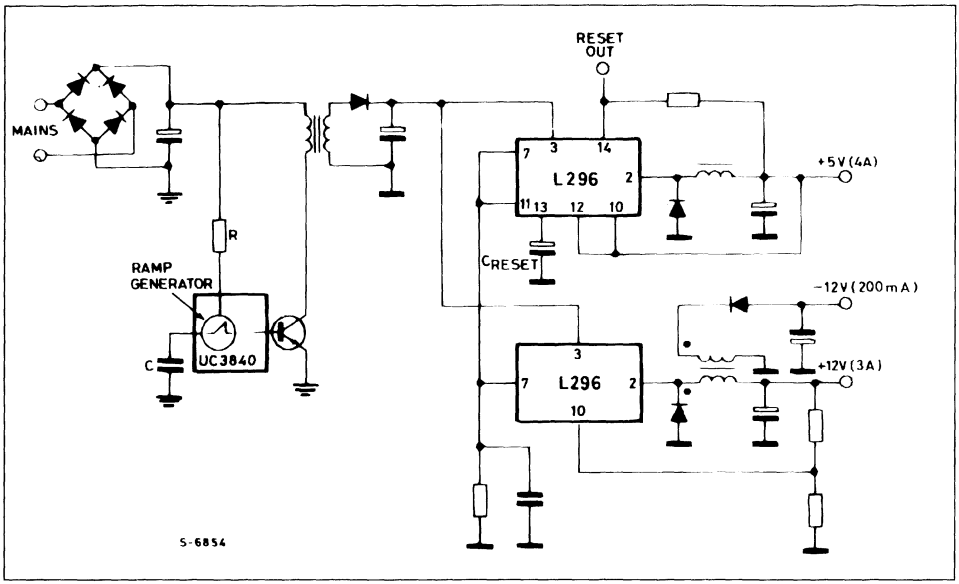
Fig. 28A shows a multi-output supply with a mains preregulator.

Figure 28 : A Typical Variable Supply showing the Mains Transformer.



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100mA)
ripple ≤ 20mV
load regulation (1A to 4A) = 10mV (V_o = 5.1V)
line regulation (200V ± 15% and to I_o = 3A) = 15mV (V_o = 5.1V)

Figure 28A : A Multiple Output Supply using a Switching Preregulator rather than a Mains Transformer.



POWER SUPPLY WITH 0 - 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10kΩ resistor is fixed at approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10kΩ resistance is reduced, together with V_o. When the current reaches zero, it follows that $V_o = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF}, the current start to flow in opposite direction and V_o begins to decrease below 5V.

When $I_1 \times 10k\Omega = V_{REF}$ it follows that $V_o = 0$.

DUAL OUTPUT REGULATOR

The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary + 12V or – 12V output are required, the latter with lower current requirements (100 ÷ 200mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, $V_o = 5.1V$ and $I_o = 2.5A$, the auxiliary - 12V/0.2A voltage is within a ± 2% tolerance.

Figure 29 : Variable 0–30V supply illustrating how output voltages below 5.1V are obtained.

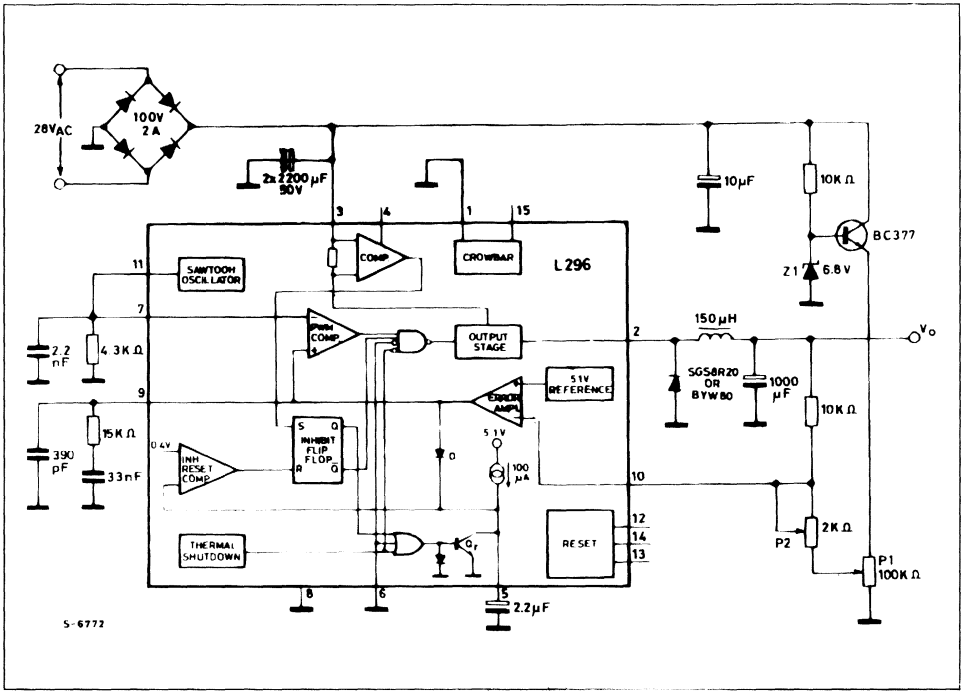


Figure 30 : When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30V.

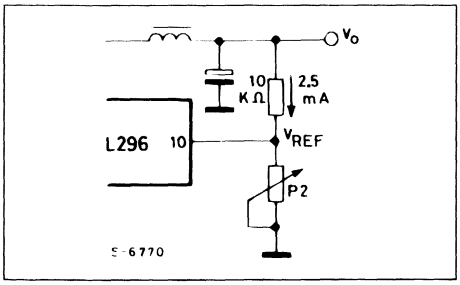


Figure 31 : Partial Schematic showing Output Voltage Adjustment of Figure 29.

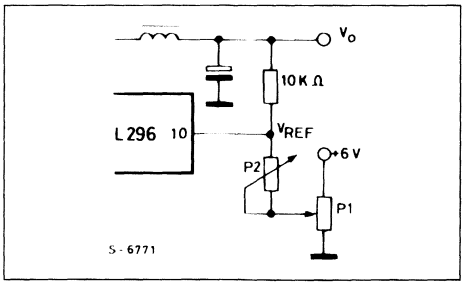
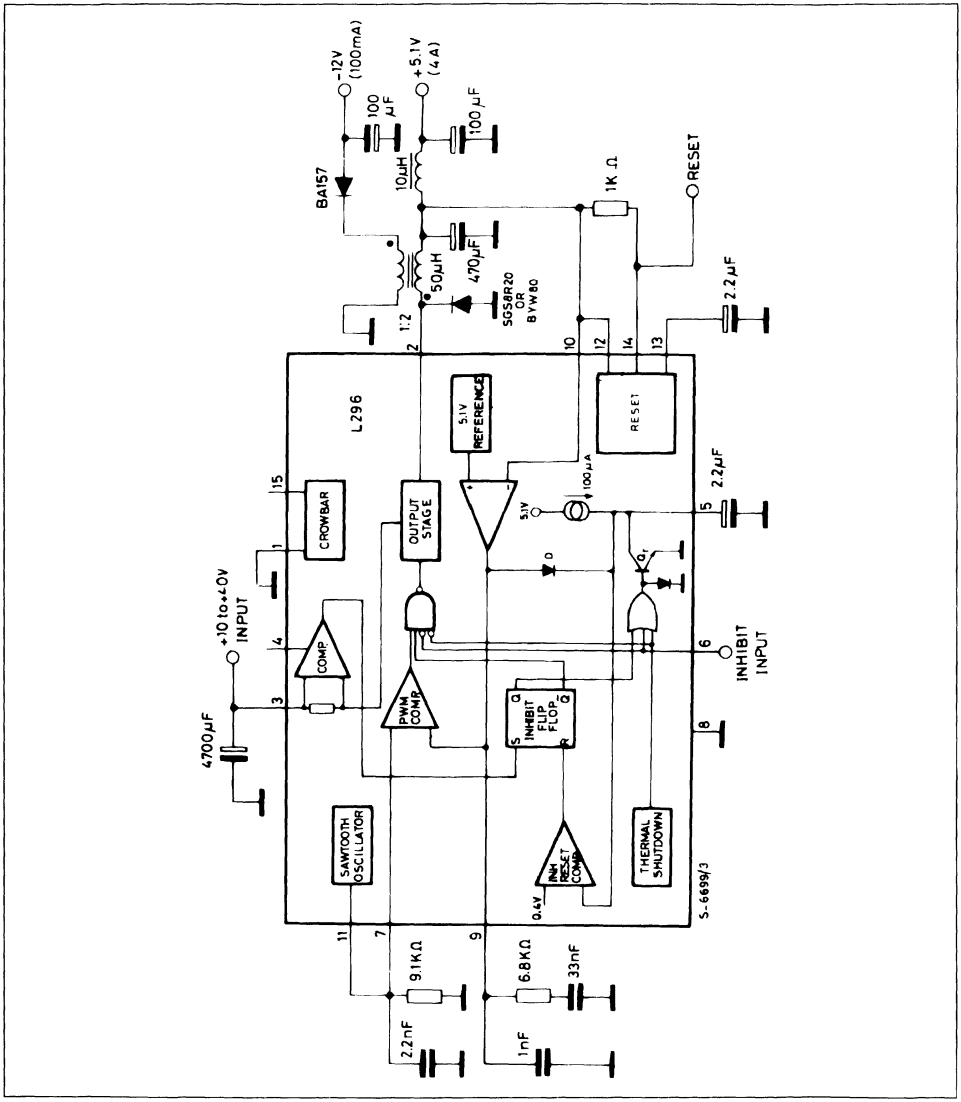


Figure 32 : Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

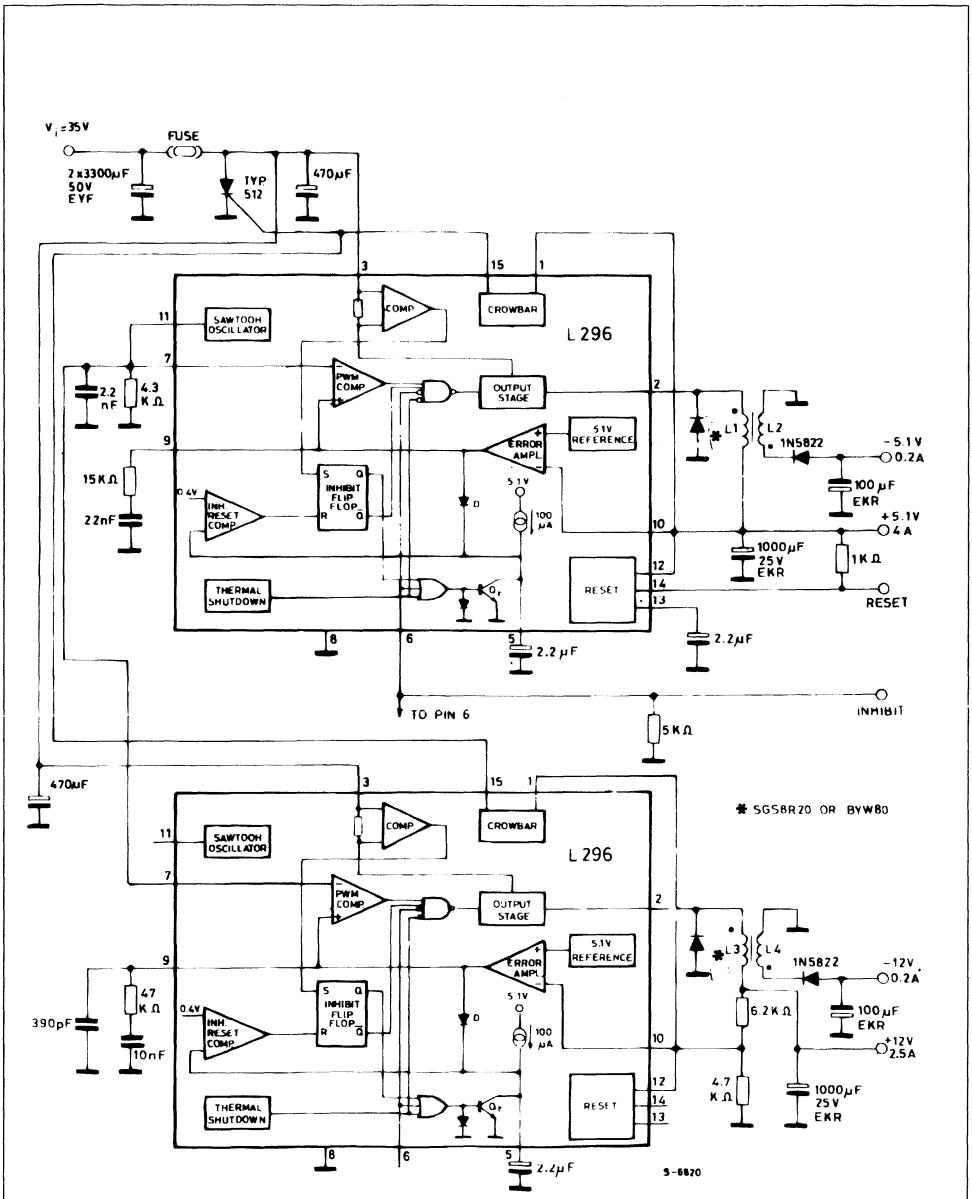
Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

V_{01} = 5.1V/4A

V_{02} = 12V/2.5A (up o 4A)
V_{03} = – 5V/0.2A
V_{04} = – 12V/0.2A

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

Figure 33 : Microcomputer Supply with 5V, – 5V, 12V and – 12V Outputs.



The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage (± 2%). For the 12 V output, by using a resistive divider with 1 % resistance an output is obtained whose spread is within ± 4%.

The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together ; the 5KΩ resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

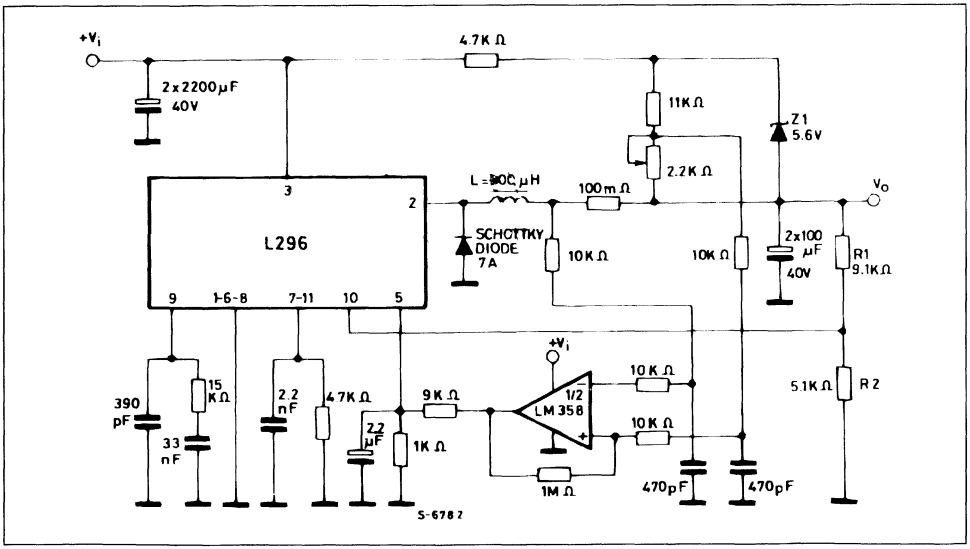
As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types (trr < 50nsec) ; should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is available, which is large enough for batteries up to 40-45Ah (for 12V type). With reference to the electric diagram through the 2KΩ potentiometer the max output current is set, while through the $R_1 - R_2$ output divider the voltage is set. (R_1 may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Figure 34 : Battery charger circuit illustrating how the device is used to regulate the output current.



HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{IDC} which has a low value when compared to I_o is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{IDC}$ (assuming the device has an ideal efficiency), it follows that $I_{IDC} = I_o (T_{ON}/T)$.

Assuming to be :

V_o = 5V I_o = 4A and $V_3 \approx$ 37V

it follows that :

$$T_{ON} / T = V_o / V_i = \frac{5}{37} = 0.135$$

I_{iDC} = 4 x 0.135 = 0.54A.

With input voltage 50V and I_o = 4A, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74% ; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{iDC} reduces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptably low.

MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

Figure 35 : The maximum input voltage can be raised above 46V by adding a transistor as shown here.

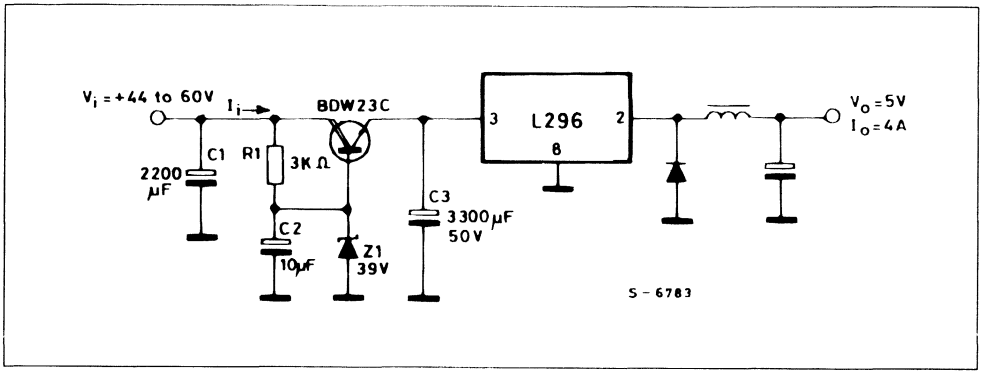
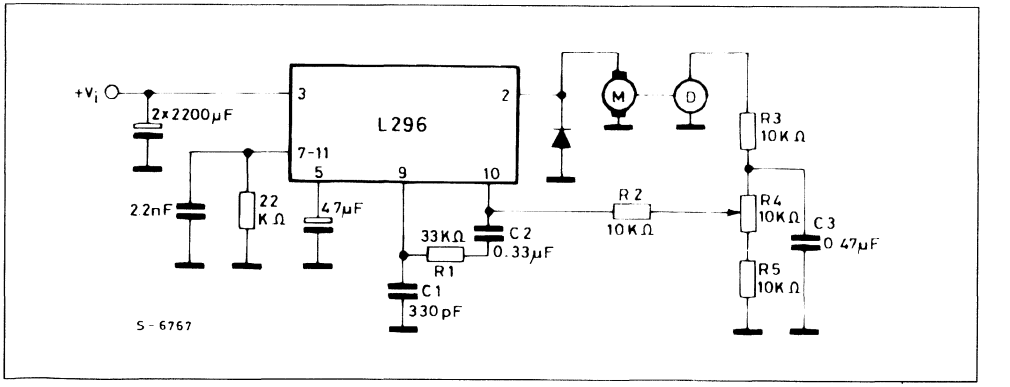


Figure 36 : With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.



HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40kHz to prevent the device from loosing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways : through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat} ; when the resistor is connected in series to the collector V_{CE} is reduced ; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Figure 37 : The output current may be increased by adding a power transistor as shown in this circuit.

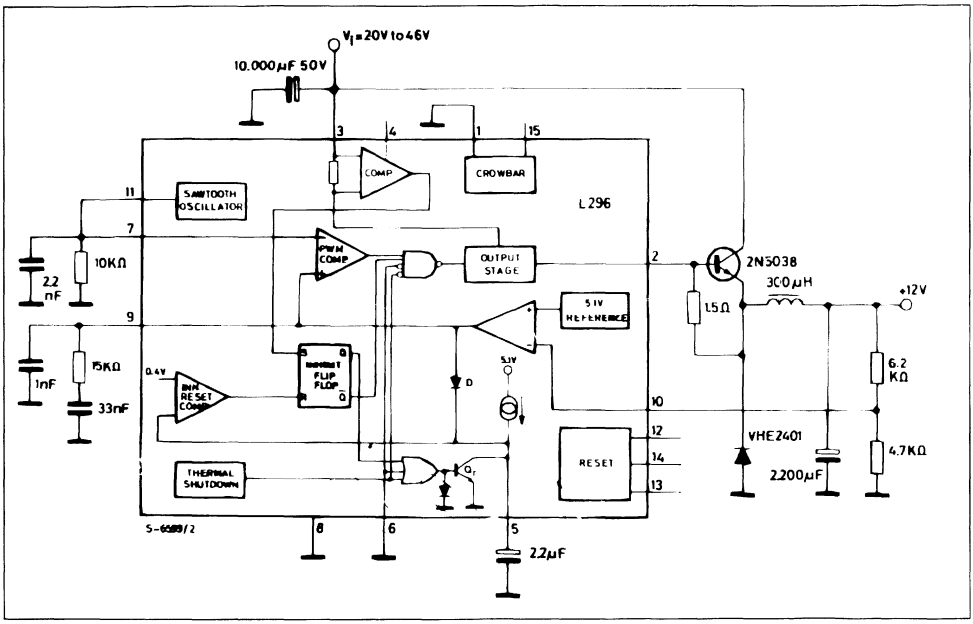


Figure 38 : This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

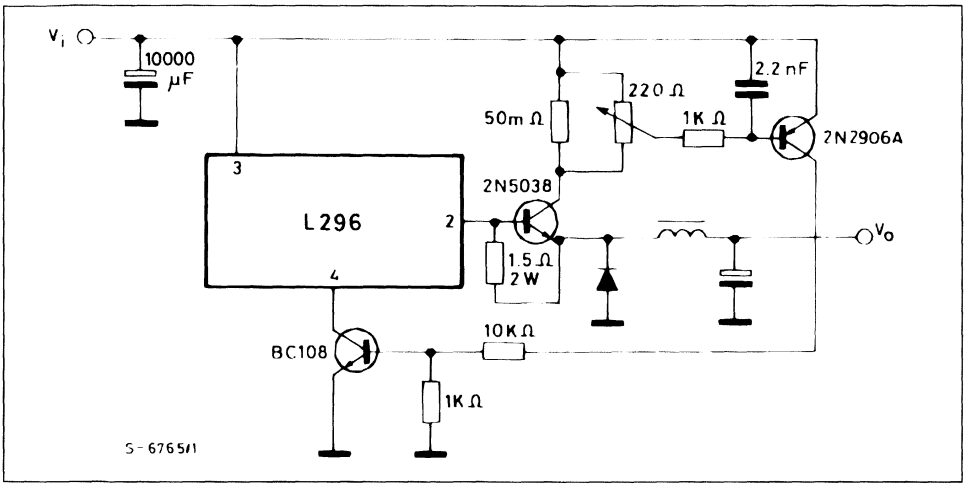
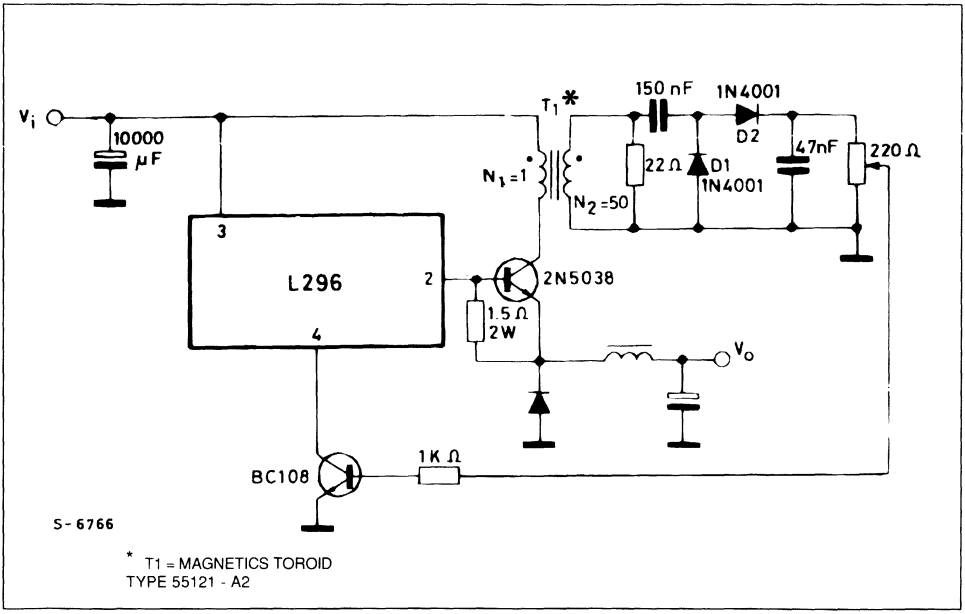


Figure 39 : A small transformer is used in this example for current limiting.



STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R_7.

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by :

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is :

$$I_{peak} = \frac{V_i}{L} T_{ON}$$

Figure 40 : A Step-up Converter using a Power MOS Transistor.

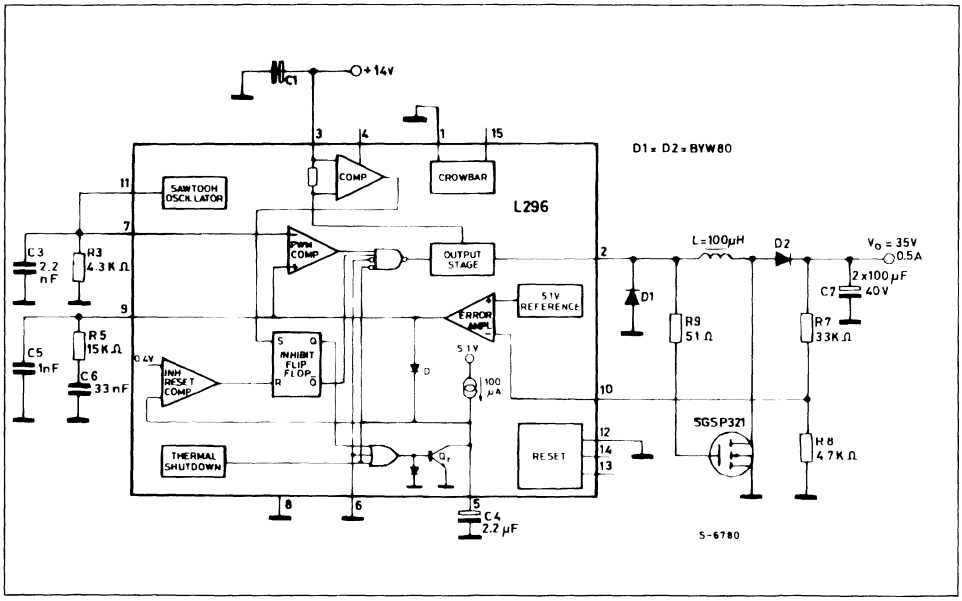
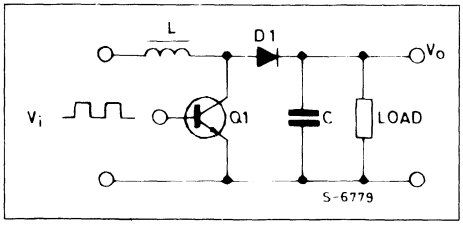


Figure 41 : Basic Schematic for Step-up Configurations.



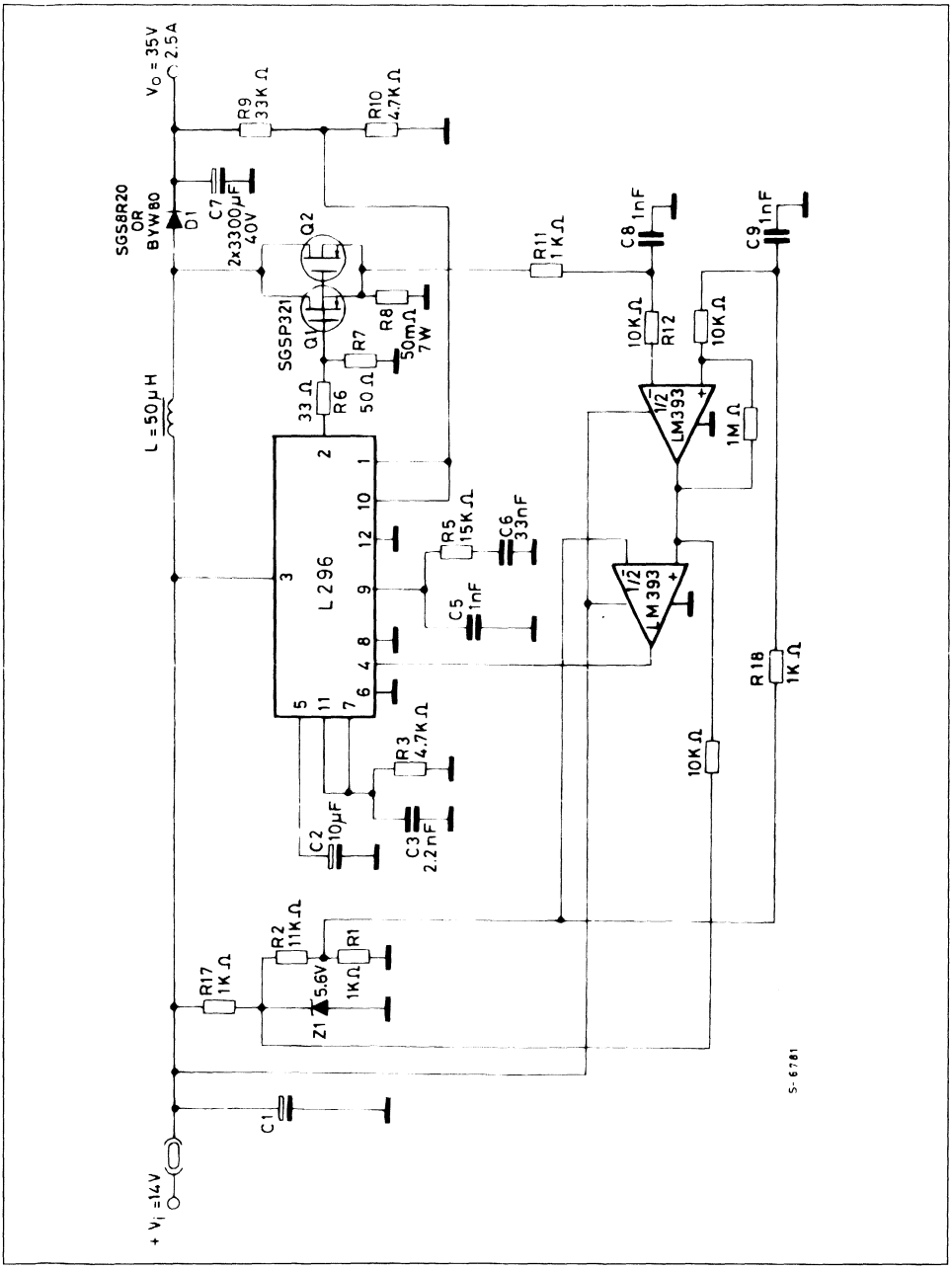
In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used :

$$\frac{1}{2} L I^2_{peak} = V_o I_o T$$

$$I_o = \frac{L I2_{peak}}{2 V_o T} = \frac{V_i^2 T_{ON}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

Figure 42 : High power step-up converter showing how the current limiting function is realized externally.



LAYOUT CONSIDERATIONS

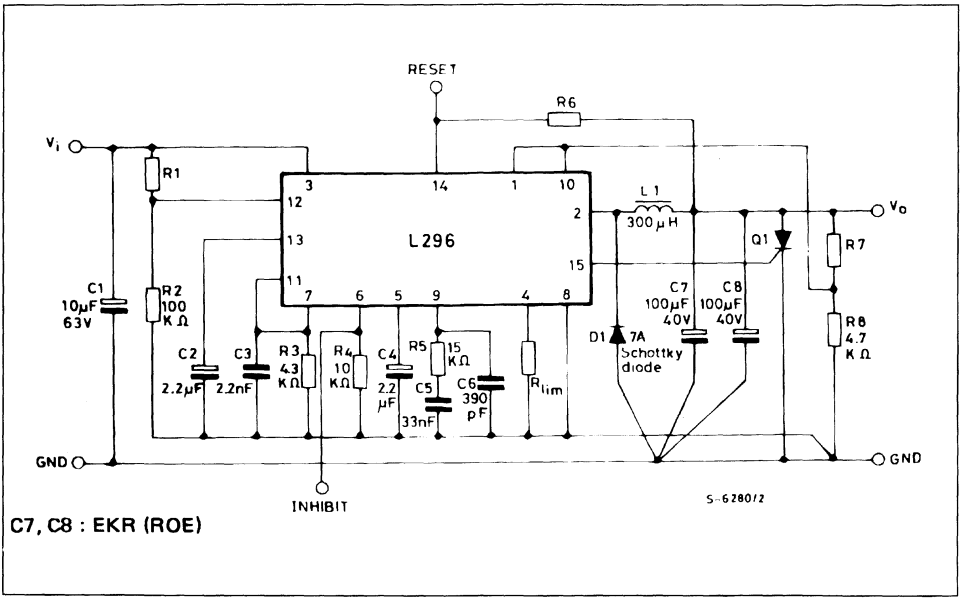
Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

Figure 43 : Typical application circuit showing how the signal and power grounds are connected.



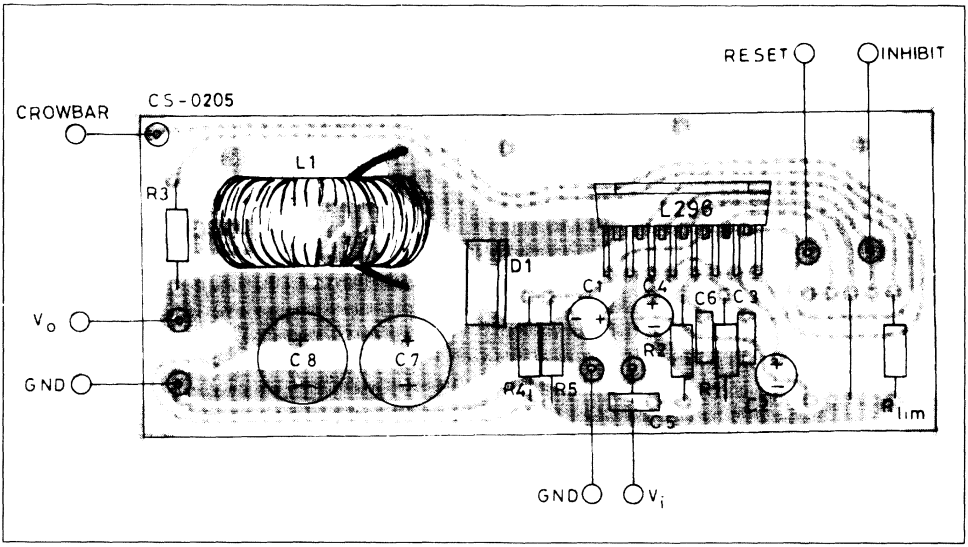
C7, C8 : EKR (ROE)

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.	
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Value for Standard Output Voltages		
V_O	R_8	R_7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ
24 V	4.7 kΩ	18 kΩ

Figure 44 : A Suitable PCB Layout for the Figure 43 Circuit realized in Accordance with the Suggestions in the Text (1 : 1 scale).



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reacing values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life ; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 45 shows the structure of a power device. As demonstrated in thermo-dynamics, a thermal circuit can be considered to be an electrical circuit where R_1, R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

C1, C2 are the thermal capacitance (expressed in °C/W)
I is the dissipated power
V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where :

C_c is the thermal capacitance of the die plus that of the tab.
C_h is the thermal capacitance of the heatsink
R_{jc} is the junction case thermal resistance
R_h is the heatsink thermal resistance

Figure 45.

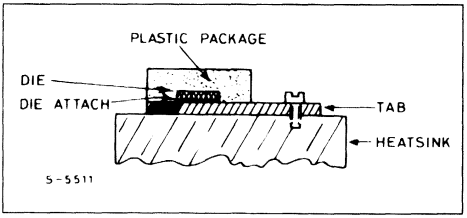


Figure 46.

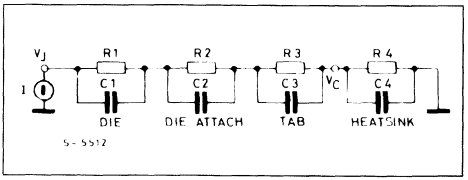
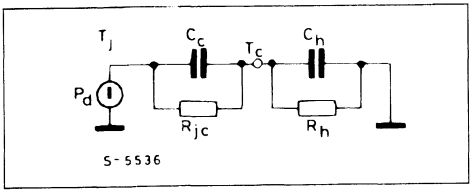
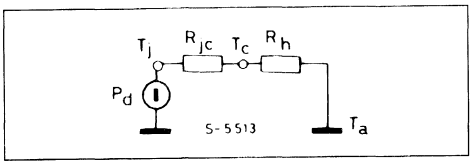


Figure 47.



But since the aim of this section is not that of studing the transistors, the circuit can be further reduced as shown in figure 48.

Figure 48.



If we now consider the ground potential as ambient temperature, we have :

$$T_j = T_a + (R_{jc} + R_h)\, P_d \qquad a)$$

$$R_h = \frac{T_j - T_a - R_{jc}\, P_d}{Pd} \qquad b)$$

$$T_c = T_a + R_h\, Pd \qquad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5°C/W ; with silicone grease roughly 0.3°C/W and with silicone grease plus a mica insulator about 0.4°C/W. See fig. 49. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperature can be calculated by solving the circuit shown in fig. 50. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices :

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Figure 49.

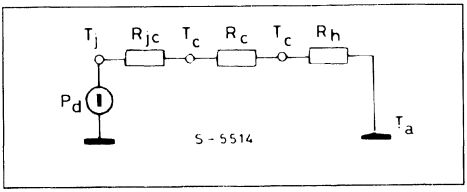


Figure 50.

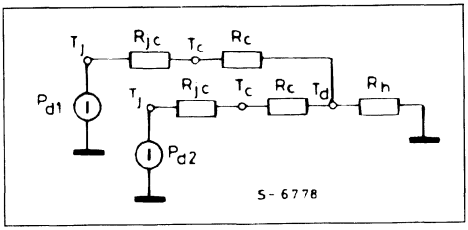


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Figure 51.

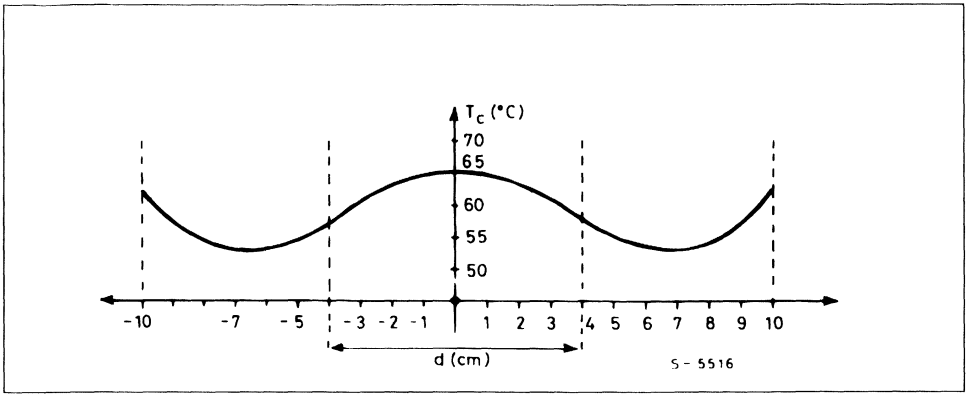
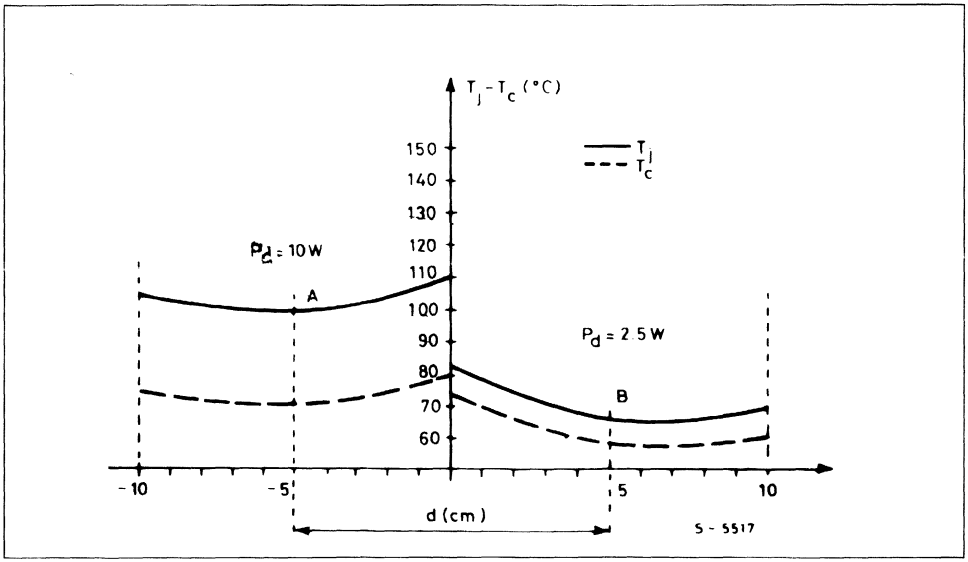


Figure 52.



APPENDIX A

CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

Figure A1 shows the entire control system of the switching regulator.

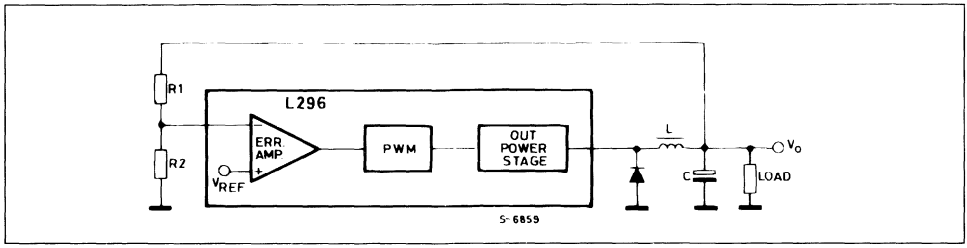
The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect. The characteristics of LC filter affect the output voltage waveforms ; is generally much less than an order of magnitude below the switching frequency.

Figure A1 : The Control Loop of the Switching Regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_o to V_i is :

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage , ΔV_O, giving :

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently :

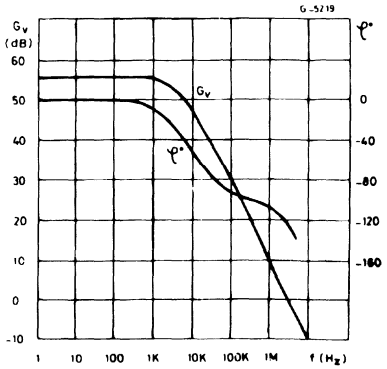
$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by :

$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i.

Figure A2 : Open Loop Frequency and Phase Response of Error Amplifier.



The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

In the application a series RC network is recommended which gives high system gain at low frequency - to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7kHz and a phase shift which reaches about – 90° at frequencies around 1MHz.

The introduction of a series network R_C C_C between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Figure A3 : Compensation Network of the Error Amplifier.

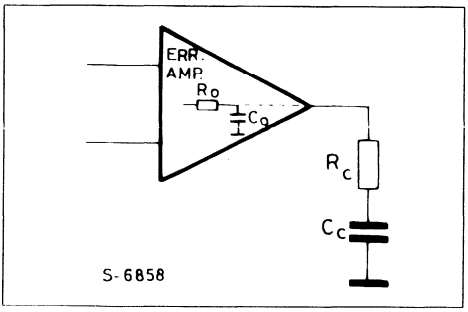
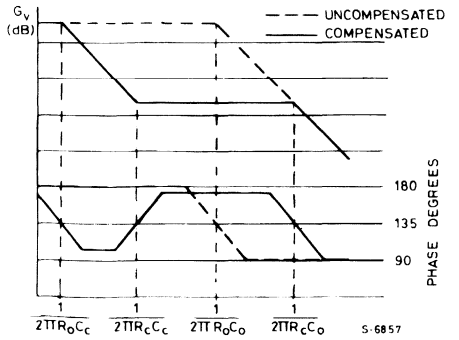


Figure A4 : Bode Plot Showing Gain and Phase of Compensated Error Amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is :

$$G_{EA} = g_m Z_c = \frac{1 + s R_C C_C}{s C_C} \quad (gm = \frac{1}{2500})$$

The DC gain must be considered equal to :

$A_o = g_m R_o$

PWM block and output stage :

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER :

$$G_{LC} = \frac{1 + s C \cdot ESR}{s^2 LC + s C ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

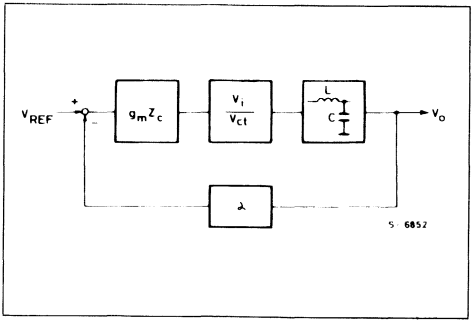
Feedback : consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Figure A5 : Block Diagram Used in Stability Calculation.



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performancen, once the frequency is fixed, are calculated with the following formulae :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

$$C = \frac{(V_i - V_o)\, V_o}{8L\, f^2\, \Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the $R_c\, C_c$ network in the same place :

$$\omega_z = \frac{1}{R_C\, C_C}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the $R_c\, C_c$ network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_c so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency :

$$w_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in figure A7.

Figure A6 : Bode Plot of System Taking Filter and Compensation Network into Account.

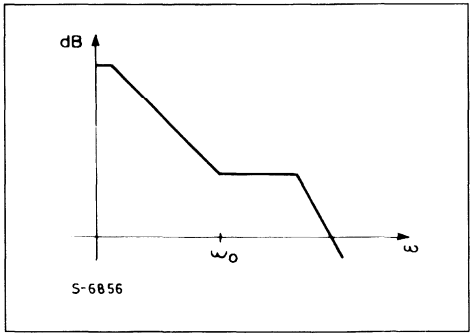
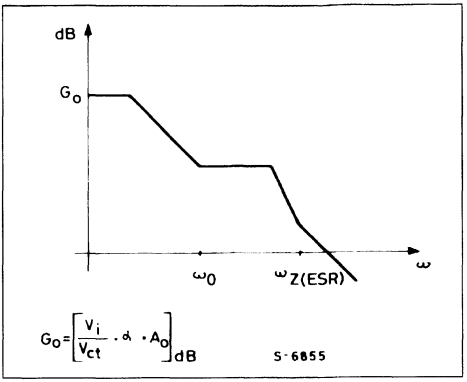


Figure A7 : Bode Plot of Complete System Taking into Consideration the Equivalent Series Resistance of the Output Capacitor.



DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_o, the overall open-loop gain of the system is :

$$A_t = A_o \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes :

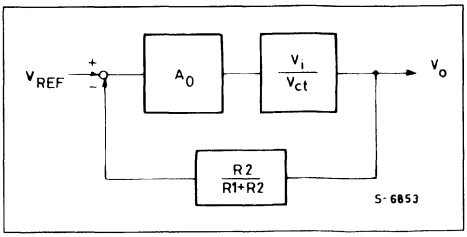
$$A_t = A_o \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i, from the literature we obtain :

$$\frac{\Delta V_o}{V_o} = \frac{\frac{\Delta V_i}{V_i}}{\frac{A_o\, V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}$$

This espression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Figure A8 : Block Diagram for Calculation of Line Regulation.



APPENDIX B

REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (trr) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences - RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with $V_o = 5.1V$ and $I_o = 4A$. The switching frequency is 100kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a 0.01µF/250V ~ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124). Measurements have also been performed beyond 30MHz ; the maximum value measured is still well below the limit curve.

Figure B1 : EMI Measurements with a Capacitor Connected across the Primary Transformer with Screen Grounded (A)

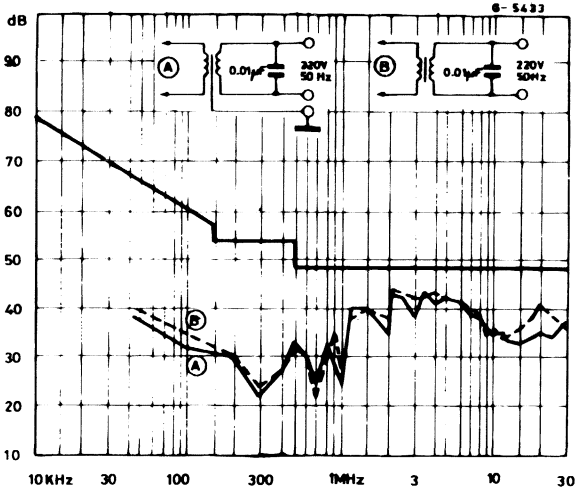
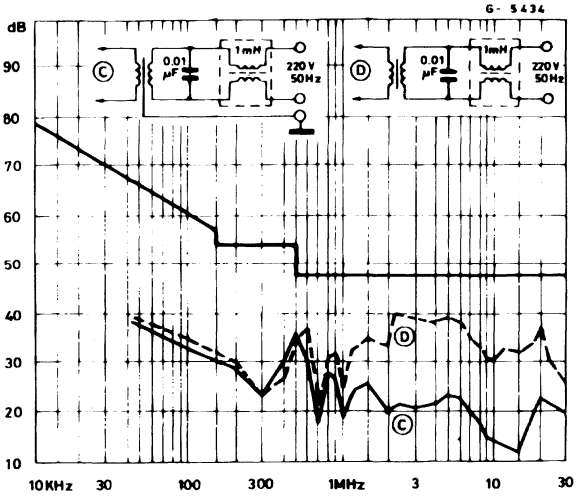


Figure B2 : EMI results with the addition of an inductive filter on the mains input.

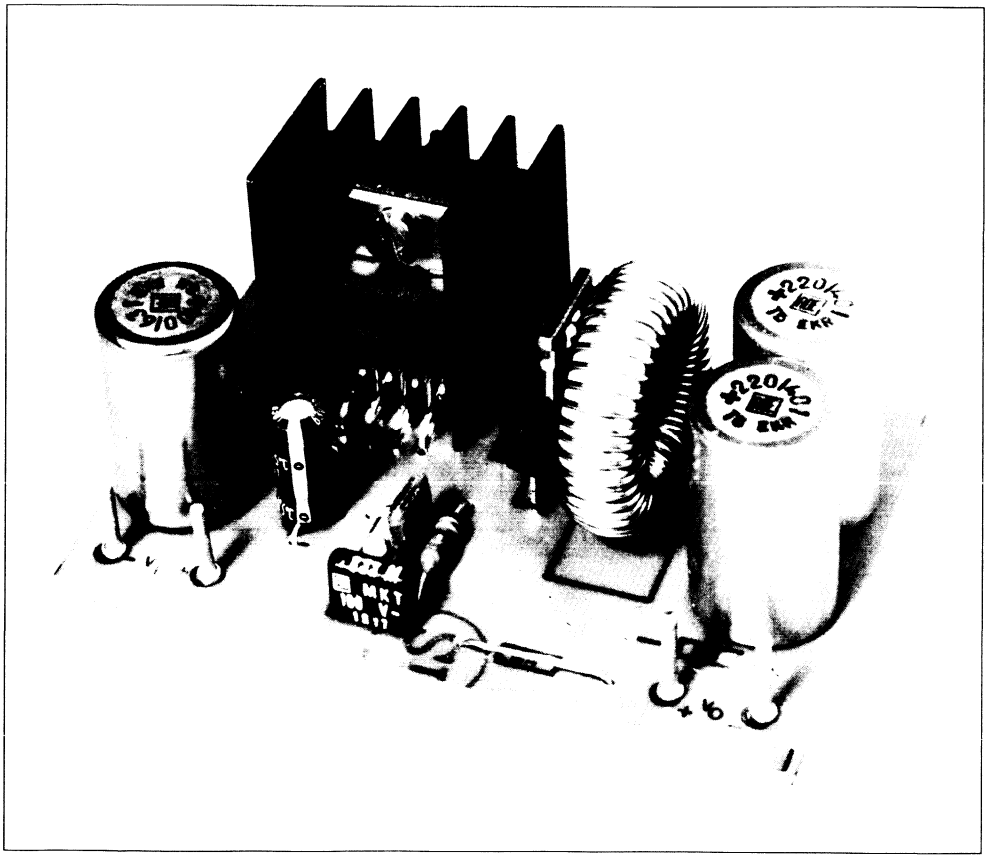


SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING MULTIPLE-OUTPUT POWER SUPPLIES WITH THE L296 AND L4960

Multiple output supplies can be realized simply and economically using the SGS THOMSON Microelectronics L296 and L4960 high power switching regulators. This note describes several practical circuits of this type.



Most of the switching regulators produced today have multiple outputs. The output voltages most frequently used - at least for powers up to 50W - are + 5V – 5V, + 12V and – 12V. In these supplies the 5 V output is normally the output which delivers the highest current and requires the highest precision. For the other voltages - particularly the negative outputs - less precision (± 5 % ± 7 %) is usually sufficient. Often, however, for high current 12V outputs better stabilization and greater precision (typically ± 4 % - the output tolerance of an L7800 series linear regulator) are required.

Multiple output supplies which satisfy these requirements can be realized using the SGS THOMSON L296 and L4960 high power switching regulator ICs, Several practical supply designs are described below to illustrate how these components are used to build compact and inexpensive multi-output supplies.

DUAL OUTPUT 15W SUPPLY

V_{o1} = 5V/3A, V_{o2} = 12V/150mA

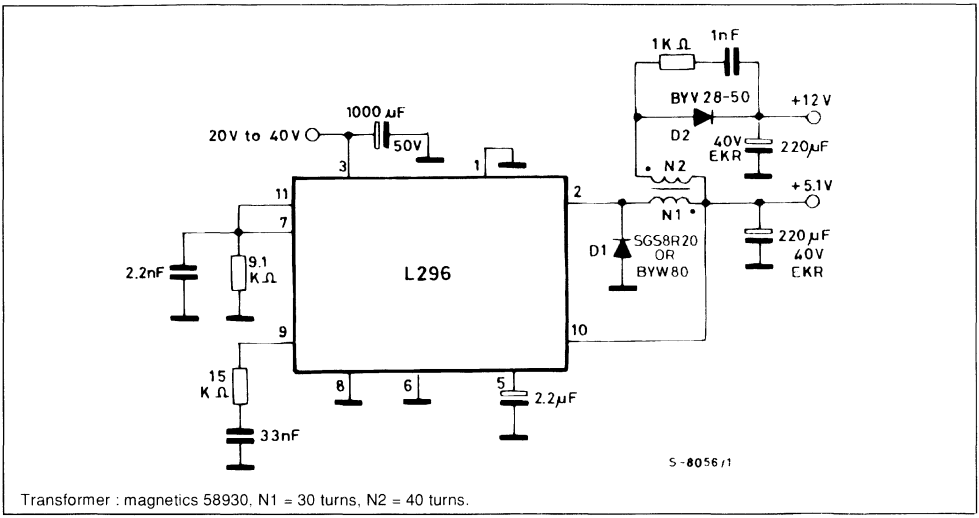
A single L296 is used in this application to produce two outputs. The application circuit, figure 1, illustrates how the second output (12V) is obtained by adding a second winding to the output inductor. Energy is transferred to the secondary during the recirculation period when the internal power device of the L296 is OFF.

Since the 12V output is not separated from the 5V output fewer turns are necessary for the second winding, therefore less copper is needed and load regulation is improved.

In applications of this type it is a good rule to ensure that the power drain on the auxiliary output is no more than 20-25% of the power delivered by the main output.

Table 1 shows the performance obtained with this dual output supply. This circuit operates at a switching frequency of 50KHz.

Figure 1 : Dual Output DC-DC Converter (5V/3A, 12V/150mA).



Transformer : magnetics 58930, N1 = 30 turns, N2 = 40 turns.

Table 1.

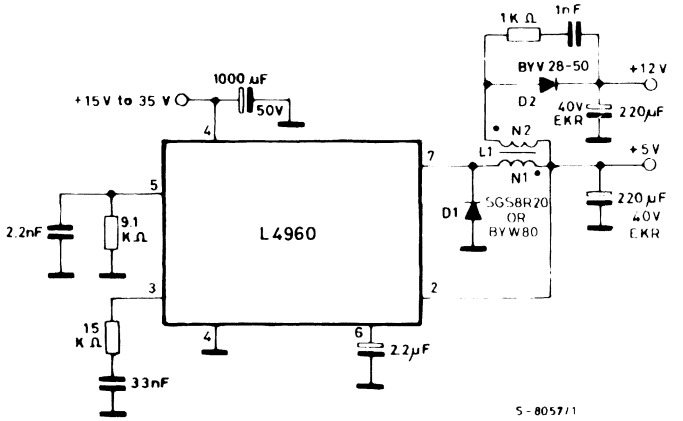
Parameter		V_{O1}	V_{O2}	Unit
Output Voltage I_{O1} = 3A	V_i = 30V I_{O2} = 150mA	5.120	12.089	V
Output Ripple		70	40	mV
Line Regulation I_{O1} = 3A	20V ≤ V_i ≤ 40V I_{O2} = 150mA	15	30	mV
Line Regulation I_{O1} = 700mA	20V ≤ V_i ≤ 40V I_{O2} = 100mA	15	10	mV
Load Regulation I_{O1} = 700mA ⇢ 3A	V_i = 30V I_{O2} = 150mA	10	130	mV
Load Regulation I_{O1} = 700mA	V_i = 30V I_{O2} = 100 ⇢ 150mA	0	40	mV
Load Regulation I_{O1} = 3A	V_i = 30V I_{O2} = 100 ⇢ 150mA	0	40	mV
Efficiency	V_i = 30V V_{O1} = 5.120V I_{O1} = 3A V_{O2} = 12.089V I_{O2} = 150mA	75		%

DUAL OUTPUT 7.5W SUPPLY

V_{o1} = 5V/1.5A, V_{o2} = 12V/100mA

The same technique - adding a secondary winding - can also be used to produce an economical and simple dual output supply with the L4960, a device containing the same control loop blocks as the L296 and a 2A output stage (fig. 2). Though this circuit costs very little the performance obtained (see table 2) is more than satisfactory. The switching frequency is 50kHz.

Figure 2 : Dual Output DC-DC Converter (5V/1.5A, 12V/100mA).



Transformer : magnetics 58206, N1 = 30 turns, N2 = 40 turns.

Table 2.

Parameter		V_{O1}	V_{O2}	Unit
Output Voltage I_{O1} = 1.5A	V_i = 25V I_{O2} = 100mA	5.050	12.010	V
Output Ripple		50	30	mV
Line Regulation I_{O1} = 1.5A	15V ≤ V_i ≤ 35V I_{O2} = 100mA	7	75	mV
Line Regulation I_{O1} = 500mA	15V ≤ V_i ≤ 35V I_{O2} = 50mA	7	60	mV
Load Regulation I_{O1} = 0.5A → 1.5A	V_i = 25V I_{O2} = 100mA	3	100	mV
Load Regulation I_{O1} = 500mA	V_i = 25V I_{O2} = 50mA → 100mA	0	55	mV
Load Regulation I_{O1} = 1.5A	V_i = 25V I_{O2} = 50mA → 100mA	0	50	mV
Efficiency	V_i = 25V V_{O1} = 1.5V V_{O2} = 100mA	78		%

TRIPLE OUTPUT 15W SUPPLY

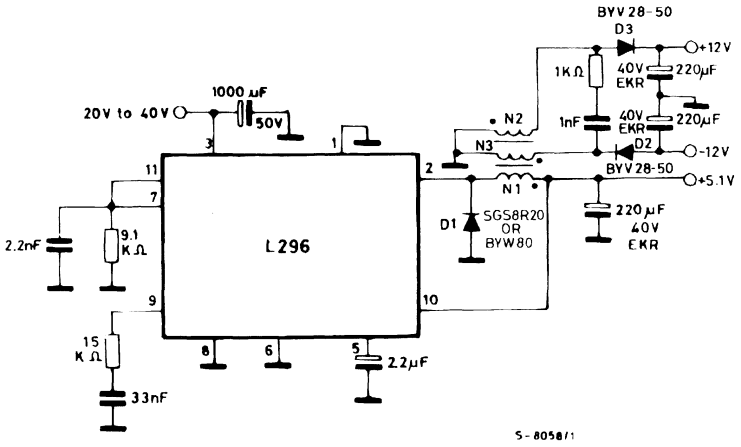
V_{o1} = 5V/3A, V_{o2} = 12V/100mA, V_{o3} = -12V/100mA

Figure 3 shows how to obtain two auxiliary outputs (± 12V) which are isolated from the 5V output. For this output power range an L296 is used.

To ensure good tracking of the 12V and - 12V outputs the secondary outputs in this application should be bifilar wound.

This circuit operates at 50KHz and gives the performance indicated in table 3.

Figure 3 : Triple Output DC-DC Converter (5V/3A, 12V/100mA).



Transformer : magnetics 58206, N1 = 30 turns, N2 = 40 turns.

Table 3.

Parameter		V_{O1}	V_{O2}	V_{O3}	Unit
Output Voltage I_{O1} = 3A	V_i = 30V $I_{O2} = I_{O3}$ = 100mA	5.057	12.300	– 12.300	V
Output Ripple		80	30	30	mV
Line Regulation I_{O1} = 700 mA	20V ≤ V_i ≤ 40V $I_{O2} = I_{O3}$ = 100mA	15	60	60	mV
Line Regulation I_{O1} = 3A	20V ≤ V_i ≤ 40V $I_{O2} = I_{O3}$ = 100mA	18	100	100	mV
Load Regulation I_{O1} = 0.7A → 3A	V_i = 30V $I_{O2} = I_{O3}$ =100mA	4	150	150	mV
Load Regulation I_{O1} = 3A	V_i = 30V I_{O2} = 100mA I_{O3} = 50 → 100mA	0	125	52	mV
Load Regulation I_{O1} = 3A I_{O2} = 50 → 100mA	V_i = 30V I_{O3} = 100mA	0	50	120	mV
Efficiency			76		%

TRIPLE OUTPUT 7.5W SUPPLY

V_{o1} = 5V/1.5A, V_{o2} = 12V/50mA, V_{o3} = – 12/50mA

For lower output powers, the L296 in the previous application may be replaced by an L4960 as shown in figure 4. The performance of this circuit is indicated in table 4.

Figure 4 : Triple Output DC-DC Converter (5V/1.5A, 12V/50mA, – 12V/50mA).

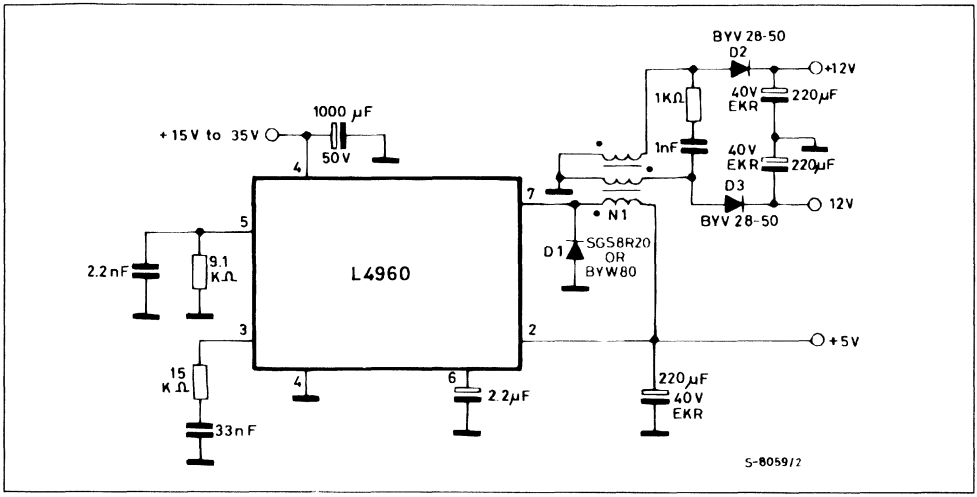


Table 4.

Parameter		V_{o1}	V_{o2}	V_{o3}	Unit
Output Voltage I_{o1} = 1.5A	V_i = 25V $I_{o2} = I_{o3}$ = 50mA	5.040	12.020	– 12.020	V
Output Ripple		60	30	30	mV
Line Regulation I_{o1} = 500mA	15V ≤ V_i ≤ 35V $I_{o2} = I_{o3}$ = 50mA	5	80	80	mV
Line Regulation I_{o1} = 1.5A	15V ≤ V_i ≤ 35V $I_{o2} = I_{o3}$ = 50mA	4	60	60	mV
Load Regulation I_{o1} = 0.5A → 1.5A	V_i = 25V $I_{o2} = I_{o3}$ = 50mA	5	120	120	mV
Load Regulation I_{o1} = 1.5A I_{o3} = 20 → 50mA	V_i = 25V I_{o2} = 50mA	0	15	50	mV
Load Regulation I_{o1} = 1.5A I_{o2} = 20 → 50mA	V_i = 25V I_{o3} = 100mA	0	50	15	mV
Efficiency		70			%

THE L296 AND L4960 HIGH POWER SWITCHING REGULATORS

The SGS THOMSON L296 is a monolithic stepdown switching regulator assembled in the 15-pin Multiwatt package. Operating with supply input voltages up to 46V it provides a regulated 4A output variable from 5.1V to 40V.

Internally the device is equipped with current limiter, soft start and reset (or power fail) functions, making it particularly suitable for supplying microprocessors and logic.

The precision of the L296's internal reference (± 2%) eliminates the need for external dividers or trinning to obtain a 5V output.

The synchronization pin allows synchronous operation of several devices at the same frequency to avoid generating undesirable beat frequencies.

The L4960 is a similar device assembled in the 7-lead Heptawatt package. Like the L296 it has a maximum input voltage of 46V and it provides a regulated output voltage variable from 5V to 40V with a maximum load current of 2.5A. Current limiting, soft start and thermal protection functions are included.

The thermal protection circuit in both the L296 and L4960 has a hysteresis of 30°C to allow soft restarting after a fault condition.

THE STEP DOWN CONFIGURATION

Figure 5 shows the basic structure of a step down switching regulator. The transistor Q is used as a switch and the ON and OFF times are determined by the control circuit.

When Q is saturated current flows from the supply, Vi, to the load through the inductor L. Neglecting the saturation voltage of Q, Ve ≅ Vi.

When Q is OFF, current continues to flow in the inductor L, in the same direction, forcing the diode into conduction immediately therefore Ve is negative. In these conditions the load current flows through L and D.

The average value of the current in the inductor is equal to the load current. In the inductor a triangular current ripple equal to . ΔI_L is added to this average current.

During the time when Q is ON this ripple is :

$$\Delta I_L = \frac{(V_i - V_o)\, T_{ON}}{L}$$

and when Q is off it is :

$$\Delta I_L = \frac{V_o \cdot T_{OFF}}{L}$$

Equating these expression and assuming that the transistor and diode are ideal we obtain :

$$V_o = V_i \cdot \frac{T_{ON}}{T}$$

T_{ON} is the conduction time of the transistor

T is the oscillator period

The absolute average current in the supply is therefore :

$$I_{ioc} = I_o \cdot \frac{T_{ON}}{T}$$

Once the working frequency and desired ripple current have been fixed the value of the inductor L is given by :

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

and the value of the capacitor C required to give the desired output voltage ripple (Δ V) is :

$$C = \frac{(V_i - V_o)\, V_o}{8\, L\, f^2\, \Delta f_o}$$

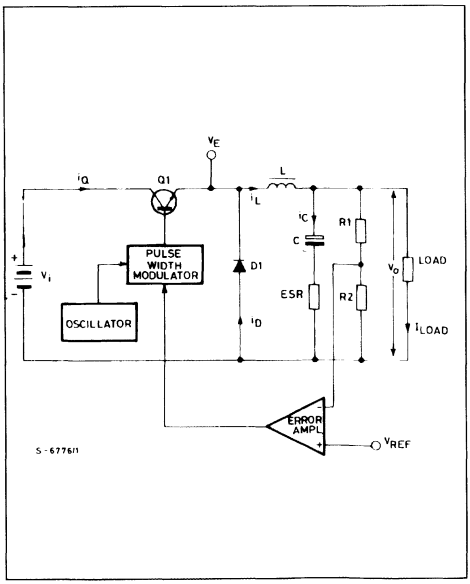
This capacitor must have a maximum ESR given by :

$$ESR_{MAX} = \frac{\Delta V_o}{\Delta I_L}$$

And, finally, the minimum load current, I_{OMIN}, must be :

$$I_{OMIN} = \frac{\Delta I_L}{2} = \frac{(V_i - V_o)\, V_o}{2\, V_i\, f_L}$$

Figure 5 : Basic STEP-DOWN Configuration.



30W DC-DC CONVERTER

Designing power supplies in the 30-40W range is becoming increasingly difficult because it is here that there is the greatest need to maintain performance levels and reduce costs. The application proposed here is very competitive because it exploits new ICs to reduce size, number of components and assembly costs.

This solution, the DC-DC converter, compares very favourable with off-line switching supplies in terms of cost. DC-DC converters can, in fact, be realized even by designers with little experience and allows the convenience of working with low voltages, Off-line switching supplies are only preferable when the weight and size of the mains transformer in a DC-DC converter would be excessive.

In this circuit, figure 6 two devices are used, an L296 and an L4960. The L296 is used, to supply a 5V output with a current of 3A and the auxiliary – 5V/100mA output and the L4960 is used to provide the 12V/1.5A output and the auxiliary – 12V/100mA output.

Figure 6 : Multioutput DC-DC Converter with L296 and L4960 (5V / 3A, 12V / 1.5A, –12V/100mA, –5V/100mA).

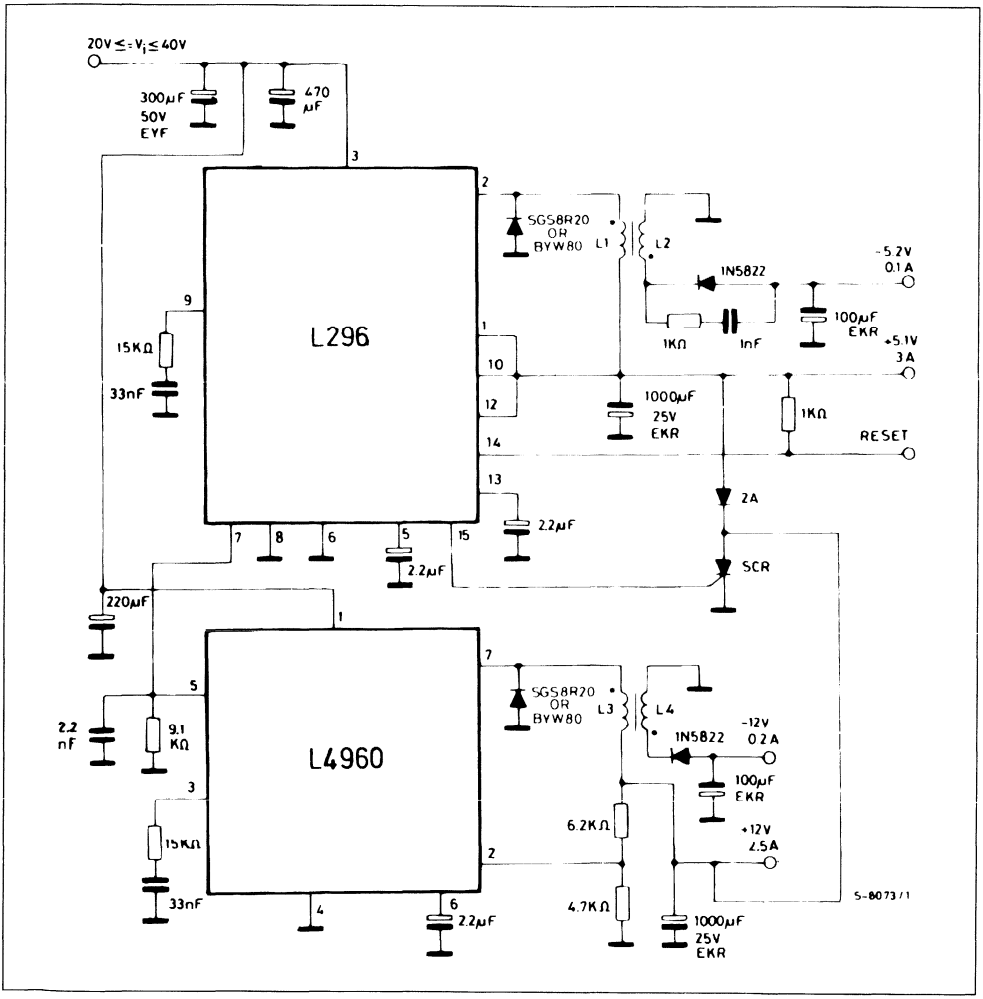


Table 5 shows the performance obtained with this power supply.

Table 5.

Parameter		V_{O1}	V_{O2}	V_{O3}	V_{O4}	Unit
Output Voltage I_{O1} = 3A I_{O2} = 100mA	V_i = 30V I_{O3} = 1.5A I_{O4} = 100mA	5.080	– 5010	11.96	12.00	V
Output Ripple		50	30	50	40	mV
Line Regulation I_{O1} = 1A I_{O3} = 0.5A	20V ≤ V_i ≤ 40V I_{O2} = 100mA I_{O4} = 100mA	13	15	10	20	mV
Load Regulation I_{O1} = 1A to 3A	V_i = 30V I_{O2} = 100mA	8	90			mV
I_{O3} = 0.5 to 1.5A	I_{O4} = 100mA			3	80	mV
Load Regulation I_{O1} = 3A	V_i = 30V I_{O2} = 50 → 100mA	0	100			mV
I_{O3} = 1.5A	I_{O4} = 50 → 100mA			0	100	mV
Load Regulation I_{O1} = 1A	V_i = 30V I_{O2} = 50 → 100mA	0	35			mV
I_{O3} = 0.5A	I_{O4} = 50 → 100mA			0	90	mV
Line Regulation I_{O1} = 3A	20 ≤ V_i ≤ 40V I_{O2} = 100mA	15	45			mV
I_{O3} = 1.5A	I_{O4} = 100mA			15	40	mV

This application illustrates how two devices may be synchronized. Note also that the reset circuit is used in this case to monitor the output voltage (see figure 7).

If a power fail function is required in place of the reset function the figure 6 circuit should be modified as shown in figure 8.

Figure 7 : Reset Output Waveforms.

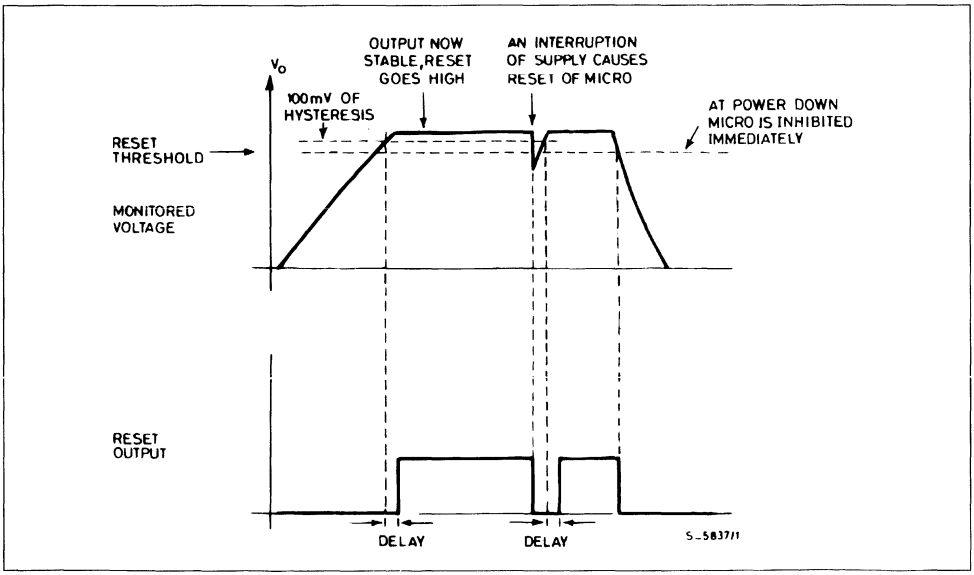
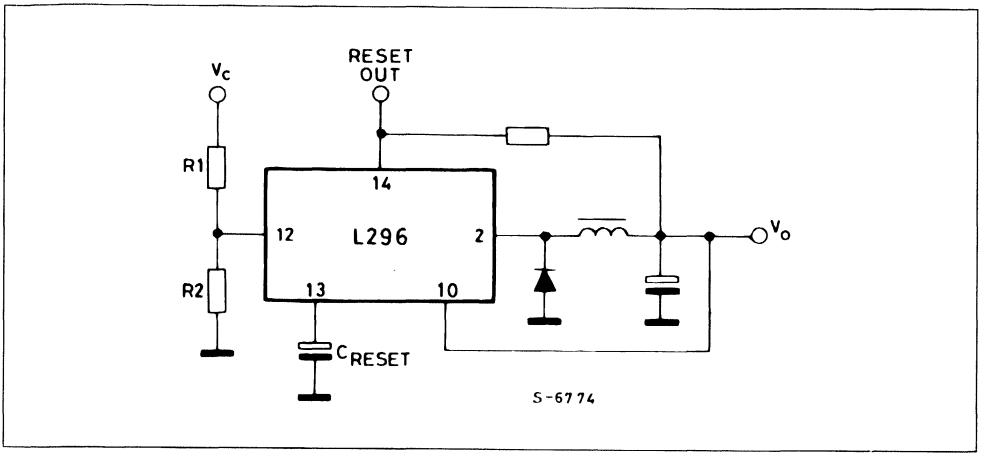


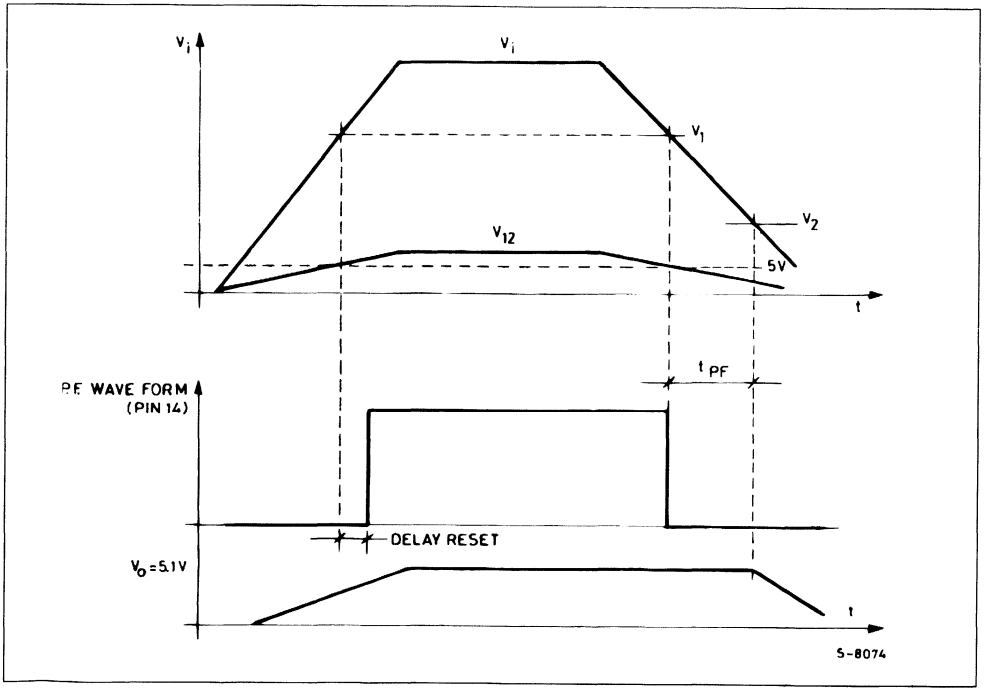
Figure 8.



CALCULATING THE POWER FAIL TIME

The 'power fail time' is defined as the time from when the power fail output (pin 14) goes low to the time when the input voltage falls to the minimum level required to maintain the regulated output (see figure 9). From this definition we can evaluate the energy balance.

Figure 9.



The energy which the filter capacitor C supplies to the operating device while it discharges is :

$$E = 1/2\ C\ (V_1^2 - V_2^2) \qquad (1)$$

The load drains a power of $P_o = V_o\ I_o$. Taking into consideration the average efficiency η (derived with the input between V_1 and V_2), the power to be supplied at the input of the device is :

$$P_{o2} = \frac{P_o}{\eta} \qquad (2)$$

Equating the expressions (1) and (2) gives :

$$1/2\ C\ (V_1^2 - V_2^2) = \frac{P_o}{\eta} \cdot t_{PF}$$

where V_i is the input voltage at which the voltage on pin 12 reaches 5V (through the divider R_1/R_2) ; V_2 is the maximum input voltage below which the device no longer regulates.

Rearranging this expression to obtain C :

$$C = \frac{2\ P_o\ t_{PF}}{\eta\ (V_1^2 - V_2^2)}$$

EXAMPLE - Suppose that V_o = 5V, I_o = 3A, T_{pf} = 10ms and V_i = 35V. Fixing V_1 = 25V and V_2 = 10V we obtain :

$$C = \frac{2\ P_o\ t_{PF}}{\eta\ (V_1^2 - V_2^2)} = \frac{2 \times 15 \times 10\ .\ 10^{-3}}{0.75\ (25^2 - 10^2)} = 760\mu F$$

We obtain choose a capacitor of 1000µF.

CROWBAR

The L296 includes an internal crowbar function ; the only external component needed is an SCR. The intervention threshold of this block is fixed internally at 20% of the nominal value of the internal reference.

In the figure 6 circuit the SCR is triggered by an overvoltage on the 5V output (usually the most important output to monitor) and shortcircuits to ground the 5V output and, through the diode which connects the two outputs, the 12V output.

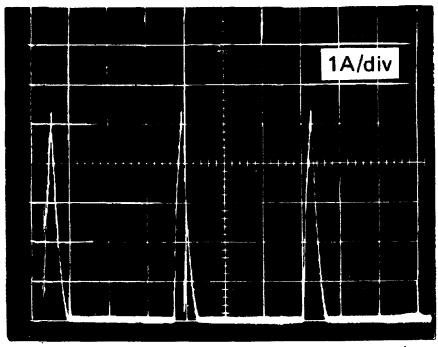
Since the internal current limiter in the device is designed to function as shown in figure 10 (that is, with pulsed output current) the SCR turns off in the gap between pulses and is re-activated gain if, when the device restarts softly, the fault condition has not been eliminated. But if the fault no longer exists the SCR remains OFF and the output voltage returns to the normal value.

If the designer prefers the supply to remain off after the SCR has been activated the circuit can be modified as shown in figure 11. In this modification, when the SCR is triggered a very high current flows in the fuse, blowing it.

Since the filter capacitor can have a high value and be charged to high voltages the choice of SCR is important. The type used in this circuit - the TYP512 - is a plastic packaged SCR able to handle 12 Arms and 300A for 10ms. The maximum forward and reverse voltages are about 50V.

If the crowbar circuit is not used it is advisable to connect pin 1 to ground or pin 10.

Figure 10 : Load Current in Short Circuit Conditions (V_i = 40V, L = 300µH, f = 100KHz).



Current at Pin 2 when the Output is Short Circuited.

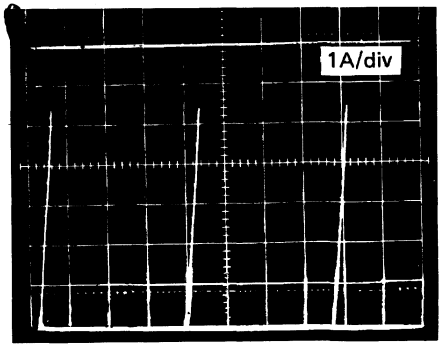
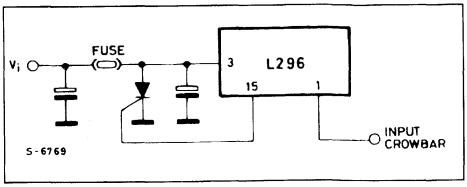


Figure 11.



THE POWER DIP (16+2+2, 12+3+3) PACKAGES

by R. Tiziani

INTRODUCTION

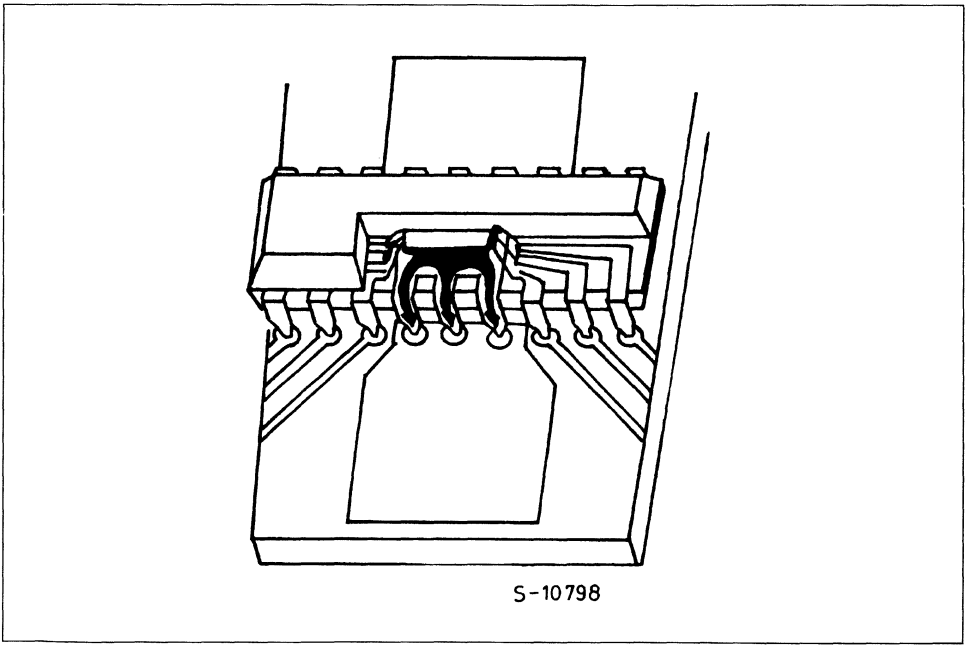
This Application Note is aimed to give a complete thermal characterization of the (16+2+2) power DIP (modified 20 lead DIP with 4 heat transfer leads) and of the (12+3+3) power DIP (modified 18 lead DIP with 6 heat transfer leads) in association with thermal modules integrated on the PCB.

Characterization is performed according with recomendations included in G32-86 SEMI guideline, by means of a dedicated test pattern developed by SGS-THOMSON. It refers to:

1. Junction to pin thermal resistance Rth(j-p)
2. Junction to ambient thermal resistance Rth(j-a)
3. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techiniques.

Figure 1. POWER DIP application on PC board



Experimental conditions

The thermal evaluation was performed by means of the test pattern P638, which is a 80x80 *mils*^{2} die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 3000 *mils*^{2}, with a power capability of 20 W. Measurement method is described in Appendix. A.

Samples with the indicated characteristics were prepared:

Package	DIP (16+2+2)	DIP (12+3+3)
Frame Material	Copper	Copper
Frame Thickness	0.4*mm*	0.4*mm*
Frame Thermal Conductivity	3.9*W/cm*°C	3.9*W/cm*°C

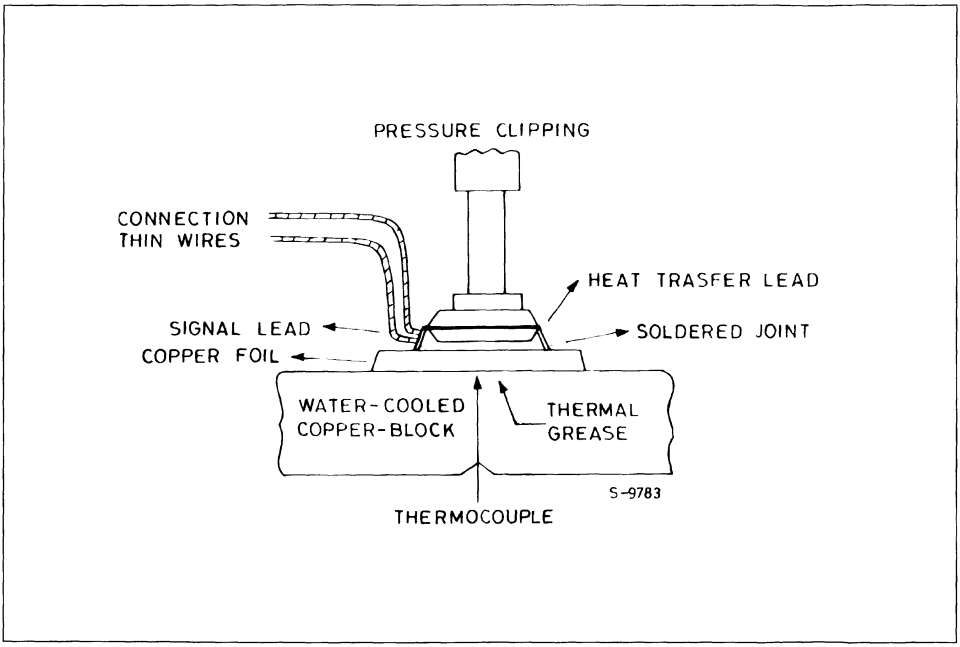
Measurement of junction to pin thermal resistance Rth(j-p) is performed by holding the package (with the heat transfer leads soldered on a copper plate) against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the plate measures the reference temperature.

For junction to ambient thermal resistance Rth(j-a) the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

The effect of "on board" external heat sinks shown in fig. 1 is quantified, using a test board which has two 4 x 4 cm^2 dissipating areas, one of each side of the package. These areas are mechanically reduced in order to study the effect of their size on thermal performance.

The measurement circuit shown in fig. A3 is used for all of the thermal evaluations.

Figure 2. Measurement of Rth(j-p)



JUNCTION TO PIN THERMAL RESISTANCE

The dependance of Rth(j-p) on the dissipated power is negligeable compared to the absolute value: starting from 1 Watt to 10 Watts the Rth(j-p) increases of about 0.5C/W due to the lowering of silicon thermal conductivity with the increasing of temperature. An important contribution to Rth(j-p) is given by the silicon die and in fig. 3,4 is showed the relationship between Rth(j-p) and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

In the figures two curves area reported: the lower one is referring the Rth(j-p) measured at the pin stand-off, the upper one is referring to the Rth(j-p) measures at 1.5 mm from the pin stand-off (1.5 mm is the typical thickness of FR4 board).

The upper curve must be used for the application in which the heat sink is placed in the lower side of PCB and the lower curve must be used when the heat sink is placed on the upper side of PCB.

Figure 3 - POWER DIP 16+2+2 $R_{th(j-p)}$ vs on die dissipating area

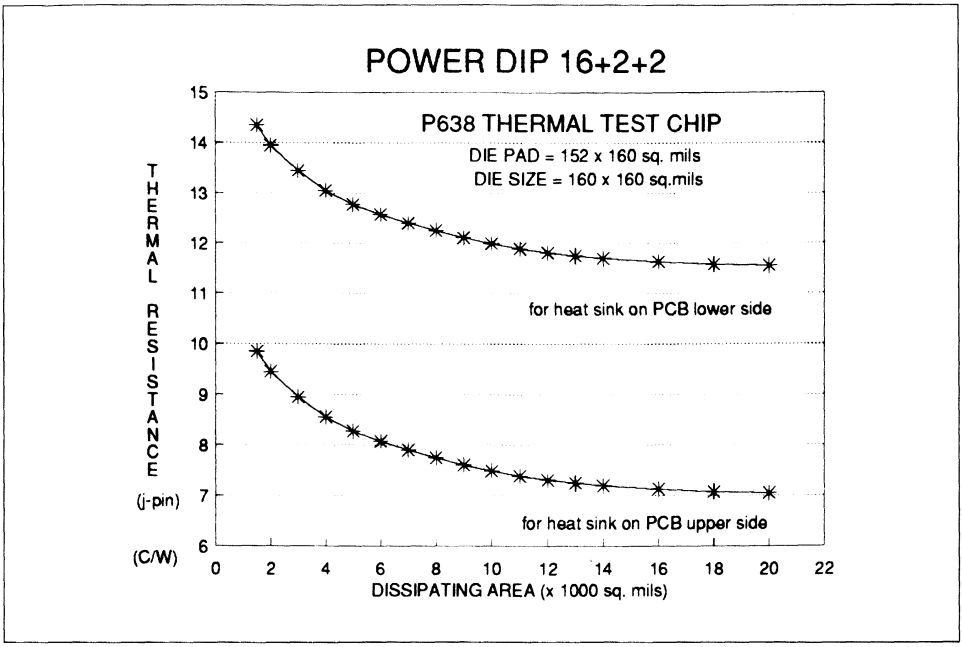
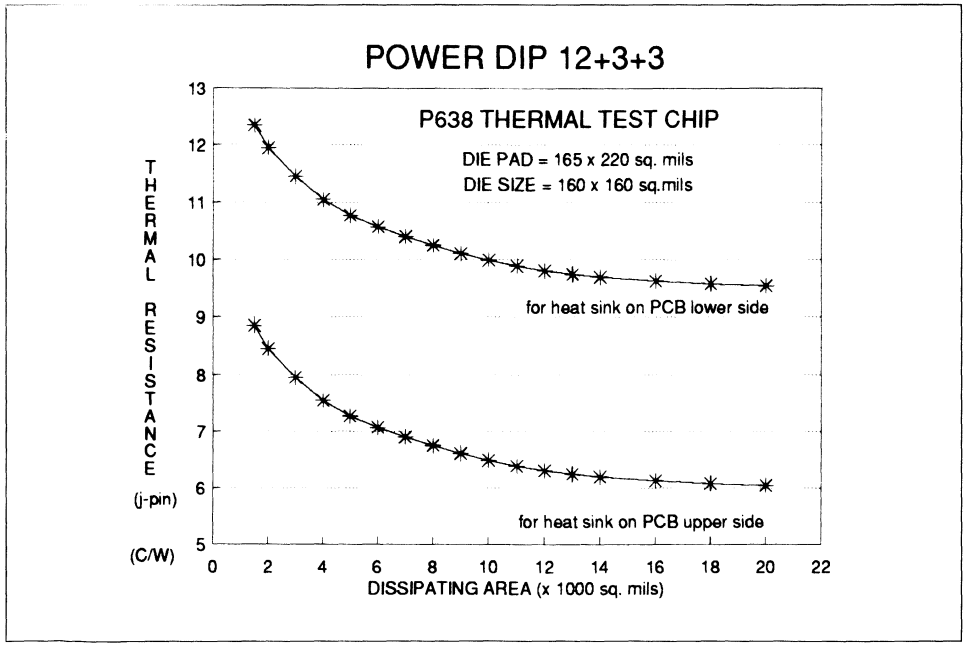


Figure 4 - POWER DIP 12+3+3 $R_{th(j-p)}$ vs on die dissipating area



JUNCTION TO AMBIENT THERMAL RESISTANCE

Fig. 5,6 give the junction to ambient thermal resistance Rth(j-a) of the package vs dissipated power; it evidences the effect of the board in improving the exchange of the heat towards the ambient. The upper curve refers to samples suspended in air, with eight thin wire connecting the dissipating transistors and the sensing diode. The lower curve is obtained with a very large heat sink (35 µm thick 4 x 4cm^2 copper area for each side) while the other curve refers the packages mounted on board with no heat sink.

Rth is decreasing when power is increased, due to a better heat transfer efficiency at higher temperature.

Figure 5 - $R_{th(j-a)}$ of DIP (16+2+2) package vs dissipated power

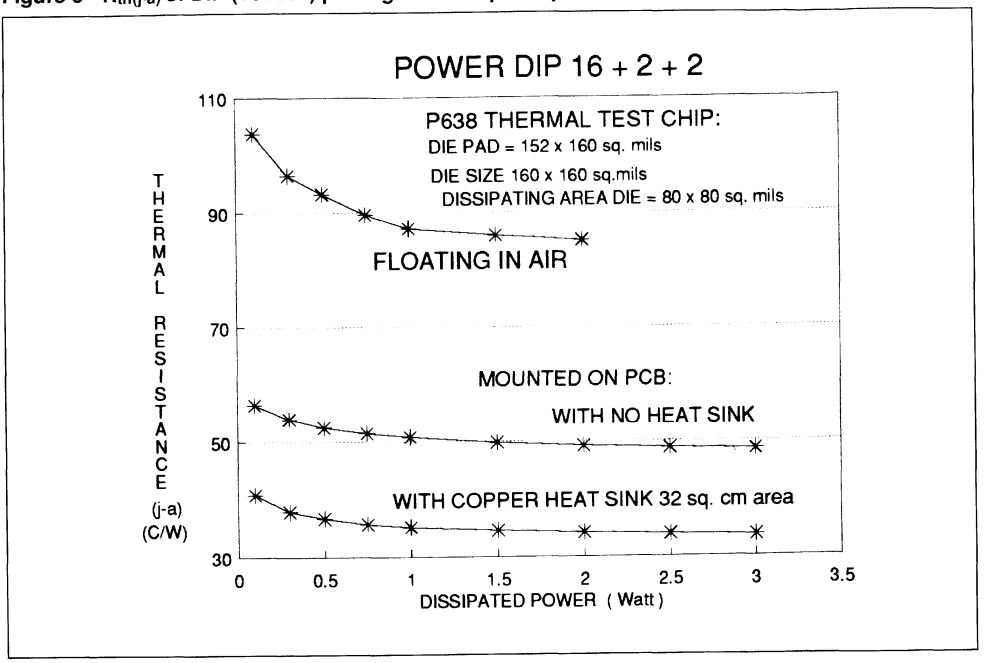
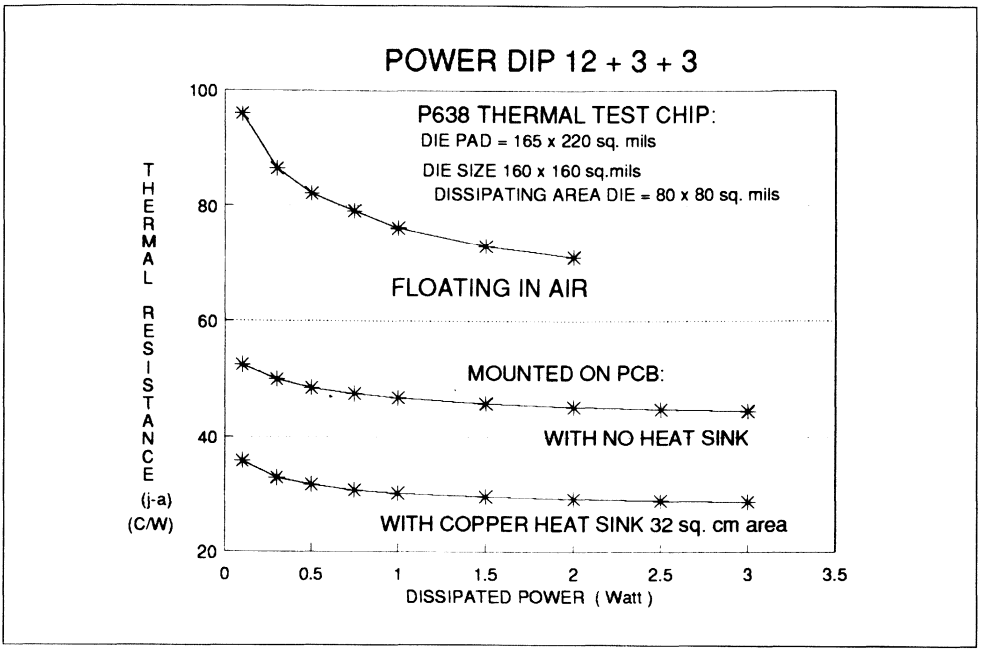


Figure 6 - Rth(j-a) of DIP (12+3+3) package vs. dissipated power



The effect of on board heat sinks with different size is summarized in fig. 8,9; thermal resistance in given vs the side l of the two thick copper squares, obtained in the lower side of the test board and dedicated to heat dissipation (see fig. 7 for test board). Standard thickness of 35µm was used for the characterization as the most part of PCb application but a large improvement can be easily obtained with a thicker copper heat sink on board: 70µm and 105µm (respectively 2 and 3 oz.) are strongly increasing the thermal performances of the considered POWER DIP application. These solutions can be attractive for low complex PC board with a cost saving in avoiding large external heat sink or forced ventilation.

Figure 7 - Test board with two "on board" square heat sinks vs side l

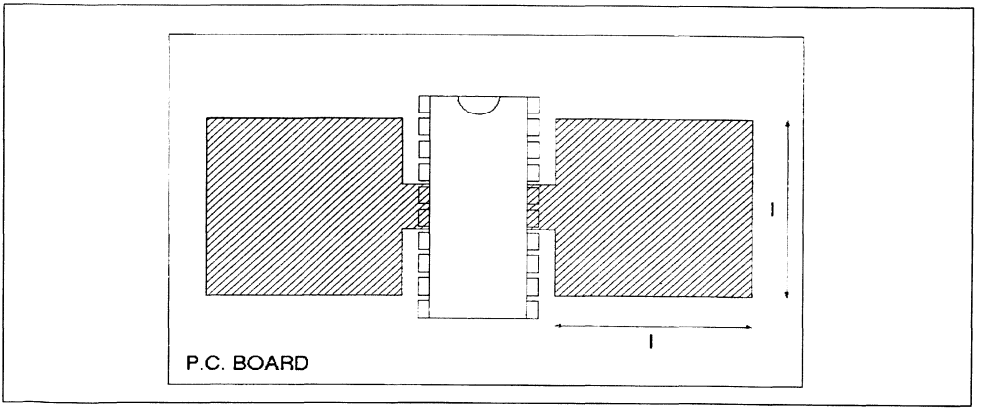


Figure 8 - $R_{th(j-a)}$ of POWER DIP 16+2+2 vs side l for heat sink on the PCB lower side

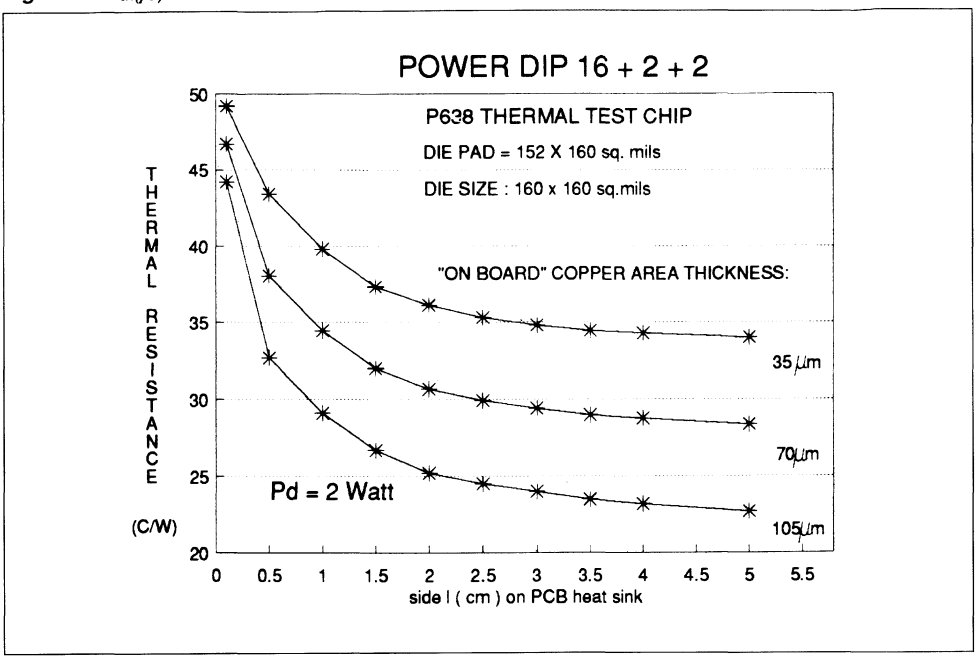
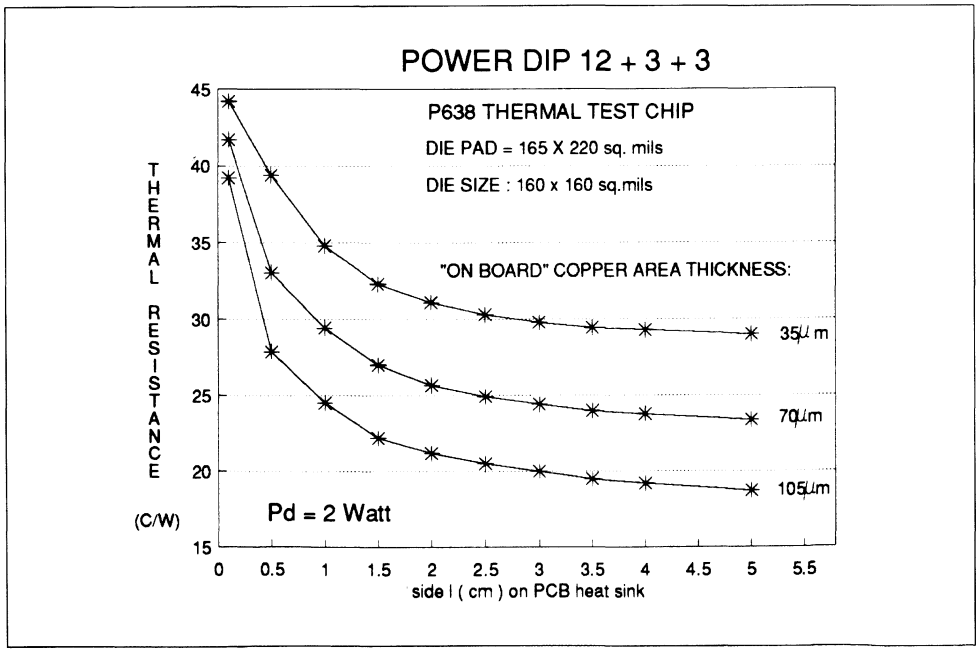


Figure 9 - $R_{th(j-a)}$ of POWER DIP 12+3+3 vs side l for heat sink on the PCB lower side



TRANSIENT THERMAL RESISTANCE

The effect of single pulse of different length and height, is shown in fig. 10,11 for POWER DIP 16+2+2 and 12+3+3. Thicker copper heat sink on PCB is effective also for short pulse width (less 1 sec.). Due to a significant thermal capacitance a correspondingly long risetime, single pulse up to 10W can be delivered to the system for 1s with acceptable junction temperature increase.

Figure 10 - DIP 16+2+2 Transient thermal resistance for single pulses

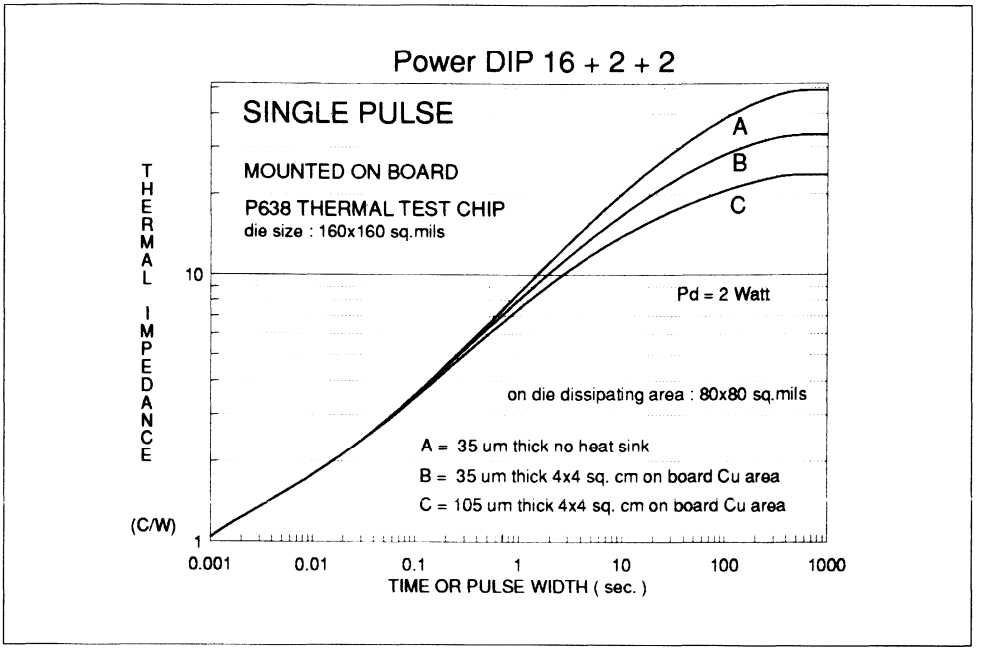
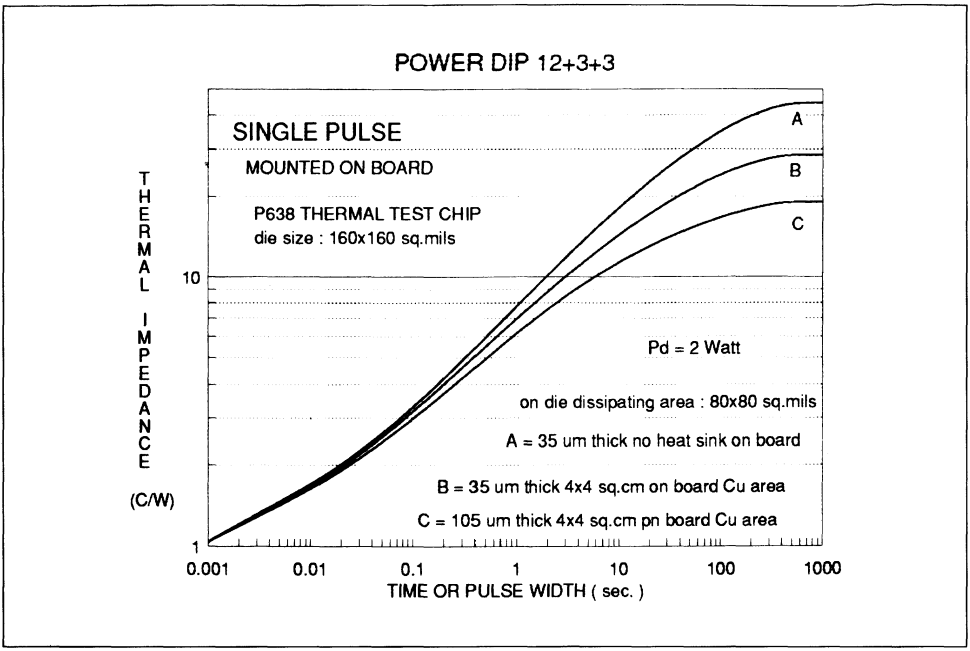


Figure 11 - DIP 12+3+3 Transient thermal resistance for single pulses



Repeatition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to an average temperature increase:

$\Delta T_{avg} = Rth \times Pd_{avg} = Rth \times Pd \times DC$

Junction temperature is oscillating about the mean value as qualitatively shown in fig. 12. The transient thermal resistance corresponding to the upper limit (peak transient thermal resistance) is reported in fig. 13,14 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

Figure 12

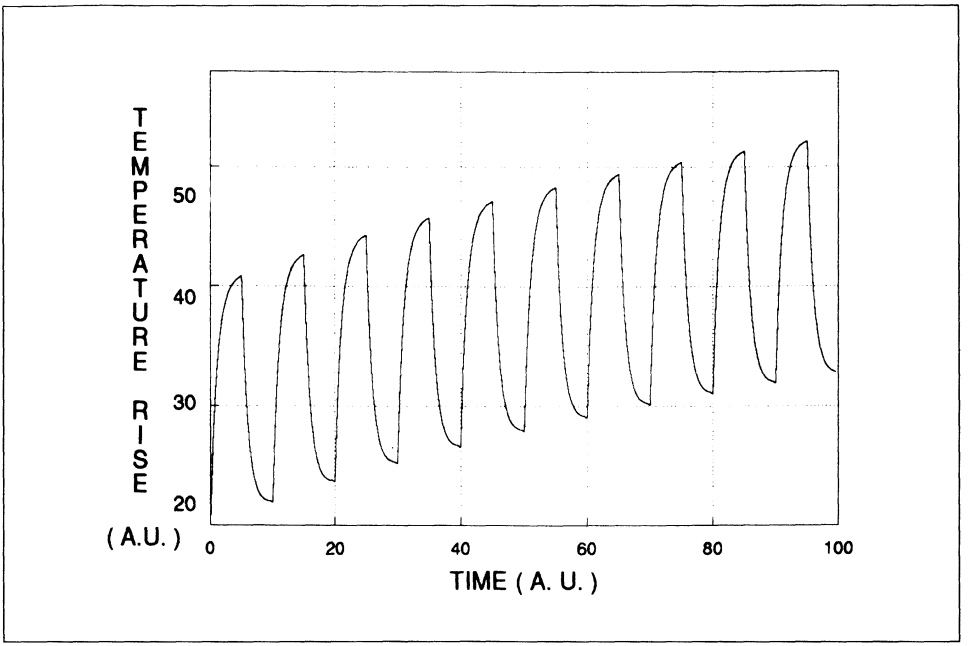


Figure 13 - Peak Transient Thermal resistance of DIP (16+2+2)

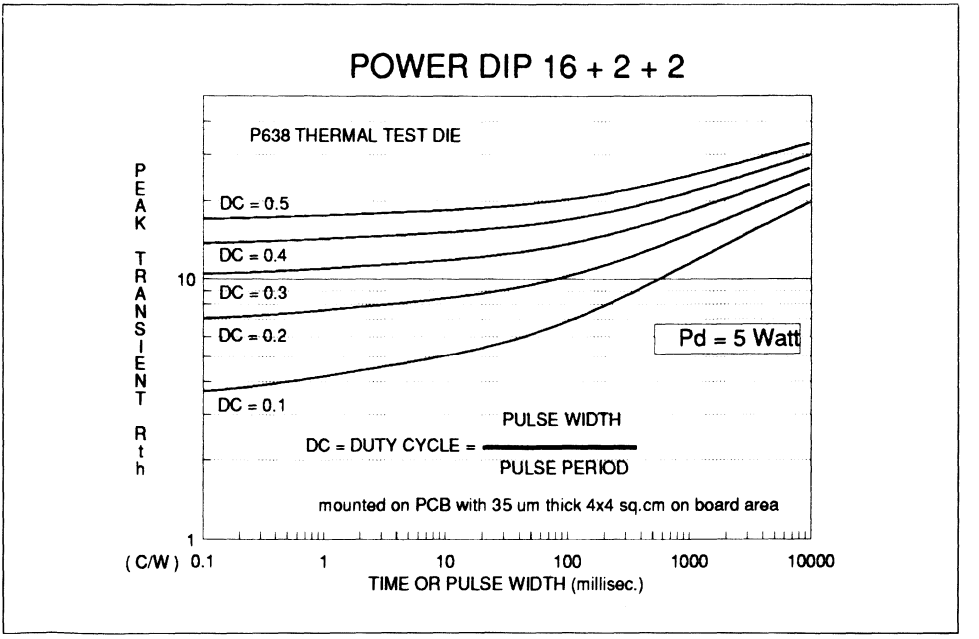
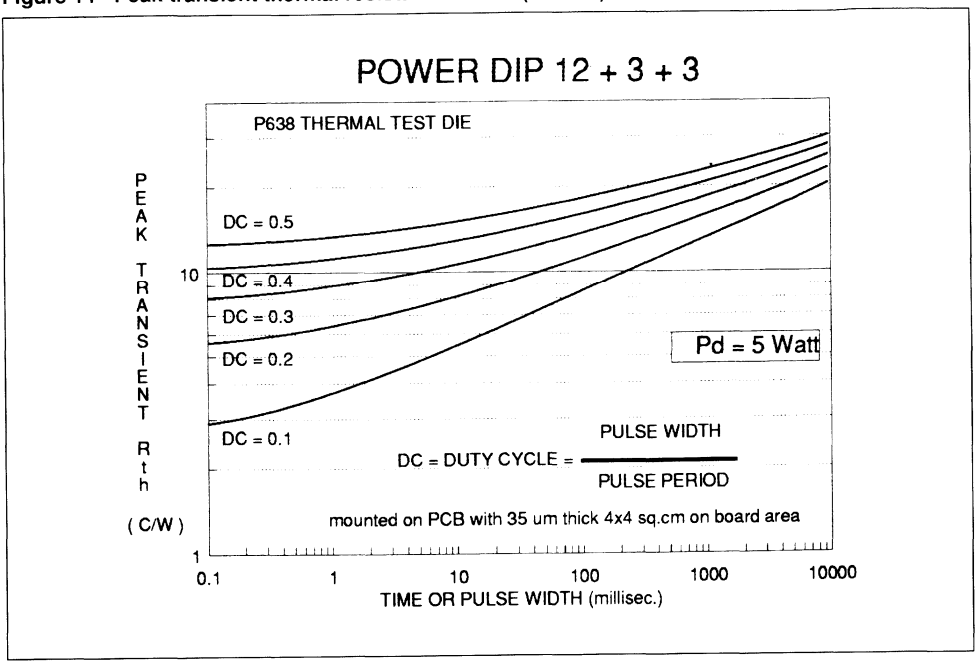


Figure 14 - Peak transient thermal resistance of DIP (12+3+3)



APPENDIX

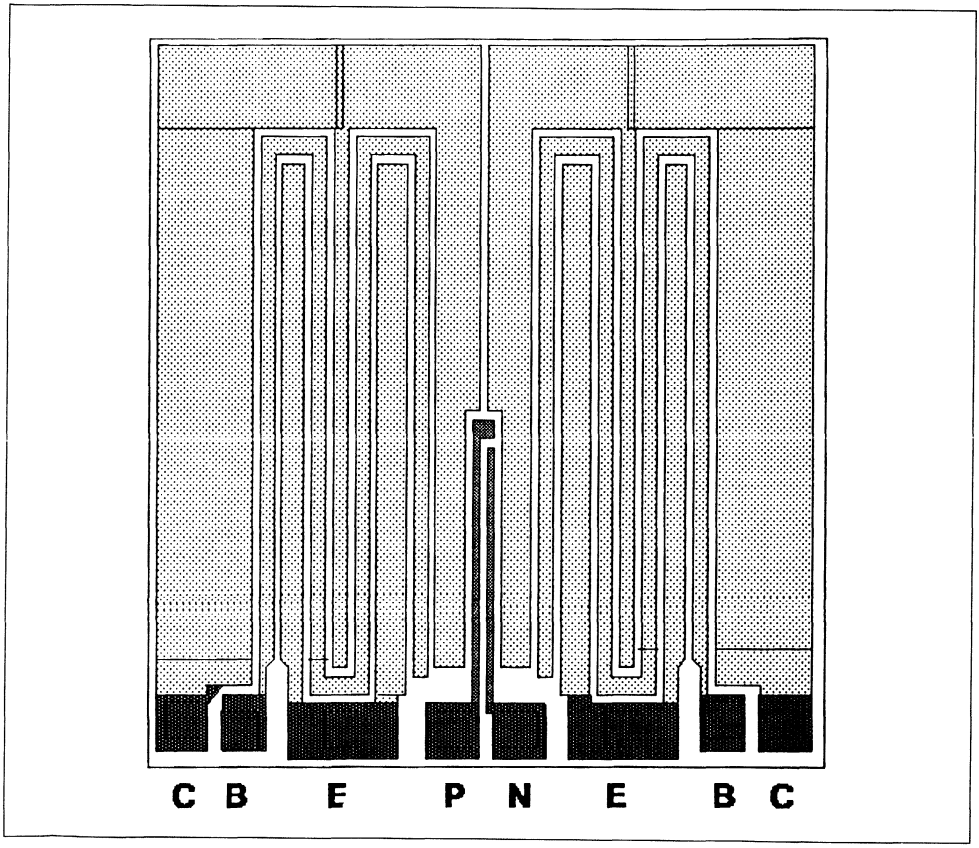
TEST PATTER P638

For thermal measurement

Test patterm P638 is designed for thermal measurement following SEMI guideline G32 (see SEMI Standard Handbook, 1986/87).

It has two bipolar power transistor with area of about 3000 sq. mils and one sensing diode (see Fig. A1). The lay-out is optimized in order to have a uniform temperature, once the two transistors are powered: the sensing diode is placed at the center of this area.

Figure A1 - P638 test pattern



Die size of single unit is 80 x 80 sq. mils; wafer thickness is about 280 microns.

The relationship between the forward voltage V_f of the diode at a constant current of **100** μA and the temperature is linear, with a coefficent **K = 1.85 mV/C** (see Fig. A2).

Therefore changes ΔT_j in junction temperature of the dissipating element formed by the two transistors, can be easily obtained from the diode forward voltage drop:

$$\Delta T_j = \frac{(V_{f1} - V_{f2})}{K}$$

(V_{f2} is the diode forward voltage at ambient temperature and V_{f1} is the voltage when the transistors are dissipating).

For thermal resistance evaluation the measurement circuit is showed in Fig. A3.

Figure A2 - Calibration curve (sensig diode).

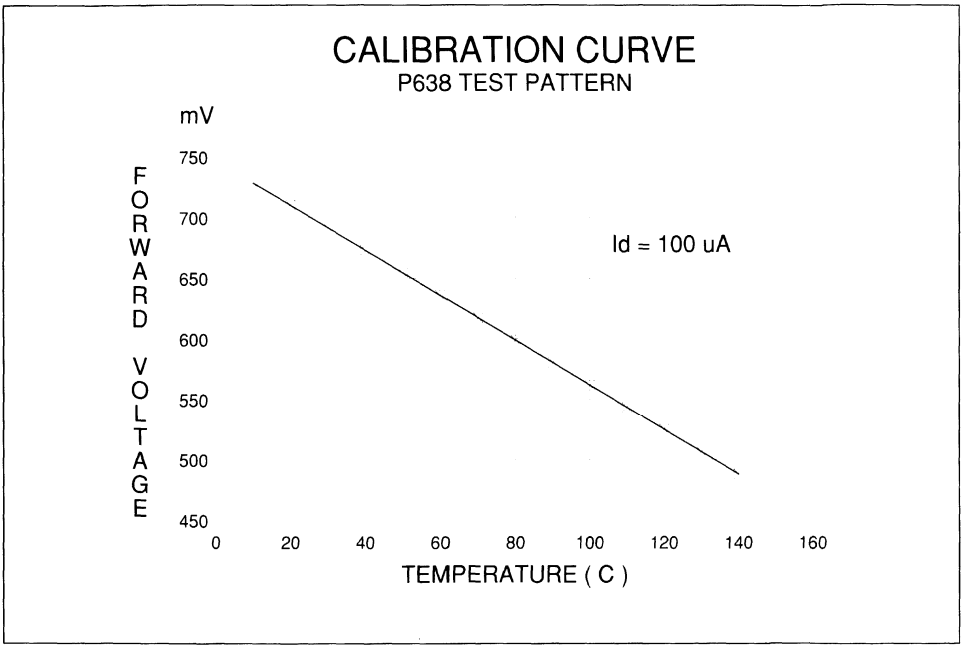
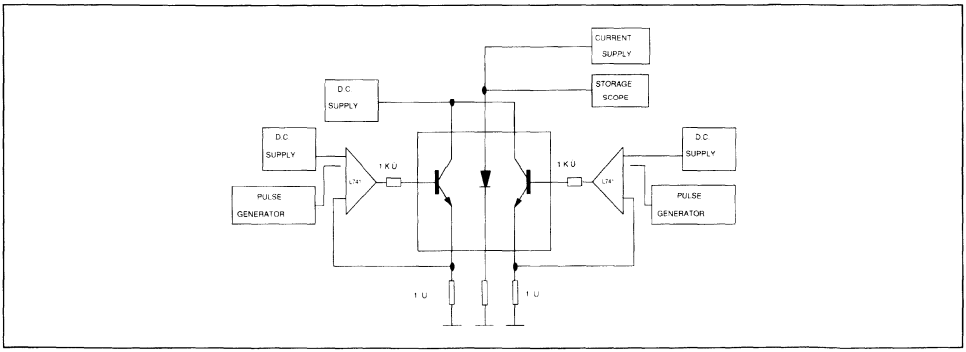


Figure A3 - Measurement System



Tipical conditions are:

P_d (Watt)	V_{ce} (Volt)	I_c (mA)
0.1	1.0	100
0.2	2.0	100
0.3	3.0	100
0.5	5.0	100
0.75	7.5	100
1.0	10.0	100
1.5	15.0	100
2.0	20.0	100
3.0	15.0	200
5.0	25.0	200
10.0	25.0	400

Each transistor is able to dissipate up to 10 Watt due to presence of second breakdown.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

DESIGNING WITH THERMAL IMPEDANCE

BY T.HOPKINS, C.COGNETTI, R.TIZIANI

REPRINT FROM "SEMITHERM PROCEDINGS" S.DIEGO (U.S.A.) 1988.

ABSTRACT

Power switching techniques used in many modern control systems are characterized by single or repetitive power pulses, which can reach several hundred watts each. In these applications where the pulse width is often limited to a few milleseconds, cost effective thermal design considers the effect of thermal capacitance. When this thermal capacitance is large enought, it can limit the junction temperature to within the ratings of the device even in the presence of high dissipation peaks. This paper discusses thermal impedance and the main parameters influencing it. Empirical measurements of the thermal impedance of some standard plastic packages showing the effective thermal impedance under pulsed conditions are also presented.

INTRODUCTION

Power switching applications are becoming very common in many industrial, computer and automotive ICs. In these applications, such as switching power supplies and PWM inductive load drivers, power dissipation is limited to short times, with single or repeated pulses. The normal description of the thermal performance of an IC package, Rth(j -a) (junction to ambient thermal resistance), is of little help in these pulsed applications and leads to a redundant and expensive thermal design.

This paper will discuss the thermal impedance and the main factors influencing it in plastic semiconductor packages. Experimental evaluations of the thermal performance of small signal, medium power, and high power packages wil be presented as case examples. The effects of the thermal capacitance of the packages when dealing with low duty cycle power dissipation will be presented and evaluated in each of the example cases.

THERMAL IMPEDANCE MODEL FOR PLASTIC PACKAGES

The complete thermal impedance of a device can be modeled by combining two elements, the thermal resistance and the thermal capacitance.

The thermal resistance, Rth, quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat dissipation (conduction, convection and radiation), is the ratio between the temperature increase above the reference and the heat flow, DP, and is given by the equation :

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta T}{\frac{\Delta Q}{\Delta t}}$$

Where : ΔQ = heat
Δt = time

Thermal capacitance, C_{th}, is a measure of the capability of accumulating heat, like a capacitor accumulates a charge. For a given structural element, C_{th} depends on the specific heat, c, volume V, and density d, according to the relationship :

$$C_{th} = c\ d\ V$$

The resulting temperature increase when the element has accumulated the heat Q, is given by the equation :

$$\Delta T = \Delta Q / C_{th}$$

The electrical analogy of the thermal behaviour for a given application consisting of an active device, package, printed circuit board, external heat sink and external ambient is a chain of RC cells, each having a characteristic time constant :

$$\tau = RC$$

To show how each cell contributes to the thermal impedance of the finished device consider the simplified example shown in figure 1. The example device consists of a dissipating element (integrated circuit) soldered on a copper frame surrounded by a plastic compound with no external heat sink. Its equivalent electrical circuit is shown in figure 2.

The first cell, shown in figure 2, represents the thermal characteristics of the silicon itself and is characterized by the small volume with a correspondingly low thermal capacitance, in the order of a few mJ/C. The thermal resistance between the junction and

the silicon/slug interface is of about 0.2 to 2 °C/W, depending on die size and on the size of the dissipating elements existing on the silicon. The time constant of this cell is typically in the order of a few milliseconds.

The second cell represents the good conductive path from the silicon/frame interface to the frame periphery. In power packages, where the die is often soldered directly to the external tab of the package, the thermal capacitance can be large. The time constant for this cell is in the order of seconds.

From this point, heat is transferred by conduction to the molded block of the package, with a large thermal resistance and capacitance. The time constant of the third cell is in the order of hundreds of seconds.

After the plastic has heated, convection and radiation to the ambient starts. Since a negligible capacitance is associated with this phase, it is represented by a purely resistive element.

When power is switched on, the junction temperature increase is ruled by the heat accumulation in the cells, each following its own time constant according with the equation :

$\Delta T = R_{th} P_d [1 - e^{(t/\tau)}]$

The steady state junction temperature, T_j, is a function of the $R_{th\ (j\ a)}$ of the system, but the temperature increase is dominated by thermal impedance in the transient phase, as is the case in switching applications.

A simplified example of how the time constants of each cell contribute to the temperature rise is shown in figure 3 where the contribution of the cells of figure 2 is exaggerated for a better understanding.

When working with actual packages, it is observed that the last two sections of the equivalent circuit are not as simple as in this model and possible changes will be discussed later. However, with switching times shorter than few seconds, the model is sufficient for most situations.

Figure 1 : Simplified Package Outline.

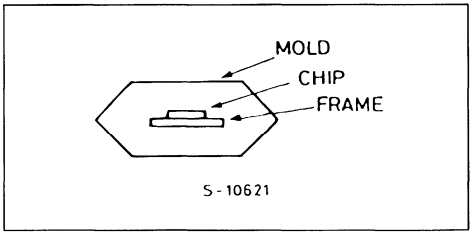


Figure 2 : Equivalent Thermal Circuit of Simplified.

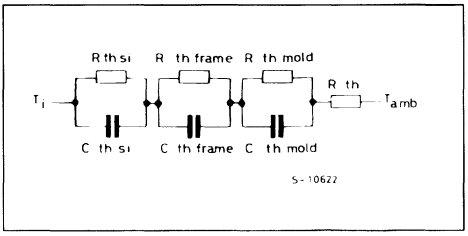
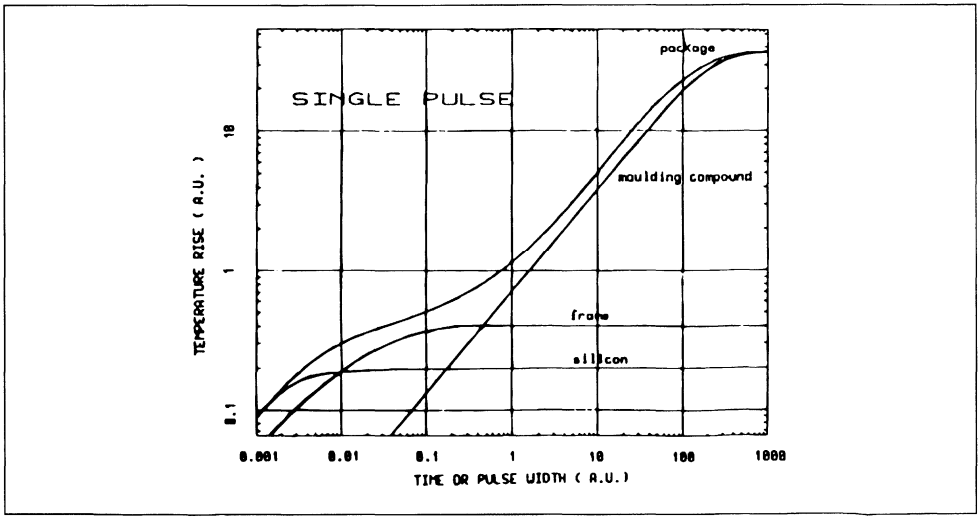


Figure 3 : Time Constant Contribution of Each Thermal Cell (qualitative example).



EXPERIMENTAL MEASUREMENTS

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method. At present, only draft specifications exist, proposed last year and not yet standardized (1).

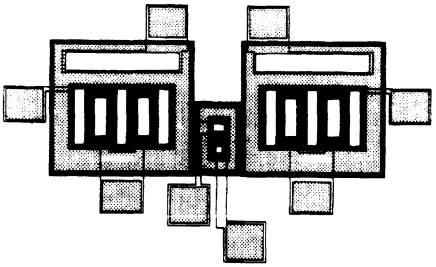
The experimental method used internally for evaluations since 1984 has anticipated these preliminary recomendations to some extent, as it is based on test patterns having, as dissipating element, two power transistors and, as measurement element, a sensing diode placed in the thermal plateau arising when the transistors are biased in parallel.

The method used has been presented elsewhere (2) for the pattern P432 (shown in figure 4), which uses two small (1000 sq mils) bipolar power transistors and has a maximum DC power capability of 40 W (limited by second breakdown of the dissipating elements).

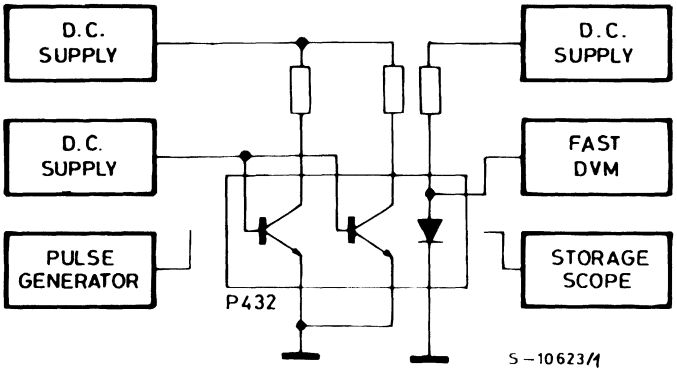
A similar methodology was followed with the new H029 pattern, based on two D-Mos transistors (3) having a total size of 17.000 sq mils and a DC power capability of 300 W on an infinite heat sink at room temperature (limited by thermal resistance and by max operating temperature of the plastics).

Figure 4.

a) P432 Test Die



b) P432 Measurement System

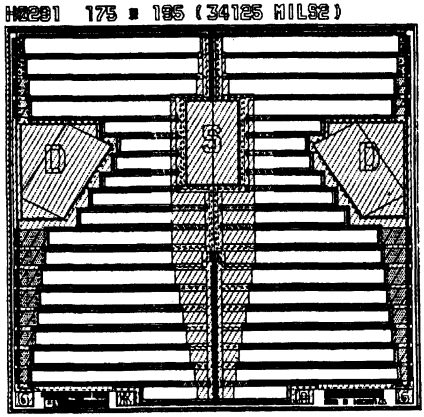


Using the thermal evaluation die, four sets of measurements were performed on an assortment of insertion and surface mount packages produced by SGS-Thomson Microelectronics. The complete characterization is available elsewhere (4). The four measurements taken were :

1) Junction to Case Thermal Resistance (Power Packages)
2) Junction to Ambient Thermal Resistance
3) Transient Thermal Impedance (Single Pulse)
4) Peak Transient Thermal Impedance (Repeated Pulses)

Figure 5.

a) H029 Test Die



b) H029 Measurement System

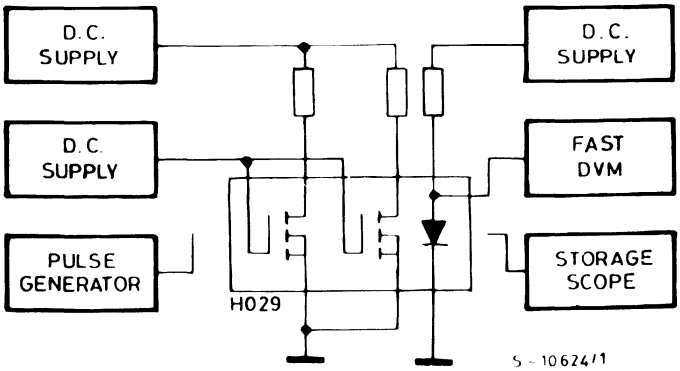
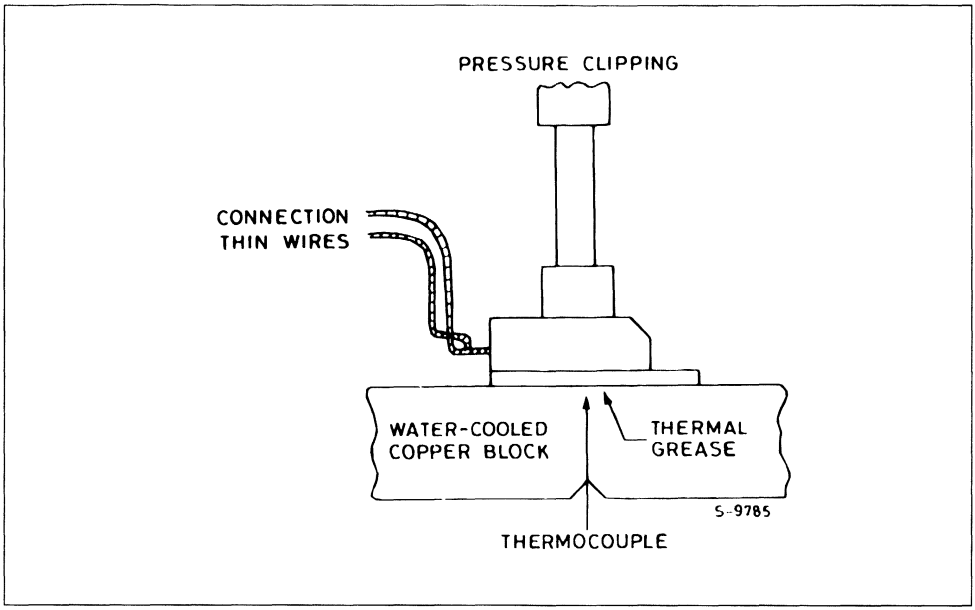


Figure 6 : Set-up for $R_{th\ (j-c)}$ Measurement.

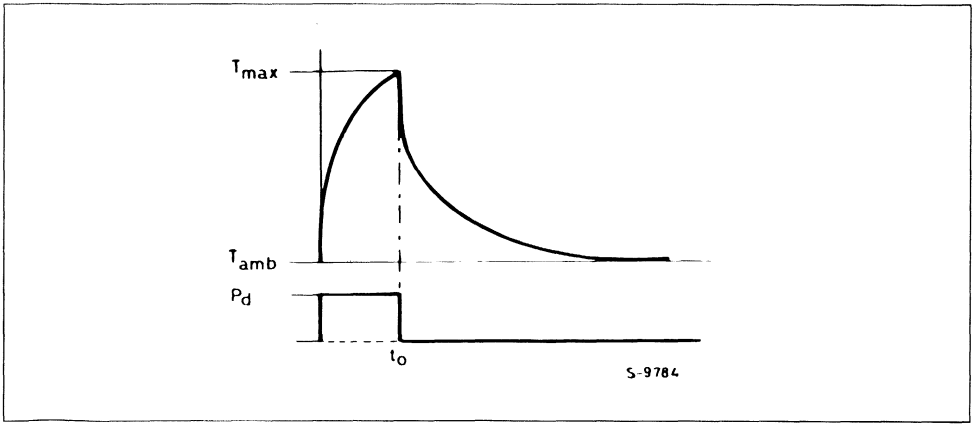


The junction to case thermal resistance measurements were taken using the well known setup shown in figure 6 where the power device is clamped against a large mass of controlled temperature.

The junction to ambient thermal resistance in still air, was measured with the package soldered on standard test boards, described later, and suspensed in 1 cubic foot box, to prevent air movement.

The single pulse transient thermal impedance was measured in still air by applying a single power pulse of duration t_0 to the device. The exponential temperature rise in response to the power pulse is shown qualitetively in figure 7. In the presence of one single power pulse the temperature, ΔT_{max}, reached at time t_0, is lower than the steady state temperature calculated from the junction to ambient thermal resistance. The transient thermal impedance R_o, is obtained from the ratio $\Delta T_{max}/Pd$.

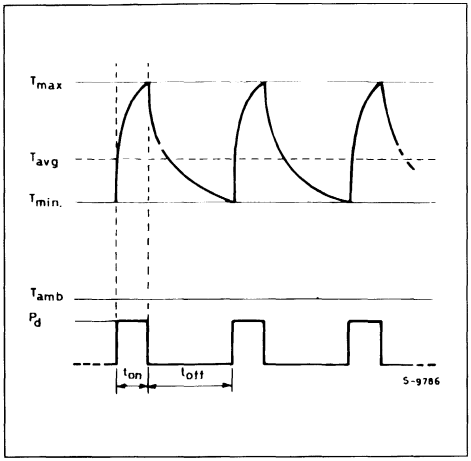
Figure 7 : Transient Thermal Response for a Single Pulse.



The peak transient thermal impedance for a series of repetitive pulses was measured by applying a string of power pulses to the device in free air. When power pulses of the same height, P_d, are repeated with a given duty cycle, DC, and the pulse length, t_p, is shorter than the total time constant of the system, the train of pulses is seen as a contiuous source with mean power level given by the equation :

$$P_{davg} = P_d \, DC$$

Figure 8 : Transient Thermal Response for Repetitive Pulses.



On the other hand, the silicon die has a thermal time constant of 1 to 2 ms and the die temperature is able to follow frequencies of some kHz. The result is that T_j oscillates about the average value :

$$\Delta T_{javg} = R_{th} \, P_{davg}$$

The resulting die temperature excursions are shown qualitatively in figure 8. The peak thermal impedance, R_{thp}, corresponding to the peak temperature, DT_{max}, at the equilibrium can be defined :

$$R_{thp} = \Delta T_{max}/P_d = F\,(t_p, DC)$$

The value of R_{thp} is a function of pulse width and duty cycle. Knowledge of R_{thp} is very important to avoid a peak temperature higher than specified values (usually 150°C).

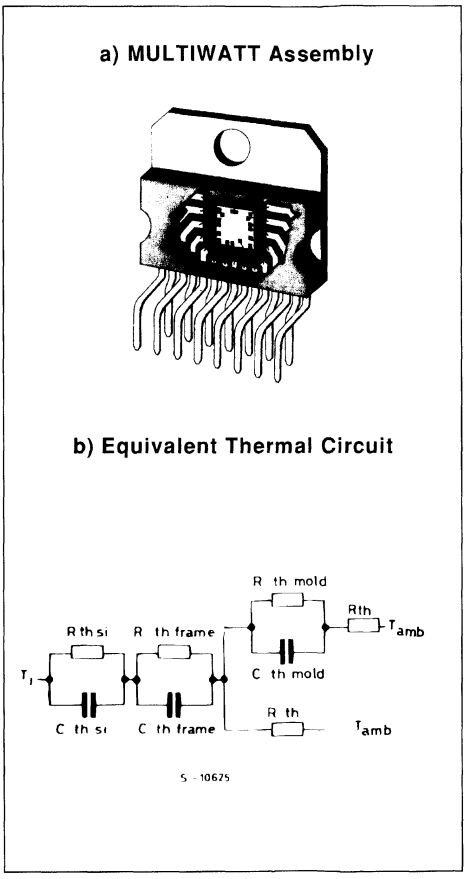
EXPERIMENTAL RESULTS

The experimental measurements taken on several of the packages tested are summarized in the following sections.

MULTIWATT PACKAGE

The MULTIWATT (R) package, shown in figure 9a, is a multileaded power package in which the die is attached directly to the tab of package using a soft solder (Pb/Sn) die attach. The tab of the package is a 1.5 mm thick copper alloy slug. The thermal model of the MULTIWATT, shown in figure 9b, is not much different from that shown in figure 2. The main difference being that when heat reaches the edge of the slug, two parallel paths are possible ; conduction towards the molding compound, and convection and radiation towards the ambient. After a given time, convection and radiation taked place from the plastic.

Figure 9.



Using the two test die, the measured junction to case thermal resistance is :

P432 $R_{th\,(j\,c)} = 2°C/W$

H029 $R_{th\,(j\,c)} = 0.4°C/W$

The measured time constant is approximately 1 ms for each of the two test patterns, but the two devices have a different steady state temperature rise.

The second cell shown in figure 9 is dominated by the large thermal mass of the slug. The thermal resistance of the slug, R_{thslug} is about 1 °C/W and the thermal time constant of the slug is in the order of 1 second.

The third RC cell in the model has a long time constant due to the mass of the plastic molding and its low thermal conductivity. For this cell the steady state is reached after hundreds of seconds.

For the MULTIWATT the DC thermal resistance of the package in free air, $R_{th\ j\ a}$, is 36 °C/W with the P432 die and 34.5 °C/W with the H029 die.

Figure 10 shows the single pulse transient thermal impedance for the MULTIWATT with both the P432 and H029 test die. As can be seen on the graph, the package is capable of high dissipation for short periods of time. For a die like the H029 the power device is capable of 700 to 800 W for pulse widths in the range of 1 to 10 ms. For times up to a few seconds the effective thermal resistance for a single pulse is still in the range of 1 to 3 °C/W.

The peak transient thermal impedance for the MULTIWATT package containing the P432 die in free air is shown in figure 11.

POWER DIP PACKAGE

The power DIP package is a derivative of standard small signal DIP packages with a number of leads connected to the die pad for heat transfer to external heat sinks. With this technique low cost heat sinks can be integrated on the printed circuit board as shown in figure 12a. The thermal model of the power DIP, shown in figure 12b accounts for the external heat sink on the circuit board by adding a second RC cell in parallel with the cell corresponding to the molding compound.

In this model, the second cell has a shorter time constant than for the MULTIWATT package, due in large part to the smaller quantity of copper in the frame (the frame thickness is 0.4 mm compared to 1.5 mm). Thus the capacitance is reduced and the resistance increased.

The increased thermal impedance due to the frame can partially be compensated by a better thermal exchange to the ambient by adding copper to the heat sink on the board. The DC thermal resistance between the junction and ambient can be reduced to the same range as the MULTIWATT package in free air, as shown in figure 13.

Figure 10 : Transient Thermal Response MULTIWATT Package.

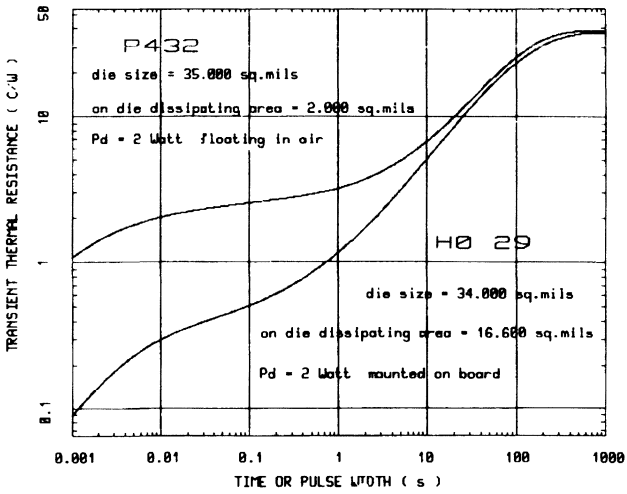


Figure 11 : Peak Thermal Resistance MULTIWATT Package.

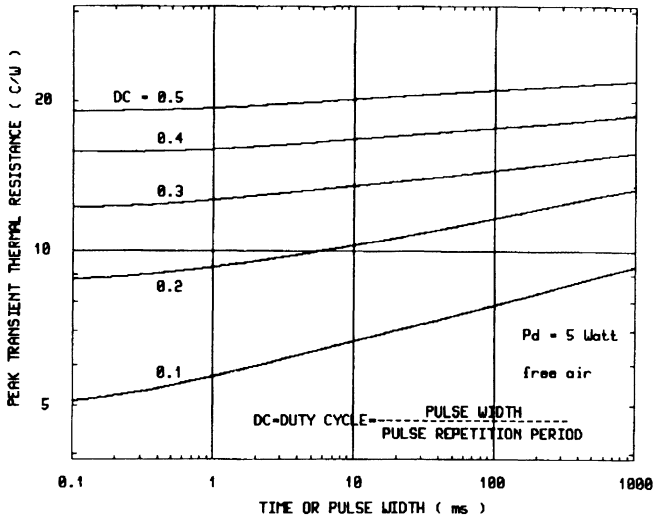
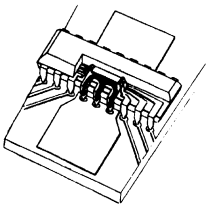
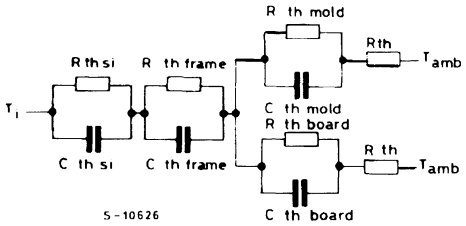


Figure 12.

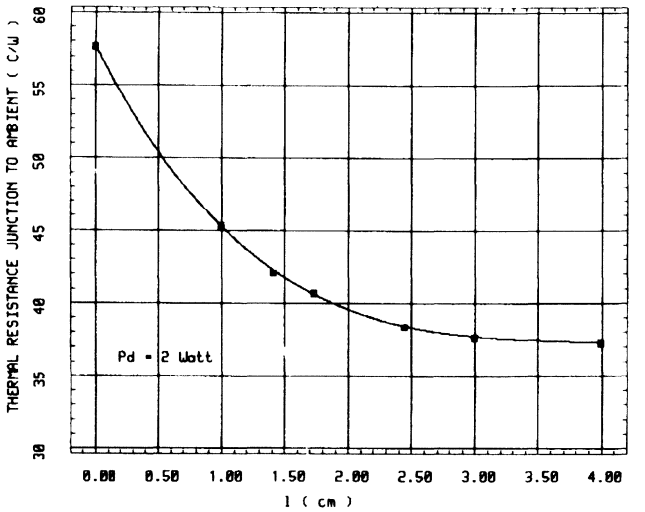


a) Power DIP Package



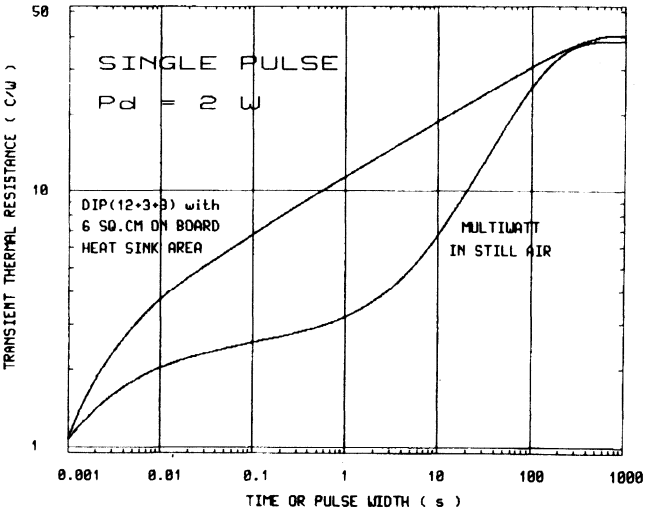
b) Equivalent Thermal Circuit

Figure 13 : Rth (j – a) vs. PCB Heat Sink Size 12 + 3 + 3 Power Dip.



As a comparison, figure 14 compares the thermal performance of the power DIP and the MULTIWATT package. It is clearly seen that even though the DC thermal resistance may be similar, the MULTIWATT is superior in its performance for pulsed applications.

Figure 14 : Transient Thermal Impedance for Single Pulses in Power DIP and MULTIWATT Packages.



STANDARD SIGNAL PACKAGES

In standard, small signal, packages the easiest thermal path is from the die to the ambient through the molding compound. However, if a high conductivity frame, like a copper lead frame, is used another path exists in parallel. Figure 15 shows the equivalent thermal model of such a package. The effectiveness of a copper frame in transferring heat to the board can be seen in the experimental results in DC conditions.

Table 1 shows the thermal resistance of some standard signal packages in two different conditions ; with the device floating in still air connected to the measurement circuit by thin wires and the same device soldered on a test board.

Table 1 : Thermal Resistance of Signal Packages

Package	Frame Thickness & Material	Rth (j-a) Floating	°C/W on Board
DIP 8	(0.4 mm Copper)	125-165	78-90
DIP 14	(0.4 mm Copper)	98-128	64-73
DIP 16	(0.4 mm Copper)	95-124	62-71
DIP 20	(0.4 mm Copper)	85-112	58-69
DIP 14	(0.25 mm Copper)	115-147	84-95
DIP 20	(0.25 mm Copper)	100-134	76-87
DIP 24	(0.25 mm Copper)	67-84	61-68
DIP 20	(0.25 mm Alloy 42)	158-184	133-145
SO 14	(0.25 mm Copper)	218-250	105-180
PLCC 44	(0.25 mm Copper)	66-83	48-72

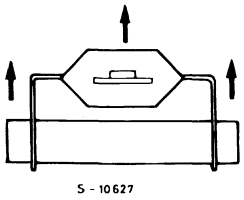
The transient thermal resistance for single pulses for the various packages are shown in figures 16 through 20.

The results of the tests, as shown in the preceding figures, show the true capabilities of the packages. For example, the DIP 20 with a Alloy 42 frame is a typical package used for signal processing applications and can dissipate only 0.5 to 0.7 W in steady state conditions. However, the transient thermal impedance for short pulses is low (11 C/W for t_p = 100 ms) and almost 7 Watts can be dissipated for 100 ms while keeping the junction temperature rise below 80°C.

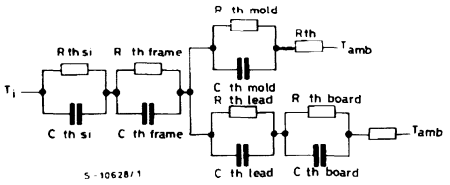
The packages using a 0.4 mm Copper frame have a low steady state thermal resistance, especially in the case of the DIP 20. The thicker lead frame increases the thermal capacitance of the die flag, which greatly improves the transient thermal impedance. In the case of the DIP 20, which has the largest die pad, the transient R_{th} for 100 ms pulses is about 4.3°C/W. This allows the device to dissipate an 18 Watt power pulse while keeping the temperature rise below 80°C.

As with the previous examples the peak transient thermal impedance for repetitive pulses depends on the pulse length and duty cycle as shown in figure 14. With the signal package, however, the effect of the duty cycle becomes much less effective for longer pulses, due primarily to the lower thermal capacitance and hence lower time constant of the frame.

Figure 15.



a) DIP Package Mounted on PCB



b) Equivalent Thermal Circuit DIP Package on PCB

Figure 16 : Transient Thermal Impedance DIP 20 (alloy 42).

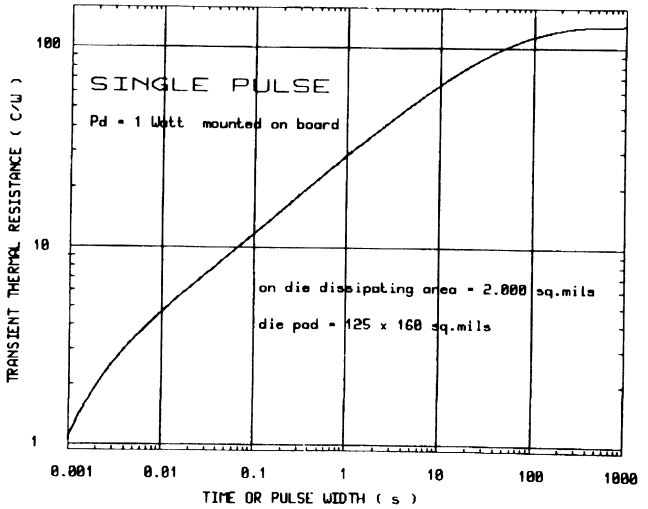


Figure 17 : Transient Thermal Impedance 0.4 mm Copper Frame DIP Packages.

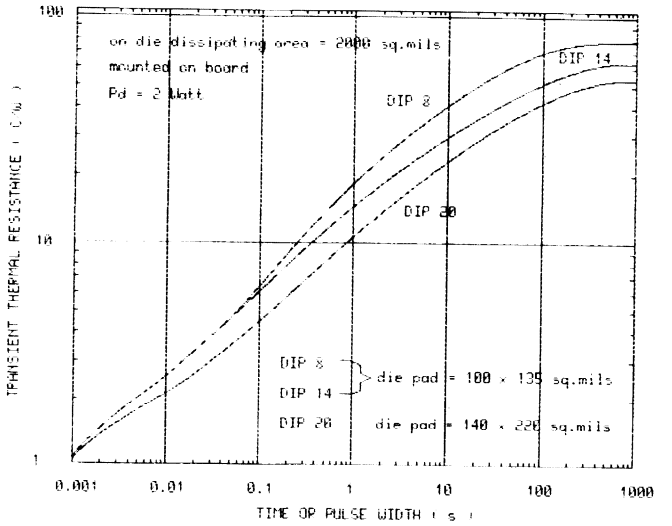


Figure 18 : Transient Thermal Impedance 0.25 mm Copper Frame DIP Packages.

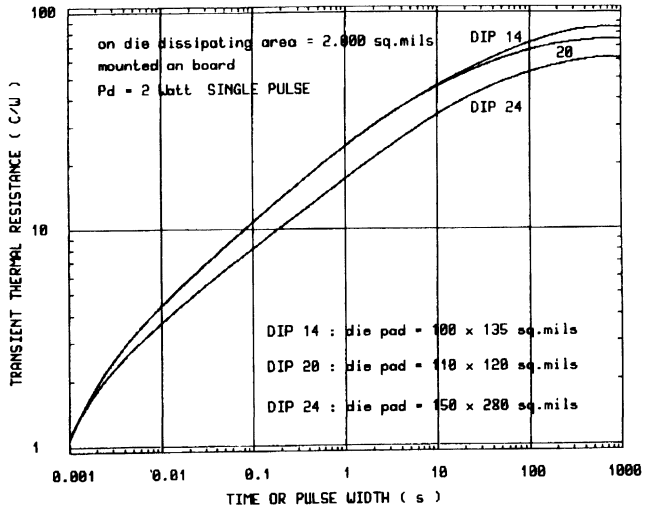


Figure 19 : Transient Thermal Impedance 0.25 mm Frame PLCC Package.

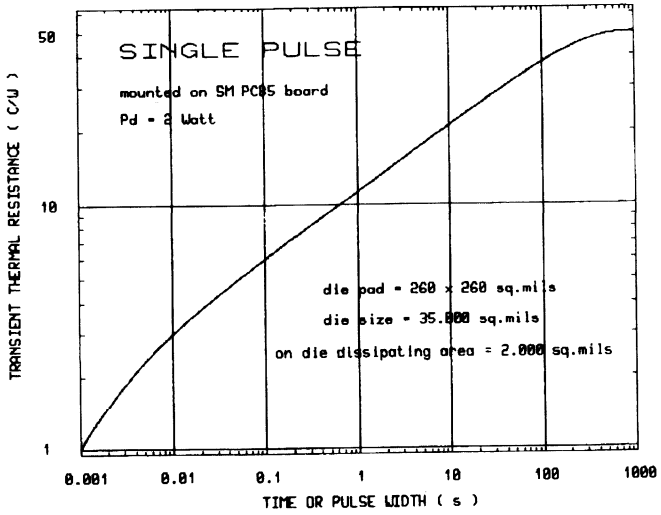


Figure 20 : Transient Thermal Impedance 0.25 mm Copper Frame SO14 Package.

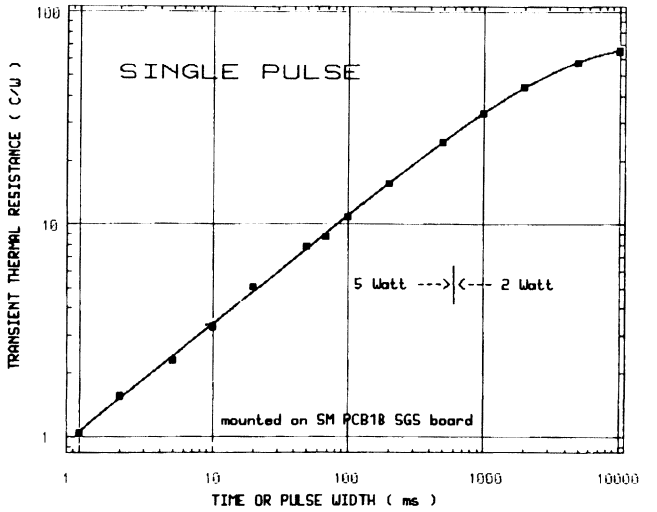
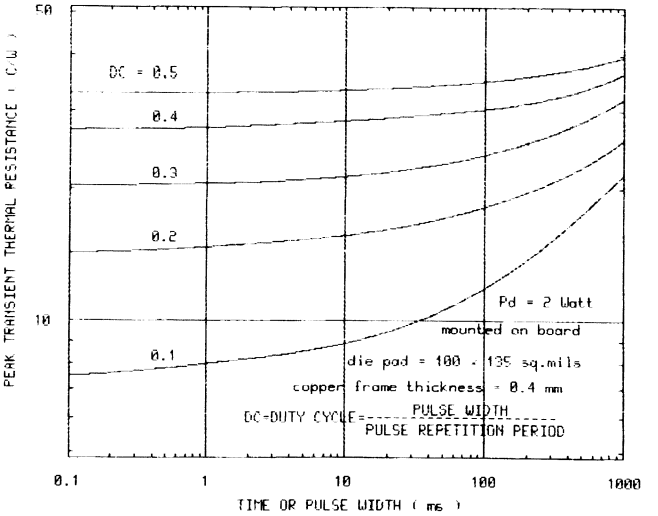


Figure 21 : Peak Thermal Impedance 0.25 mm Copper Frame 14 Lead DIP.



CONCLUSION

This paper has discussed a test procedure for measuring and quantifying the thermal characteristics of semiconductor packages. Using these test methods the thermal impedance of standard integrated circuit packages under pulsed and DC conditions were evaluated. From this evaluation two important considerations arise :

1) The true thermal impedance under repetitive pulsed conditions needs to be considered to maintain the peak junction temperature within the rating for the device. A proper evaluation will result in junction temperatures that do not exceed the specified limits under either steady state or pulsed conditions.

2) The proper evaluation of the transient thermal characteristics of an application should take into account the ability to dissipate high power pulses allowing better thermal design and possibility reducing or eliminating expensive external heat sinks when they are oversized or useless.

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(2) T. Hopkins, R. Tiziani, and C. Cognetti, "Improved thermal impedance measurements by means of a simple integrated structure", presented at SEMITHERM 1986

(3) C. Cini, C. Diazzi, D. Rossi and S. Storti, "High side monolithic switch in Multipower-BCD technology", Proceedings of Microelectronics Conference, Munchen November 1986

(4) Application Notes 106 through 110, SGS-THOMSON Microelectronics, 1987

THERMAL MANAGEMENT IN SURFACE MOUNTING

The evolutionary trends of integrated circuits and printed circuits boards are, in both cases, towards improved performance and reduced size. From these points of view, a factor of major importance has been mutual thermal interaction between ICs, even those with low dissipation.

It follows then that thermal design of medium and high density applications has evolved to include factors such as power effects, die size, package thermal resistance, **integration level of active devices** and substrate type. Added to this a trend towards greater use of switching techniques exists.

Today, in order to design reliable application circuits, it is necessary to have complete data on package thermal response characteristics. In fact, it is a well known and long established fact that device lifetime has an exponential relationship with junction temperature.

PRELIMINARY CONSIDERATIONS

Heat dissipation for DIPs with a low thermal conductivity frame (e.g. Alloy42) is due to convection and **irradiation** from an emiting area corresponding to the silicon die and the package die pad.

Since heat transmission through the lead frame is very poor, dissipation does not depend greatly on substrate type. In fact, samples soldered on printed circuit boards, or inserted in **connectors** have nearly the same dissipation capability as samples suspended in air. The difference, in the range of just 10%, is commonly ignored and specifications for insertion ICs only give one thermal resistance value, which is more than adequate for good thermal design.

The question then arises, is the approximation valid for SO and PLCC packages ?

The answer is no ! Thermal characteristics for these devices are influenced by many factors.

1) Device Related Factors
   - size of the dissipating element
   - dissipation level
   - pulse length and duty cycle

2) Package Related Factors
   - thermal conductivity of the frame
   - frame design

3) Substrate Related Factors
   - thermal conductivity of the substrate
   - layout

Therefore a number of parameters can change the thermal characteristics. These cannot be described by a single thermal resistance, in fact a set of experimental curves gives the best presentation.

JUNCTION TO AMBIENT THERMAL RESISTANCE $R_{th(j-a)}$

$R_{th(j-a)}$ represents the thermal resistance of the system and comprises the silicon die, the package, and any thermal mass in contact with the package to dissipate heat to the ambient.

At a given dissipation level P_d, the increase in junction temperature ΔT_j over ambient temperature T_a is given by :

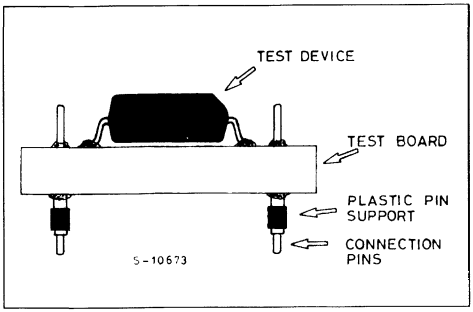
$\Delta T_j = R_{th(j-a)} \times P_d$

$R_{th(j-a)}$ is made up of many elements both within the device and external to it.

If the device is considered alone, $R_{th(j-a)}$ is given by the dissipation path from the silicon die to the leadframe, to the molding compound, to the ambient. **Experimental values are very large in this condition, especially for small packages such as Small Outline types.**

However, this situation is not met in practice and experimental data included in the present work indicates the worst case (floating samples). In most applications, Surface Mount Devices are soldered onto a substrate (commonly epoxy glass (FR4) and are in thermal contact with it through the soldered joints and the copper interconnections. In this case, the heat generated by the active circuit is transferred to the leadframe and then to the substrate. A new dissipation path thus exists in parallel with the previous one whose efficiency depends on the thermal conductivity of the frame and on the length of the printed circuit's copper tracks. Figure A shows the experimental module.

Figure A : Device Soldered to the Best Board, for Junction to Ambient Thermal Resistance Measurement.

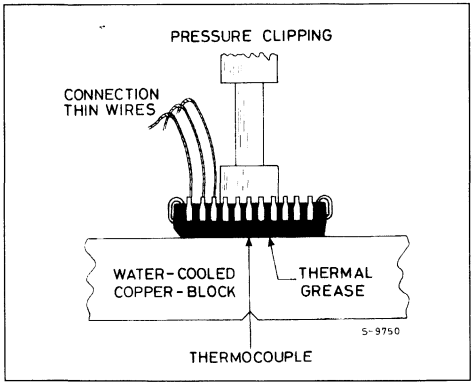


JUNCTION TO CASE THERMAL RESISTANCE $R_{th(j-c)}$

$R_{th(j-c)}$ is the thermal resistance from the junction to a given area of the peackage's external surface where a heatsink is applied.

In signal packages, a suitable area is its upper surface. **Measurements are made with the samples in good thermal contact with an infinite heatsink (fig. B).**

Figure B : Junction to Case Thermal Resistance Measurement.



When a heatsink of thermal resistance R_{hs} is attached to the package, the following relationship is valid :

$$R_{th(j-a)} = R_{th(j-c)} + \frac{R_{hs} \times R^{*}}{R_{hs} + R^{*}}$$

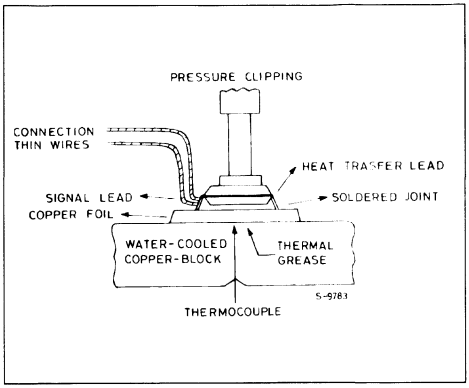
Where R^{*} takes into account all the other dissipation paths (i.e. junction/frame/substrate). R^{*} is the lowest with low thermal conductivity frames.

In high power applications R^{*} " R_{hs} and $R_{th(j-a)} = R_{th(j-c)} + R_{hs}$

JUNCTION TO PIN THERMAL RESISTANCE $R_{th(j-p)}$

In medium power packages $R_{th(j-p)}$ is the thermal resistance of the heat transfer leads, from the junction to the external heatsink. In most cases the external heatsink is integrated on the board. Figure C shows the experimental setup.

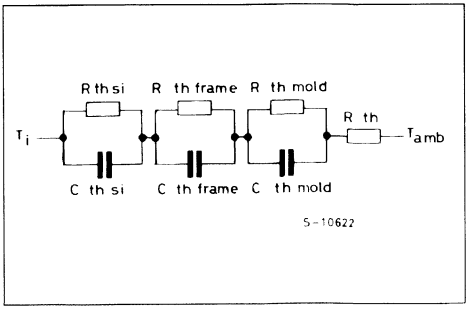
Figure C : Junction to Pin Thermal Resistance Measurement.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

The electrical equivalent of heat dissipation for a module formed by an active device, its package, a PCB and the ambient, is a chain of RC cells, as shown in fig. D, each with a characteristic rise time (τ) = RC.

Figure D : Equivalent Thermal Circuit Simplified Package.

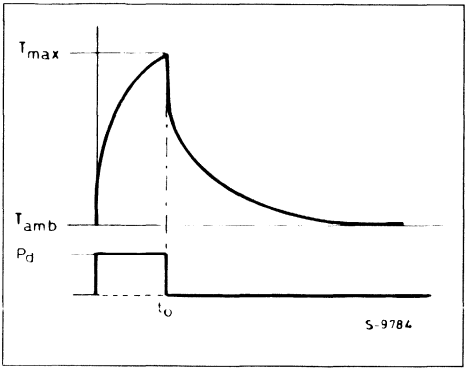


The thermal capacitance of each cell is a measure of its ability to accumulate heat and depends on the specific heat, volume and density of the constituent materials.

When power is switched on, the junction temperature after time it is governed by the heat impedance of the cells, each of which follows its own time constant - this is analogous to the exponential charge of RC cells in an electrical circuit.

For a pulse lenght t_o, the effective T_j can be significantly lower than the steady state T_j (fig. E) and the transient thermal resistance $R_{th(to)}$ can be defined from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Figure E : Temperature Rise for Single Power Pulse.



Obviously, this parameter is smaller for shorter pulses and higher power can be dissipated without exceeding the maximum junction temperature defined from a reliability point of view.

The knowledge of transient thermal data is an important tool for cost effective thermal design of switching applications.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

When pulses of the same height Pd are repeated with a duty cycle, DC, and a pulse width t_o, which is shorter than the overall system time constant, the train of pulses is seen as a continuous source of mean power Pd_{avg}, where :

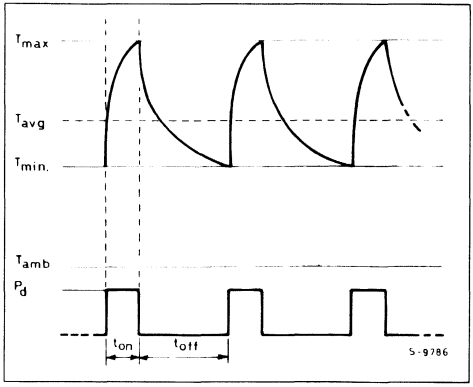
$Pd_{avg} = Pd \times DC$

However the silicon die has a time constant in the order of 1 to 2ms and is able to follow frequencies in the kHz range. Thus junction temperature oscillates about an average value given by :

$T_{javg} = R_{th} \times Pd_{avg}$

as is graphically shown in fig. F.

Figure F : Temperature Rise for Repeated Power Pulses.



The thermal resistance corresponding to the peak of the steady state oscillations (peak thermal resistance indicates the maximum temperature reached by the junction and, depending on duty cycle and pulse width, may be much lower than the DC thermal resistance.

EXPERIMENTAL METHOD

Measurements were performed by means of the especially developed thermal test pattern P432, which is designed according to the Semiconductor Equipment and Materials Institute (SEMI) G32 guideline.

Test chip P432 is based on a dissipating element formed by two npn transistors, each with 10W power capability, and one sensing diode (fig. G). The diode is placed on the temperature plateau generated when the two transistors are biased in parallel, and gives the actual junction temperature T_j of the dissipating element, through the calibration curve (fig. H) of its forward voltage Vf versus temperature at a constant current of 100µA.

Figure G : Thermal Test Pattern P432.

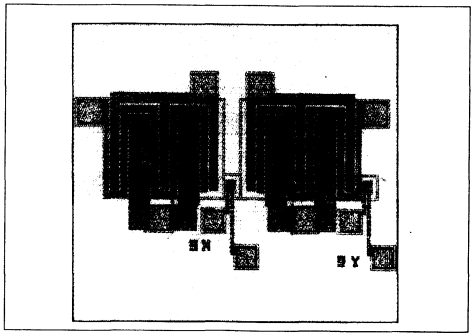
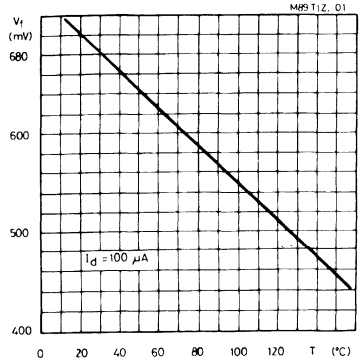


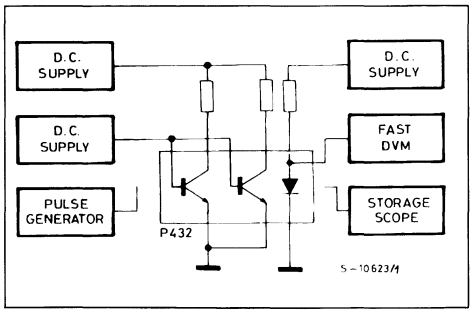
Figure H : Calibration Curve of P432 Temperature Sensing Diode.



Transistor size is intentionally limited to 1000sq. mils, in order to simulate high power density, characterizing a worst case. Die size, which is found to have little influence on thermal resistance when a copper frame is used, is slightly smaller than the die pad size and never exceeds 30k sq mils even in the largest packages such as high pin count PLCCs.

The measurement setup is shown in fig. I. it is compatible with DC and AC supplies and has an accuracy of better than 5%.

Figure I : Experimental Setup.



The advantages offered by the test pattern are :

- high power capability
- repeatable V_f and temperature coefficient (1.9mv/C) of the sensing element
- high resolution in pulsed conditions (100µs)
- better correlation from one package to another.

Both Alloy 42 and copper frames were considered for narrow SO packages (150mils body). For wide SO (300mils body) and PLCC packages only copper frames were examined. Suitable test boards were developed (figs J, K and L).

Figure J : Test Board Lay-out for SO Packages (150 mils body width)
Board size is : 23 x 42mm^2.

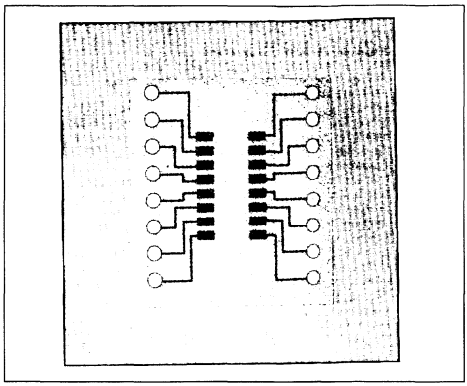


Figure K : Test Board Lay-out for SO Packages (3000 mils body width)
Board size is 38 x 43mm^2.

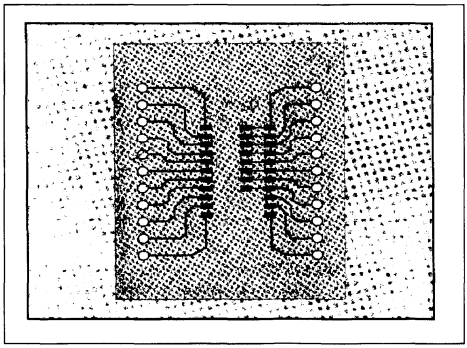
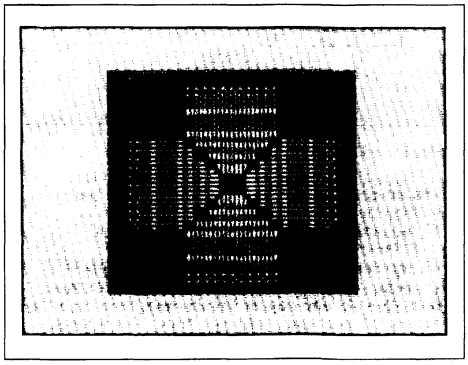


Figure K : Test Board for PLCCs
Board size is 58 x 58mm^2.



MEDIUM POWER PACKAGES

While surface mount signal ICs are readily available, almost all power ICs are still assembled in traditional insertion packages.

Medium power SM packages (Pd < 2W) can readily be derived from existing small outline and chip carrier packages by modifying the leadframe - in much the same way that Powerdip packages were derived from standard Dips.

This approach is particularly attractive because the external dimensions of the package are identical to existing low power packages, allowing the use of standard automatic assembly and test equipment. Frame modification is aimed at obtaining a low junction to pin thermal resistance path for the transfer of heat to a suitable external heatsink. A number of leads are connected to the die pad for this purpose. Two possibilities are considered here : a medium power PLCC44 with 11 heat transfer leads (fig. M) and a medium power SO20 with 8 heat transfer leads (fig. N).

A cost effective heat spreader can be obtained on the board by means of suitably dimensioned copper areas. The heat transfer leads are soldered to there areas (fig. M1, N1).

Figure M : Lead Frame for Medium Power PLCC44.

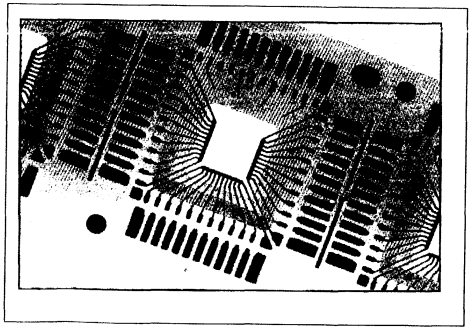


Figure N : Lead Frame for Medium Power SO20.

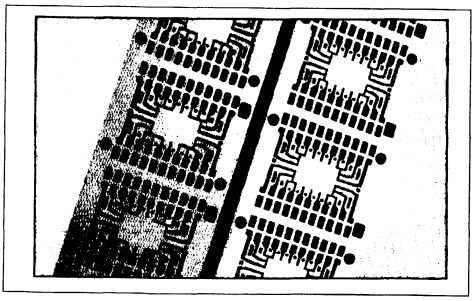


Figure M1 : Test Board for Medium Power PLCC44.

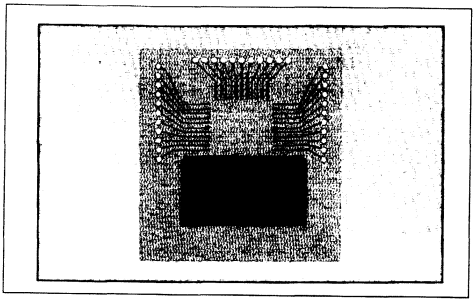
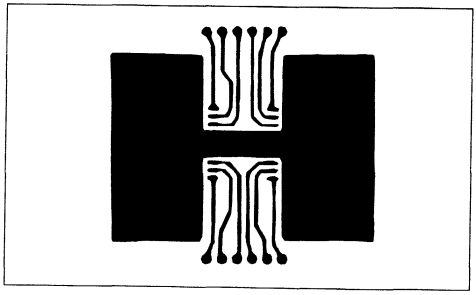


Figure N1 : Test Board for Medium Power SO20.



THERMAL DATA OF SIGNAL PACKAGES

SUMMARY OF JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION (SGS-THOMSON test board)

	Die Size (millinches)	**Power PD [W]**	$R_{th(j-a)}$ [°C/W] on Board
SO8 Alloy 42 Copper	90 x 100 94 x 125	0.2 0.2	250-310 130-180
SO14 Alloy 42 Copper Copper	98 x 100 78 x 118 98 x 125	0.3 0.5 0.7	200-240 120-160 105-145
SO16 Alloy 42 Copper	98 x 118 94 x 185	0.3 0.5	180-215 95-135
SO16W Copper	120 x 160	0.7	90-112
SO20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41
$R_{th(j-a)}$ values correspond to low and high board density			

SUMMARY OF JUNCTION TO CASE THERMAL RESISTANCE

	Die Pad Size (millinches)	$R_{th(j-a)}$ [°C/W]
PLCC20	140 x 140	25
PLCC44	260 x 260	13
PLCC68	425 x 425	10
PLCC84	450 x 450	9

JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION

Figure 1 : SO8.

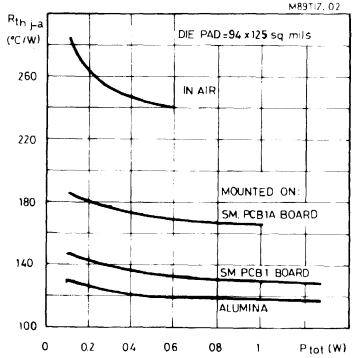


Figure 2 : SO14.

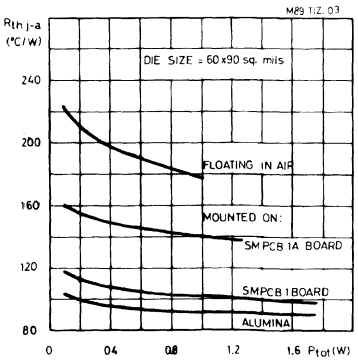


Figure 3 : SO16.

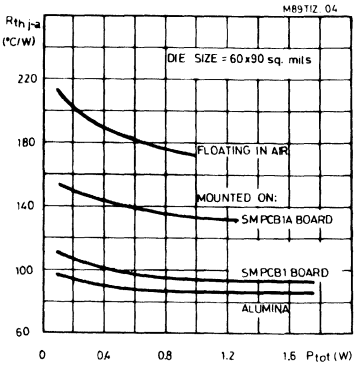


Figure 4 : SO20.

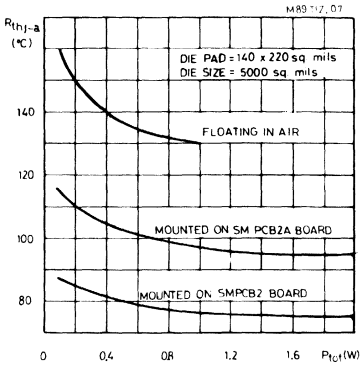


Figure 5 : PLCC20.

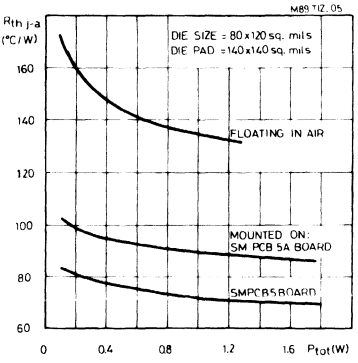


Figure 6 : PLCC44.

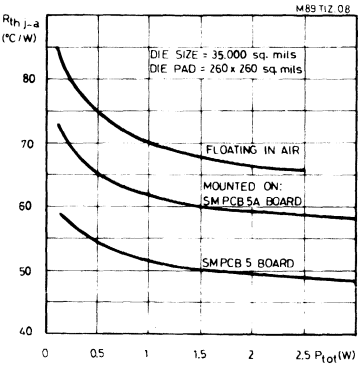


Figure 7 : PLCC68.

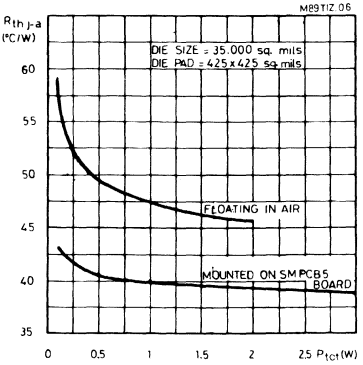
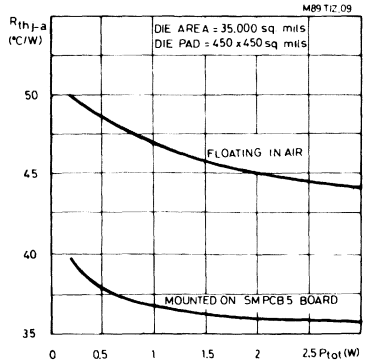


Figure 8 : PLCC84.



JUNCTION TO AMBIENT THERMAL RESISTANCE VS BOARD LAY-OUT

(area of copper tracks on the board)

Figure 9 : SO16.

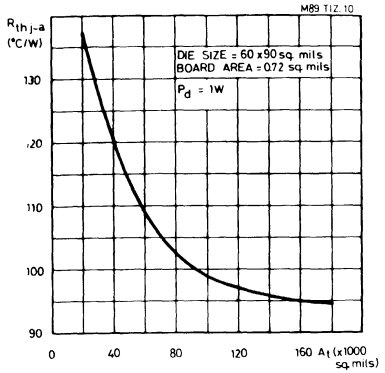


Figure 10 : SO20.

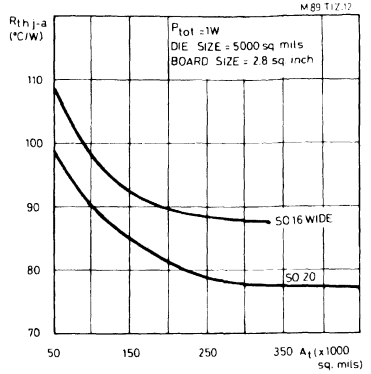


Figure 11 : PLCC44.

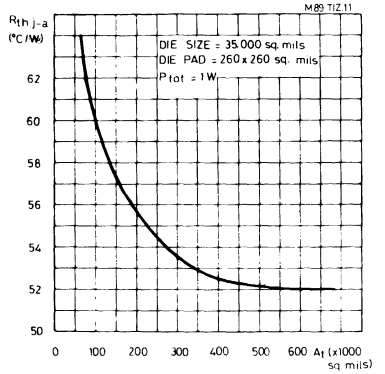
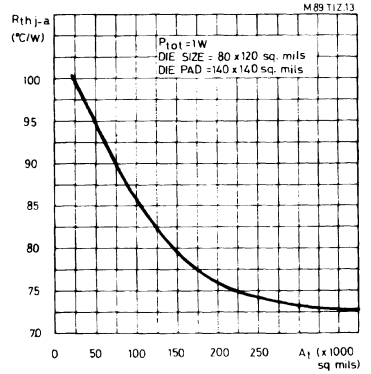


Figure 12 : PLCC20.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 13 : SO8.

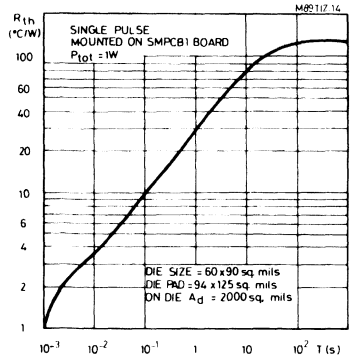


Figure 14 : SO14, 16.

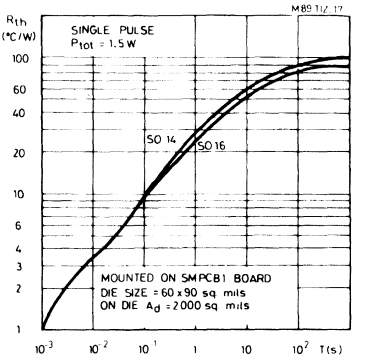


Figure 15 : SO20.

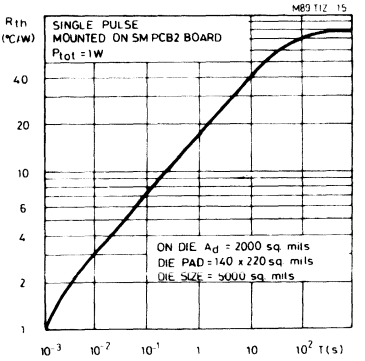


Figure 16 : PLCC44.

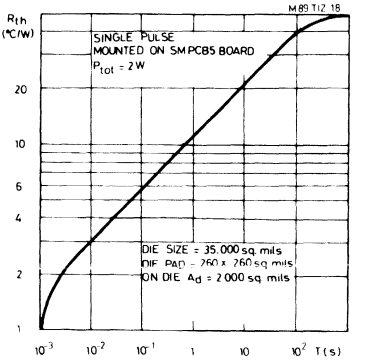


Figure 17 : PLCC68.

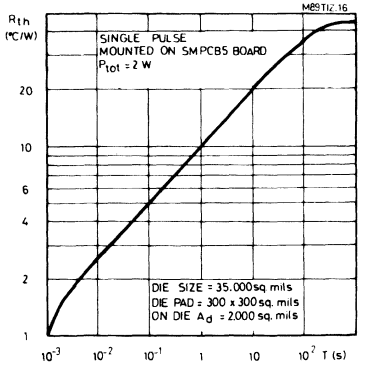
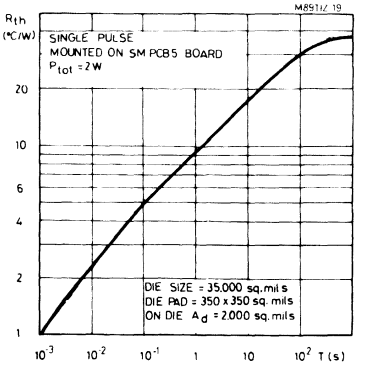


Figure 18 : PLCC84.



PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

Figure 19 : SO14.

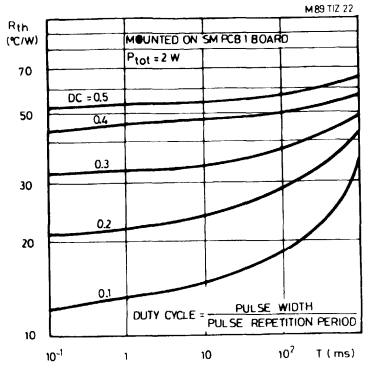


Figure 20 : SO20.

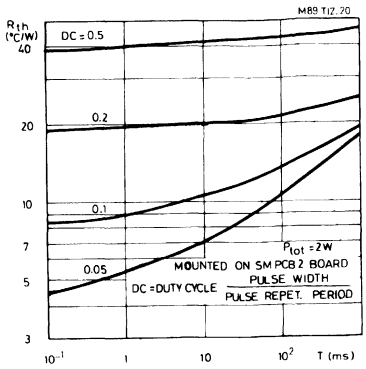


Figure 21 : PLCC44.

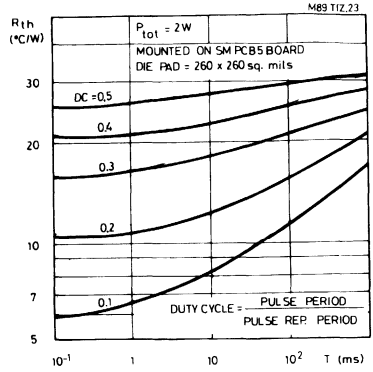


Figure 22 : PLCC68.

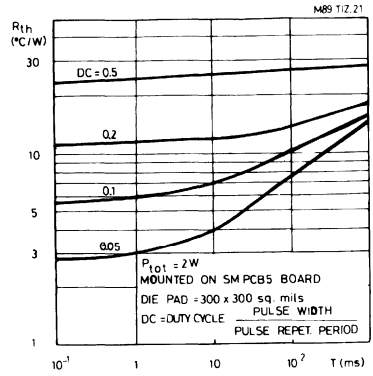
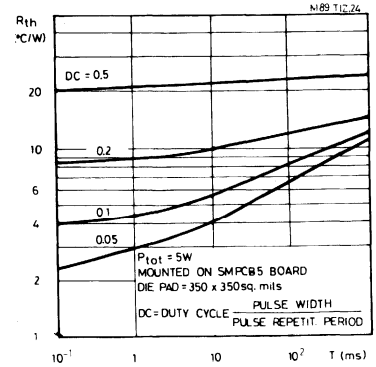


Figure 23 : PLCC84.



THERMAL DATA OF MEDIUM POWER PACKAGES

	$R_{th(j-p)}$ [°C/W] (AVERAGE)	$R_{th(j-a)}$* [°C/W]
SO (12 + 4 + 4)	14	50
PLCC (33 + 11)	12	41

* with 6 sq. cm. on board heat-sink.

JUNCTION TO PINS THERMAL RESISTANCE VS ON DIE DISSIPATING AREA

Figure 24 : SO (12 + 4 + 4).

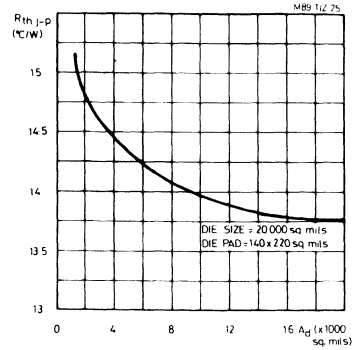
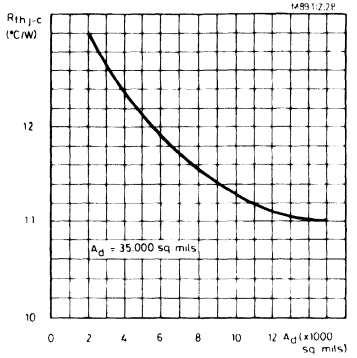
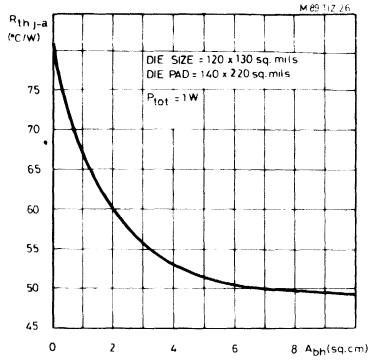


Figure 25 : PLCC (33 + 11).



JUNCTION TO AMBIENT THERMAL RESISTANCE VS AREA ON BOARD HEAT-SINK

Figure 26 : SO (12 + 4 + 4).



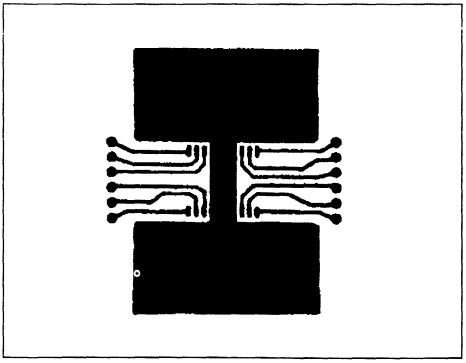
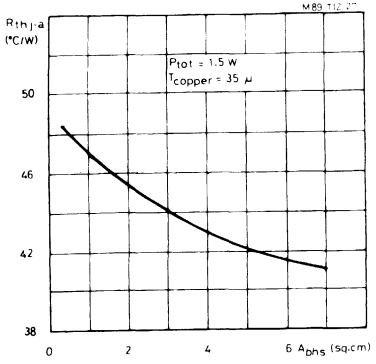
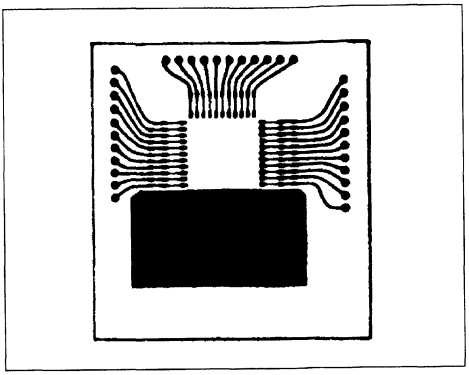


Figure 27 : PLCC (33 + 11).





TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 28 : SO (12 + 4 + 4).

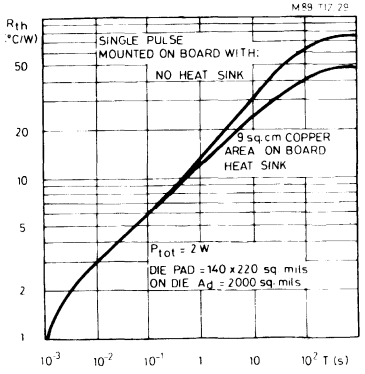
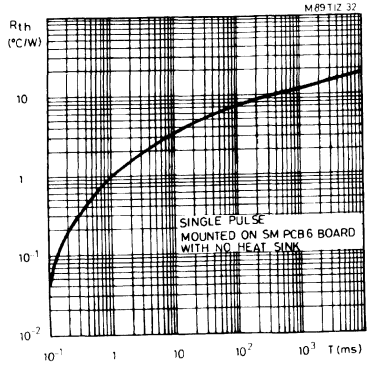
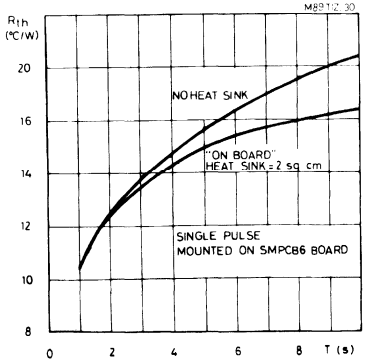


Figure 29 : PLCC (33 + 11).



pulse length = 0.1 – 10ms.

Figure 30 : PLCC (33 + 11).



pulse length = 1 – 10s.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES.

Figure 31 : PLCC (12 + 4 + 4).

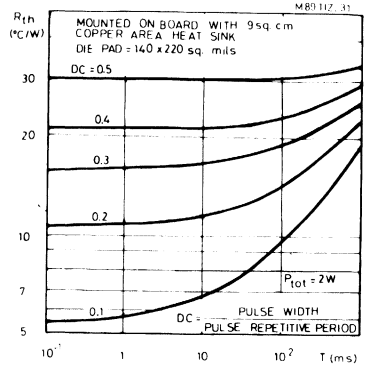
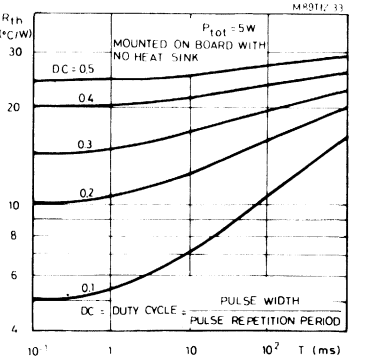


Figure 32 : PLCC (33 + 11).



APPLICATION EXAMPLES OF THERMAL DATA

Good thermal design begins with system and reliability considerations. This turn is based on correct consideration of ambient and device temperature parameters.

The ambient temperature T_a defined for applications can range from 50 to 55°C, as is common in many consumer and computer applications, through to 80°C or more in applications such as automotive systems. The ambient temperature depends on the various heat and cooling sources surrounding the device. An important factor in device lifetime is junction temperature - lifetime is approximately halved when junction temperature T_j is increased by 10°C. The maximum junction temperature commensurate with good reliability, takes into account the activation energy of the failure mechanisms which may differ for various silicon and packaging technologies.

In plastic packages the maximum T_{jmax} is 150°C, but lower values (100 to 120°C) may be specified in high rel applications such as telecoms.

When T_{jmax} and T_a are known, their difference ΔT_j indicates the permissible junction temeperature rise for a given device. For a given power dissipation Pd, the thermal design must ensure that the product Pd x Rth(j-a) is lower than ΔT_j : where $R_{th(j-a)}$ is the thermal resistance of the device from the junction to the ambient at temperature T_a. This takes into consideration the many elements connected to the heat source and includes the leadframe, moulding compound, substrate and heatsink, if used.

EXAMPLE 1 : Maximum dissipation for SO16 packaged device soldered onto an FR4 board (1 oz copper) under the following conditions :

- Ambient temperature : T_a = 70°C
- Maximum Junction Temperature : T_{jmax} = 130°C

The average length of the 12mils wide copper line connected to each pin is 80mils, soldering pads are 30 x 40mils. The total are is thus :

A = [(80 x 12) + 1200 x 16] = 34560sq.mils

SOLUTION

From fig. 13, the value for $R_{th(j-a)}$ is 125°C/W for a copper frame package. Comparing figs. 5 and 6, a value of about 240°C/W can be assumed for Alloy 42 packages. The allowed rise in junction temperature is : ΔT_{jmax} = 130 - 70 = 60°C

Maximum dissipation is given by $\Delta Tjmax/R_{th(j-a)}$.

Therefore :

60/125 = 0.48W for Copper frame

60/240 = 0.25 for Alloy 42 frame

EXAMPLE 2 : Junction temperature for an SO20 packaged device soldered on FR4, under the following conditions :

- Ambient temperature T_a = 70°C
- Dissipated Power Pd = 0.6W

SOLUTION

A total trace-area of 200k sq.mils is assumed,this then gives, from fig. 14 :

- Thermal Resistance $R_{th(j-a)}$ = 90°C/W
- $\Delta T_j = Pd \times R_{th(j-a)}$
- $\Delta T_j = 0.6 \times 90 = 54°C$
- Junction Temperature $T_j = 54 + 70 = 124°C$

EXAMPLE 3 : To determine the size of an integrated heatsink for a medium power application using a PLCC (33 + 11) under the following conditions :

- Ambient temperature T_a = 50°C
- Max. Junction Temperature T_{jmax} = 150°C
- Dissipated Power Pd = 2.2W

SOLUTION

By calculation the application needs an $R_{th(j-a)}$ of : (150 - 50)/2.2 = 45.5°C/W

From figure 32 the on board heatspreader can thus be defined as needing an area of about 2 sq.cm.

EXAMPLE 4 : Given the application described in example 3 determine the maximum pulse width for a single 4W pulse superimposed on a continuous 1.5W dissipation

SOLUTION

The continuous steady state junction temperature at 1.5W dissipation is :

$T_{jss} = (1.5 \times 45.5) + 50 = 118.25°C$

The single pulse is allowed to cause a maximum increase of (150 - 118.25°C) = 31.75°C.

The related transient thermal resistance is (31.75/4) = 7.9°C/W

From figure 33, the corresponding pulse width can be interpreted as being in the order of 200ms.

EXAMPLE 5 : In a medium power application using an SO (12 + 4 + 4) calculate the average junction temperature and the peak temperature for repeated pulses under the following conditions :

- Ambient temperature T_a = 70°C
- On board heatsink area A = 9 sq.cm.
- Pulse length = 100ms
- Pulse height = 5W
- Duty cycle = 20%

SOLUTION

From figure 31, the thermal resistance is found to be 49°C/W. Thus the average junction temperature can be calculated :

$T_{javg} = (5 \times 49 \times 0.2) + 70 = 119°C$

From figure 36, the peak thermal resistance is given as around 15°C/W. The peak temperature can thus be calculated as :

$T_p = (5 \times 15) + 70 = 145$

THERMAL CHARACTERISTICS OF THE MULTIWATT PACKAGE

By R. TIZIANI

INTRODUCTION

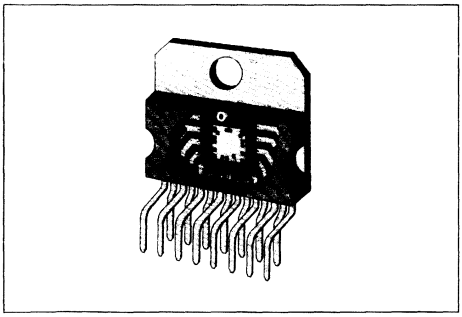
This Application Note provides a complete thermal characterization of the Multiwatt ® package (multilead double TO-220 - fig. 1).

Characterization is performed according with recomandations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repated pulses, with different pulse width and duty cycle ;
4. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Multiwatt Assembly.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 20K mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2K mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package Multiwatt 15 leads

Frame Material	Copper
Slug Thickness	1.5mm
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady stata $R_{th(j-a)}$ can be found, according to pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 especially developed by Thermalloy for the Multiwatt package, whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 3.

It is well known that the main contribution to $R_{th(j-c)}$ of power packages in given by the silicon die.

Figure 2 : Measurement of $R_{th\ (j-c)}$.

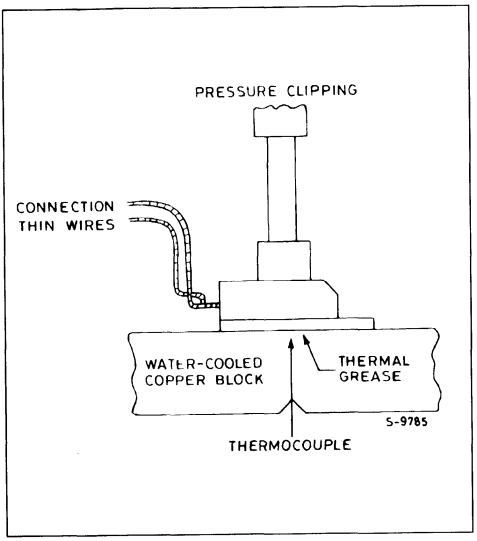
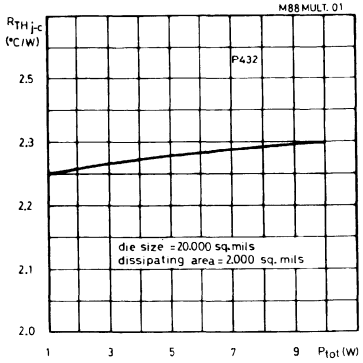


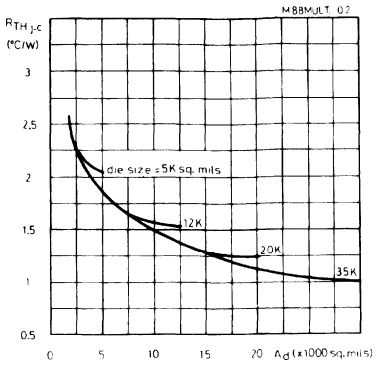
Figure 3 : $R_{th\ (j-c)}$ of Multiwatt Package vs. Power Level.



FOR DEVICES OTHER THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 4 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 4 : $R_{th(j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power applications (1.5-2W), the Multiwatt package can be used without external heat sink, thanks to the significant size (about 3.5cm^2) of its integrated thermal mass.

Its $R_{th(j-a)}$ has two contributions : the $R_{th(j-c)}$, mainly due to the silicon die (as shown in fig. 4) and the thermal resistance of the copper slug $R_{th\ slug}$.

Figure 5 : $R_{th(j-a)}$ of Multiwatt Package vs. dissipated Power.

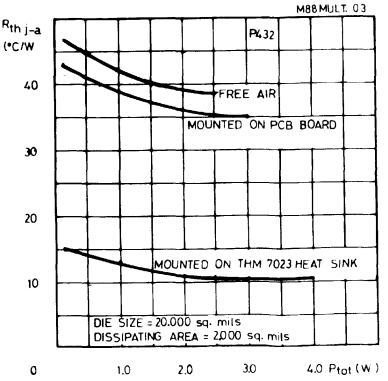


Fig. 5 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern is still air, on PC board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 5 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 4 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED ON PC BOARD.

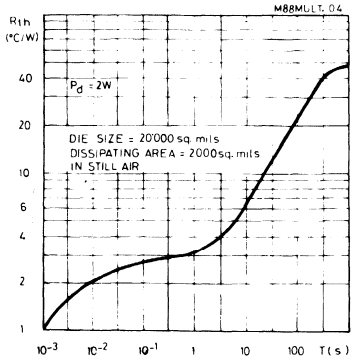
TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height for the Multiwatt package without any external heat sink is shown in fig. 6.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 2J/°C) and correspondingly long risetime (τ = 80s), single pulses up to 30W can be delivered to the Multiwatt package for 1s with acceptable junction temperature increase.

IN ORDER TO HAVE ACCURATE R_{th} (t$_o$ FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Figure 6 : Transient Thermal Resistance for Single Pulse.



Repetition of pulses with defined P_d, period and duty cycle DC (ratio betwen pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 7 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (with external heat sink)

Characterization has been repeated with a commercial heat sink (Thermalloy THM7023) in order to have an example of the effect of an external thermal mass on the impedance of the thermal module.

Relationship between transient R_{th} and pulse length is reported in fig. 8.

The effect of the increased thermal capacitance is evident in fig. 9, where thermal data of fig. 6 and 8 are compared : it can be noticed that the curves are definitely different for pulses longer than 1s, corresponding about to the rise time of the slug. The effect of the thermal mass is to keep low the heating rate of the silicon die thus allowing a better power management of long power pulses. This conclusion has general validity and can be applied to other heat sinks than the one considered in this note.

Figure 7 : Peak Transient R_{th} vs. Pulse width and Duty Cycle.

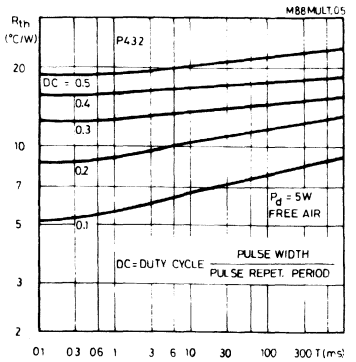


Figure 8 : Transient R_{th} for single pulses, with Heatsink.

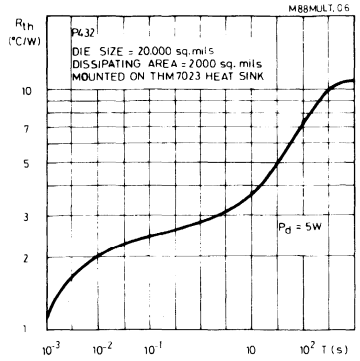
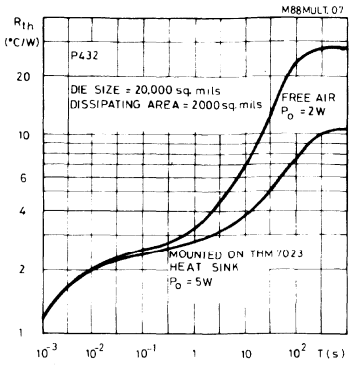


Figure 9 : Comparison of Transient R_{th} for single pulses, with and without Heat Sink.



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sensing diode (fig. A1). The active area is about 2000 $mils^2$ on a 35000$mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

The relationship between the forward voltage V_f of the diode at the constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A1 : Test Pattern P432 Lay-out.

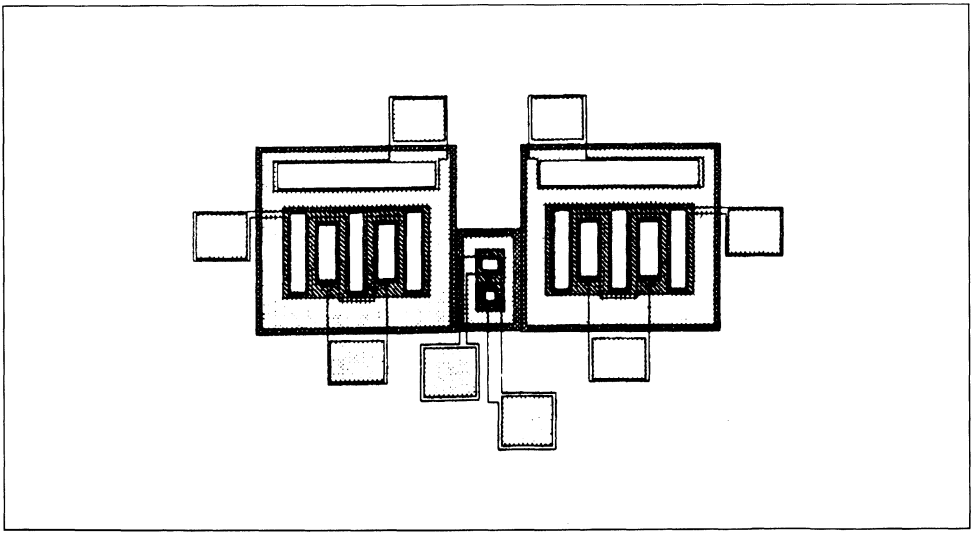


Figure A2 : Calibration Curse (sensing diode).

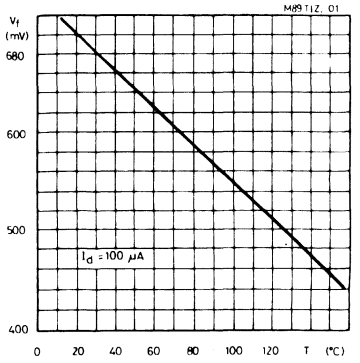
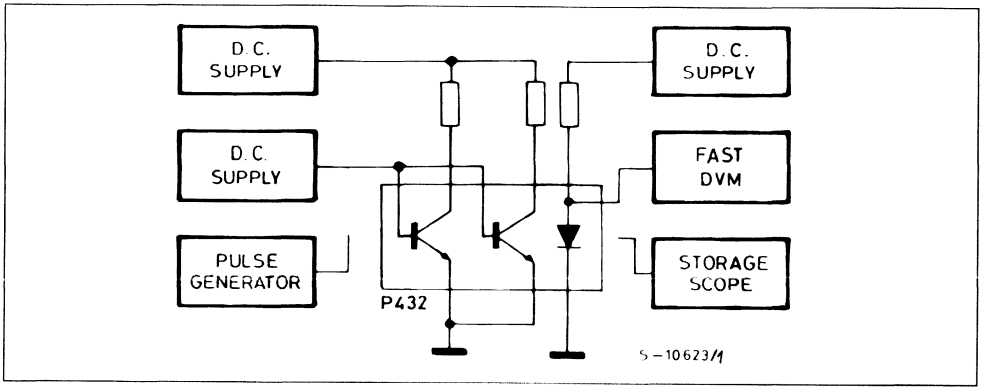


Figure A3 : Measurement Circuits.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (°C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{\gamma}{K \times S}$$

where K is the thermal conductivity of the material, the length of the conductive path and S its section.

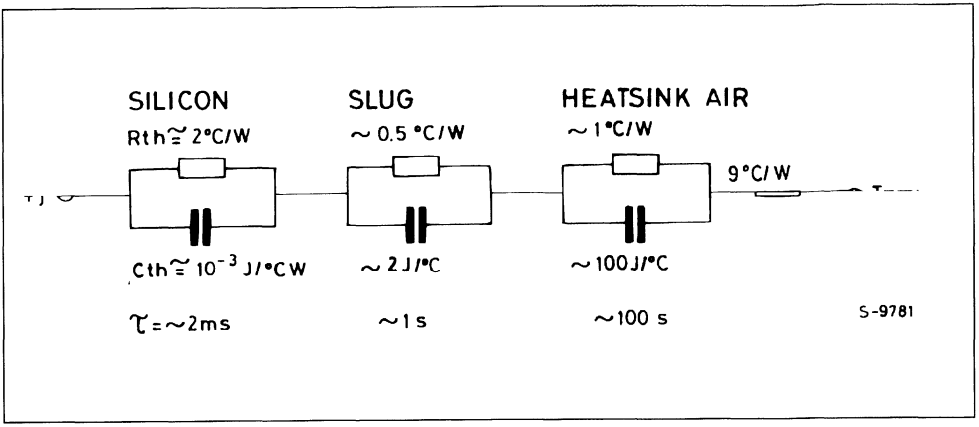
Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Figure B1 : Electrical Equivalent of Multiwatt Package Mounted on the External Heatsink.



Each cell has its own risetime τ , given by the product of the thermal resistance and capacitance :

$$\tau = R_{th_i} \times C_{th}$$

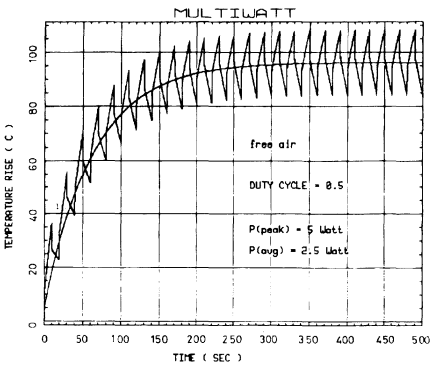
The value of the time constant determines whether a cell approaches equilibrium rapidly of slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \left[1 - e^{-t/r}\right] (1)$$

Typical values of R_{th}, C_{th} and τ for Multiwatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitances while the value reached in the steady state depends on thermal resistances only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

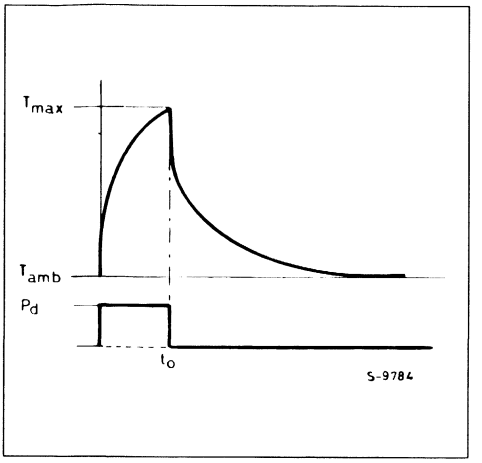
Figure B2 : Qualitative T_j increase (network of fig. B1) for repeated Power Pulse.



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than the steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorted pulses, R_{th} (t_o) is lower and a higher power can be dissipated. without exceeding the maximum junction temperature $T_{j\text{-}max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Multiwatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

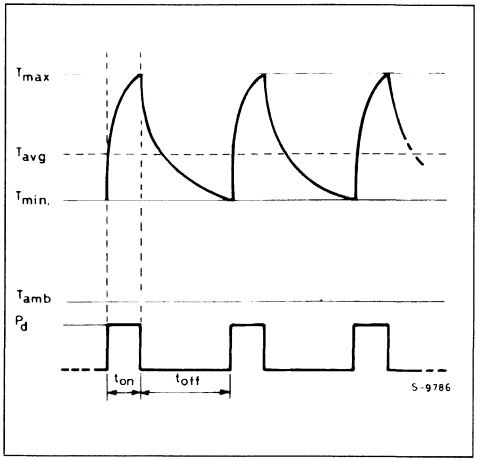
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die (τ_S = 1– 3ms) is able to follow frequencies of some KHz and junction temperature oscillates about the average as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

Figure B4 : Junction Temperature increase for repeated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of Multiwatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 20K mils^2, with dissipating area of 2K mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 39°C/W, Multiwatt package can dissipate about 2W in steady state. From fig. 7 the transient thermal resistance corresponding to one single pulse of 20ms is R_{th} (20ms)$_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area. Practical case : IC having a die size of 35K mils^2 with a dissipating area of 20k mils^2.

SOLUTION : from fig. 5, thermal resistances of P432 and of the IC under consideration are $R_{th\,P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.2°C/W.

As the length of the pulse is 10-15 times longer than the rise time of the silicon, the die (first cell of fig. B1) can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$:

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.2^{\circ}C/W = 1.1^{\circ}C/W$$

A single pulse of 80/1.1 ≅ 72W can be delivered to such device.

When the pulse has the same order of silicon rise time τ P432 is about 1ms) another type of correction is needed. In first approximation, τ increase with dissipating area with the relationship :

$$t_{IC} = \sqrt{20K_{IC}/2K_{P432} \times \tau_{P432}} \cong 3.1ms$$

Expansion of the exponential term of relationship (1) limited to the first term term, is :

$$R_{th\ IC}\ (t_o) \cong R_{th\ P432}\ (t_o)\ /3.1$$

for t_o = 1ms :

$$R_{th\ IC}\ (1ms) = 1.05/3.1^{\circ}C/W \cong 0.34^{\circ}C/W$$

A single pulse of 80/0.34 ≅ 235W can be delivered to such device.

EXAMPLE 3 – R_{th} WITH REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Multiwatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C, maximum temperature is allowed to be 125°C.

SOLUTION : a maximum ΔT = 75°C has to be considered. Fig. 5 indicated that for a pulse width of 10ms and a duty cycle of 0.1, $R_{th\ peak}$ is 6.7°C/W. Maximum P_d is 75/6.7 = 11.2W, with an average temperature increase ΔT_{peak} of 39 x 0.1 x 11.2 ≅ 43°C.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

THERMAL CHARACTERISTICS OF THE PENTAWATT-HEPTAWATT PACKAGES

By R. TIZIANI

INTRODUCTION

This Application Note is aimed to give a complete thermal characterization of the Heptawatt and Pentawatt package (fig. 1, 2).

Characterization is performed according with recomendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repeated pulses, with different pulse width and duty cycle ;
4. thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Pentawatt.

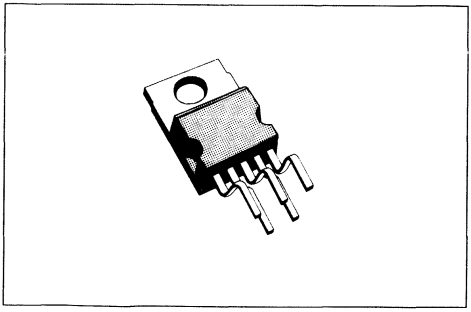
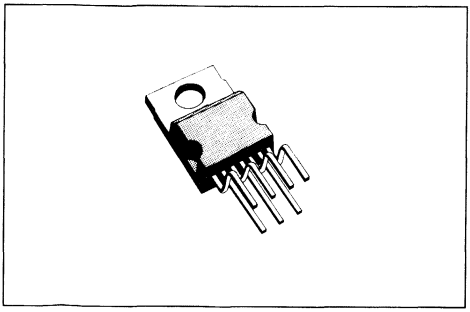


Figure 2 : Heptawatt.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 15k mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2k mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package	Pentawatt - Heptawatt
Frame Material	Copper
Slug Thickness	1.25mm Typ.
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 3. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady state $R_{th(j-a)}$ can be found, according with pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 (Thermalloy) whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all of the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 4. The absolute value and the behaviour with the dissipated power are the same for

both packages as the slug thickness and the die - attach are equal.

Figure 3 : Measurement of $R_{th\ (j-c)}$.

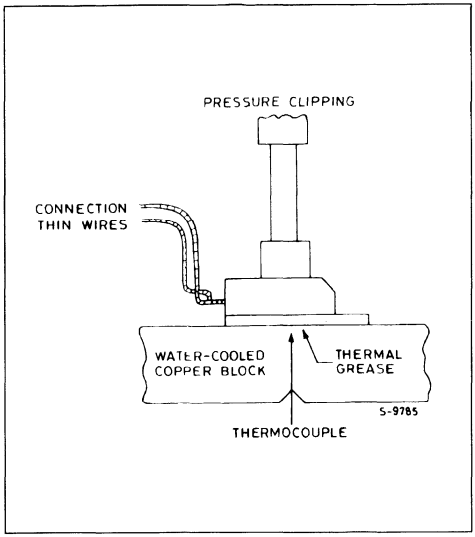
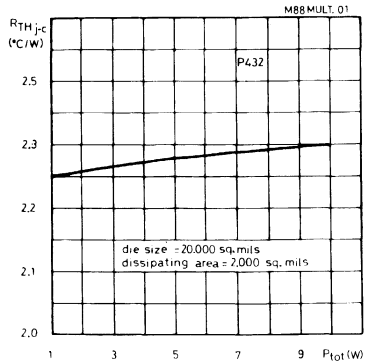


Figure 4 : $R_{th\ (j-c)}$ of Pentawatt and Heptawatt Package vs. Power Level.

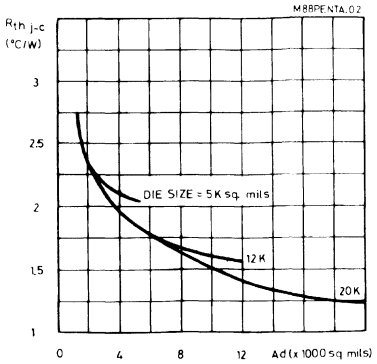


It is well known that the main contribution to $R_{th(j-c)}$ of power packages is given by the silicon die.

FOR OTHER DEVICES THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 5 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 5 : $R_{th\ (j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power application (1W), the Pentawatt and Heptawatt packages can be used without external heat sink thanks to the significant size (about 1.5cm^2) of its integrated thermal mass.

An effective cost solution for higher power application (1.5-2.0W) is using a copper area heat sink.

An board with the external leads bent down as shown in fig. 7.

Fig. 6 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern in still air, on PC board, on integrated heat sink on board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 6 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 5 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED IN PC BOARD.

Figure 6 : $R_{th\ (j\text{-}a)}$ vs. dissipated Power (heptawatt).

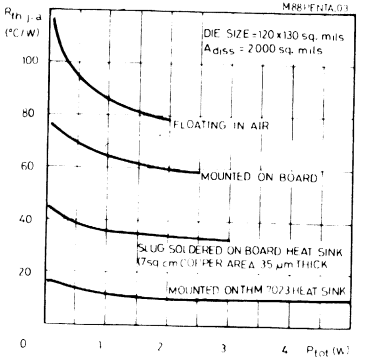
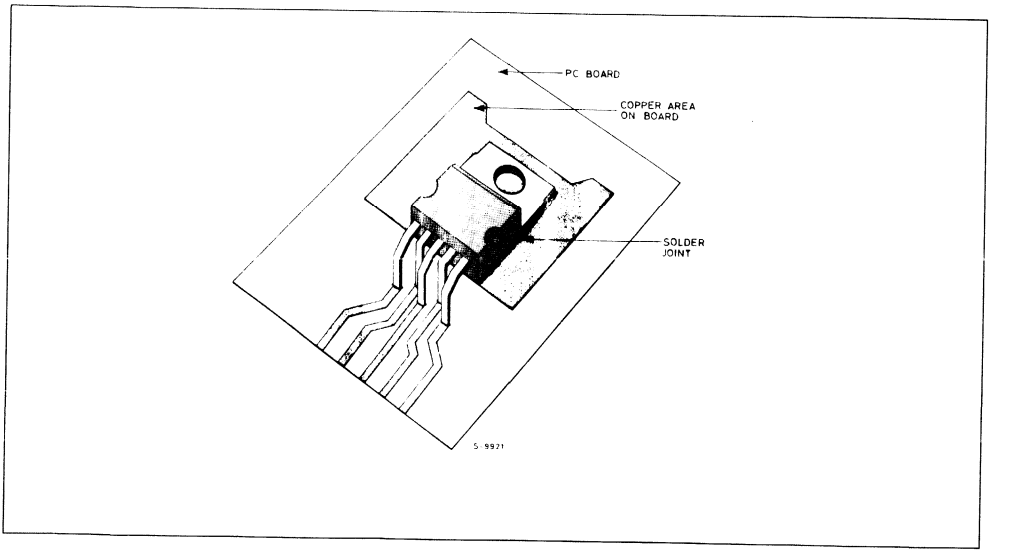


Figure 7 : Pentawatt Soldered on Copper Heatsink on P.C Board.

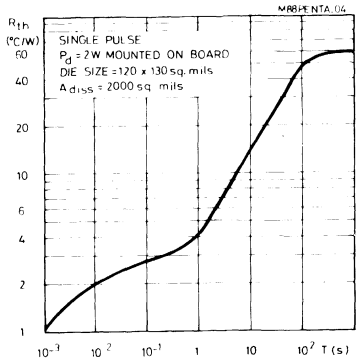


TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height without any external heat sink is shown in fig. 8.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 1J/°C) and a correspondingly long risetime (τ = 80s), single pulses up to 20W can be delivered for 1 s with acceptable junction temperature increase.

Figure 8 : Transient Thermal Resistance for Single Pulses (heptawatt).

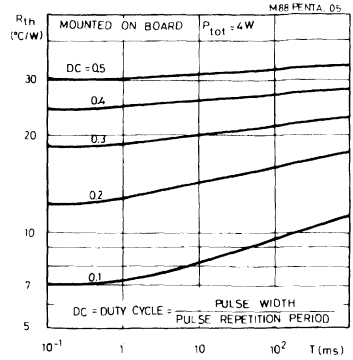


IN ORDER TO HAVE ACCURATE $R_{th}(t_o)$ FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Repetition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 9 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

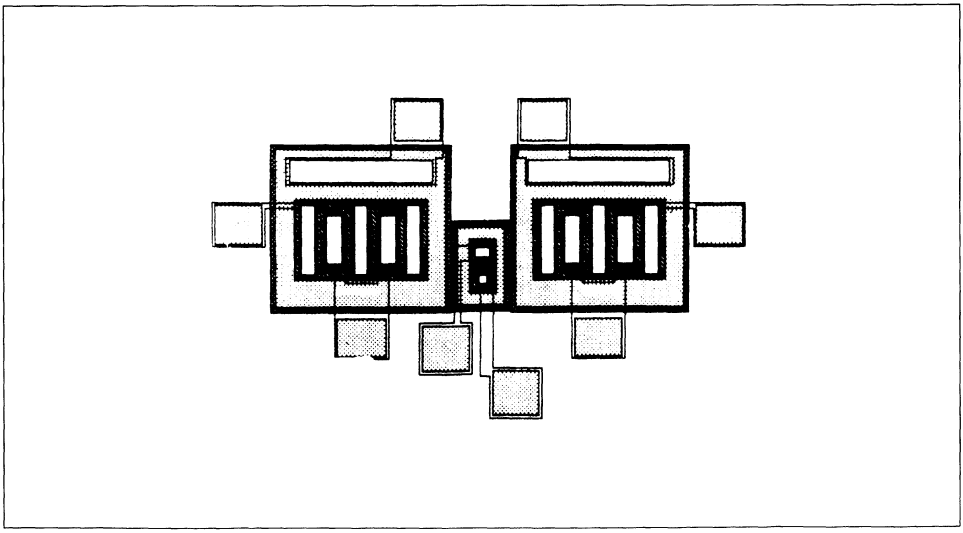
Figure 9 : Peak Transient R_{th} vs Pulse width and Duty Cycle (heptawatt).



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sending diode (fig. A1). The active area is about 2000 $mils^2$ on a 15000 $mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

Figure A1 : Test Pattern P432 Lay-out.



The relationship between the forward voltage V_f of the diode at a constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A2 : Calibration Curve (sensing diode).

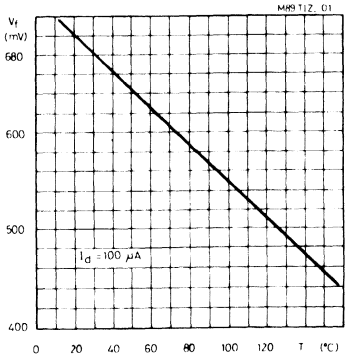
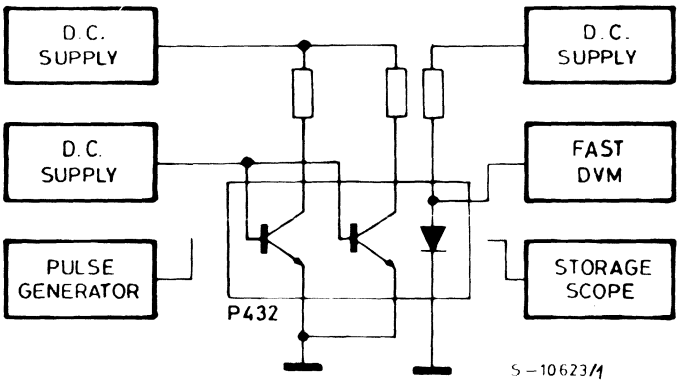


Figure A3 : Measurement Circuit.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

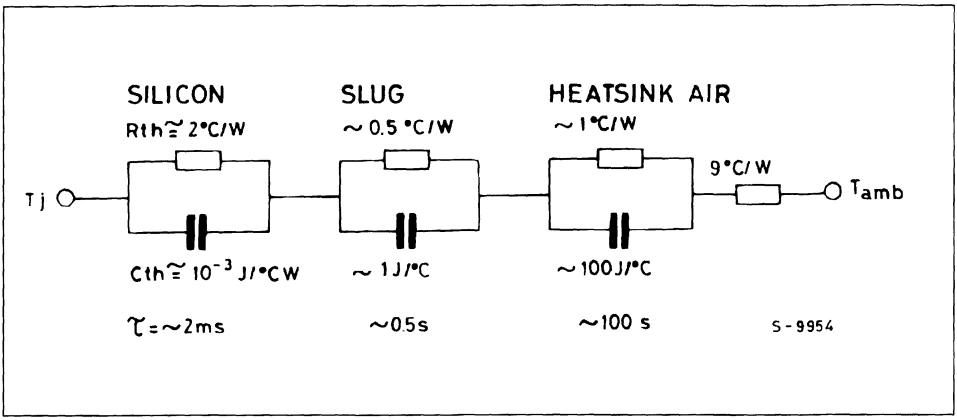
The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink Rth can be calculated from the relationship :

$$R_{th} = \frac{1}{K \times S}$$

Where K is the thermal conductivity of the material, 1 the length of the conductive path and S its section.

Figure B1 : Electrical Equivalent of Pentawatt and Heptawatt Package mounted on the External Heatsink.



Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Each cell has its own risetime τ, given by the product of thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

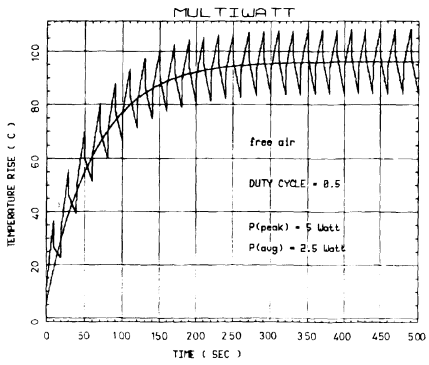
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \times [1 - e^{-t/\tau}] \quad (1)$$

Typical values of R_{th}, C_{th} and τ for Heptawatt and Pentawatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitance while the value reached in the steady state depends on thermal resistance only. Qualitative beahaviour of the network of fig. B1 is shown in fig. B2.

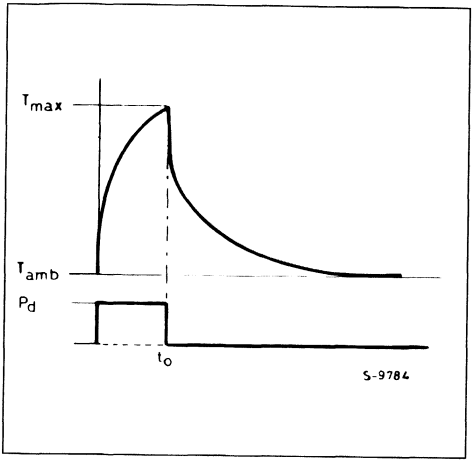
Figure B2 : Qualittative T_j increase (network of fig. B1) for repeated power pulse (heptawatt).



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorter pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\,max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Heptawatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height Pd are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = Pd \times DC$$

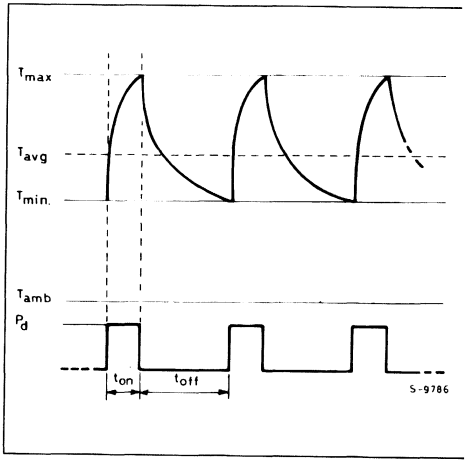
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times Pd_{avg} = R_{th} \times Pd \times DC$$

On the other hand, the silicon die ($\tau_{SI} = 1 \div 2$ms) is able to follow frequencies of some kHz and junction temperature oscillates about the average, as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known Pd_{max} is derived from the same figure.

Figure B4 : Junction Temperature increase for operated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM Pd FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum Pd for a single pulse with a length of 20ms in the case of Heptawatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 15k mils^2, with dissipating area of 2k mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 60°C/W, Heptawatt package can dissipate about 1.3W in steady state From fig. 8 the transient thermal resistance corresponding to one single pulse of 20ms in R_{th} (20ms)$_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area.

Pratical case : IC having a die size of 15k mils^2 with a dissipating area of 10k mils^2.

SOLUTION : from fig. 5, thermal resistance of P432 and of the IC under consideration are $R_{th\ P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.5°C/W.

As the length of the pulse is 10-15 times longer than the risetime of the silicon, the die (first cell of fig. B1)

can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$.

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.5^{\circ}C/W = 1.4^{\circ}C/W$$

A single pulse of 80/1.4 ≡ 57W can be delivered to such a device.

EXAMPLE 3 - CORRECTION FOR SINGLE PULSES OF 1–3ms

PROBLEM : Correct the results of example 2, for pulse length of 1ms.

SOLUTION : when the pulse has the same order of magnitude of silicon rise time (τ_{P432} is about 1ms) another type of correction is needed. In first approximation it is considered that remains constant when the dissipating area gets higher and the Rth for the silicon die decreases as the reciprocal of the dissipating area. From relationship (1) :

$\Delta T = R_{th}\ (1ms)_{P432} \times 2K/10K \times Pd \times [1 - e^{-t/\tau}]$ for t_o = 1ms :

$$R_{thIC}\ (1ms) = 1.05/0.5^{\circ}C/W \equiv 0.21^{\circ}C/W$$

A single pulse of 80/0.21 ≡ 380W can be delivered to such a device.

EXAMPLE 4 - Rth REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Heptawatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C. maximum temperature is allowed to be 125°C.

SOLUTION : a maximum $\Delta T = 75^{\circ}C$ has to be considered. Fig. 9 indicated that for a pulse width of 10ms and a duty cycle of 0.1, Rth_{peak} is 8.5°C/W. Maximum Pd is 75/8.5 = 8.8W, with an average temperature increase ΔT_{peak} of 60 x 0.1 x 8.8 ≡ 68°C.

REFERENCES

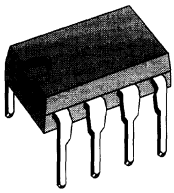
"Improved thermal evaluation, by means of a simple integrated structure" T. Hopkins, C. Cognetti, R. Tiziani - SEMI THERM (USA, 1986).

PACKAGES

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



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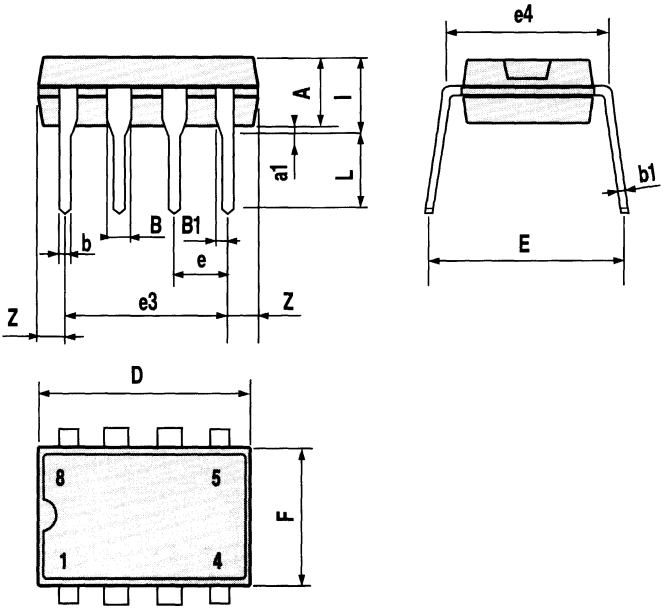
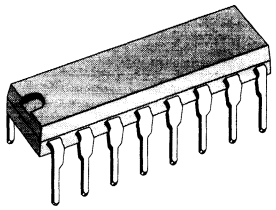


P001W

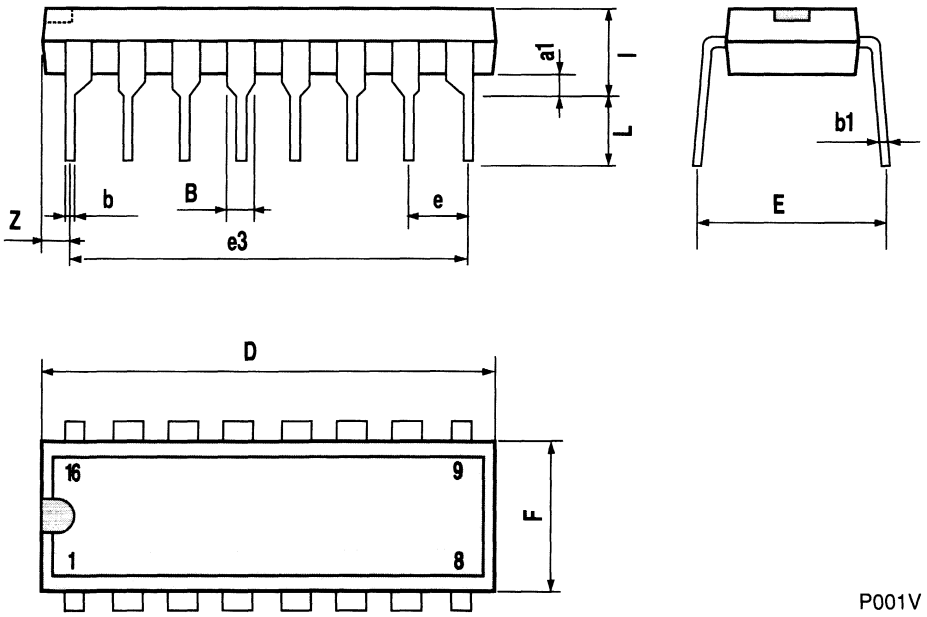
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (8+8), (12+2+2)

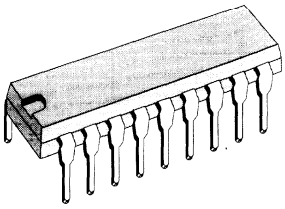


P001V

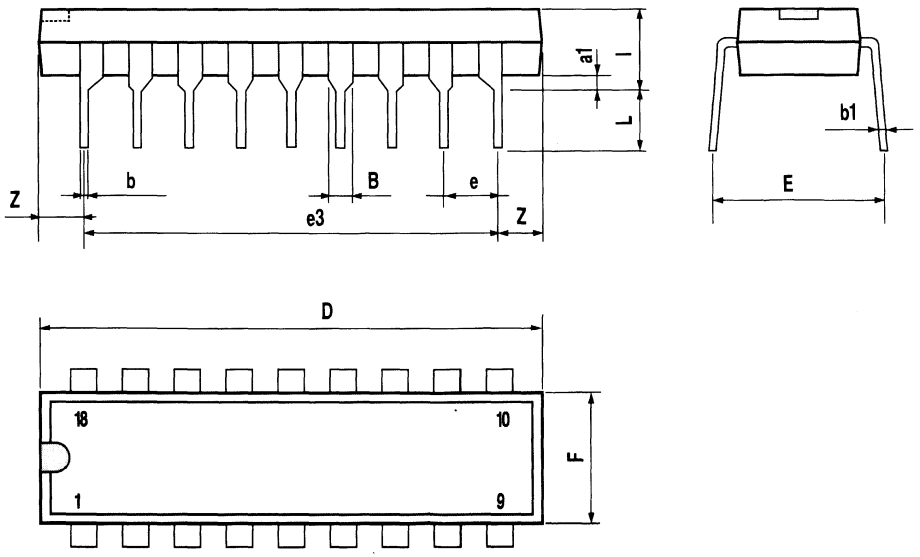
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			2.54			0.100

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP: (9+9), (12+3+3)

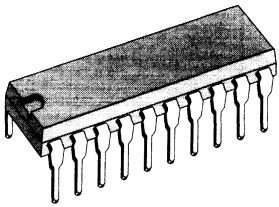


P001U

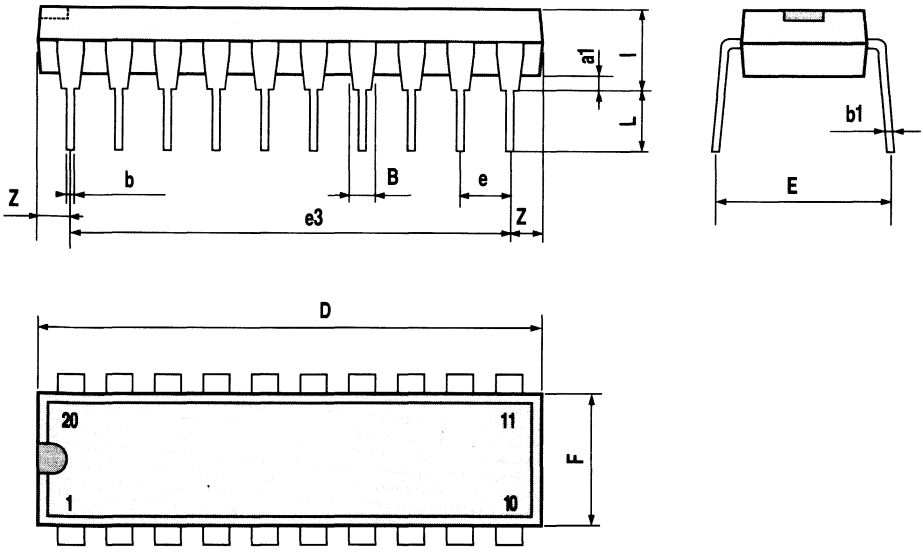
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

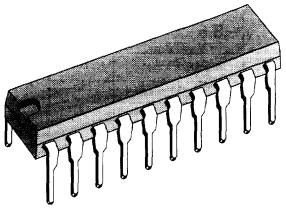


P001J

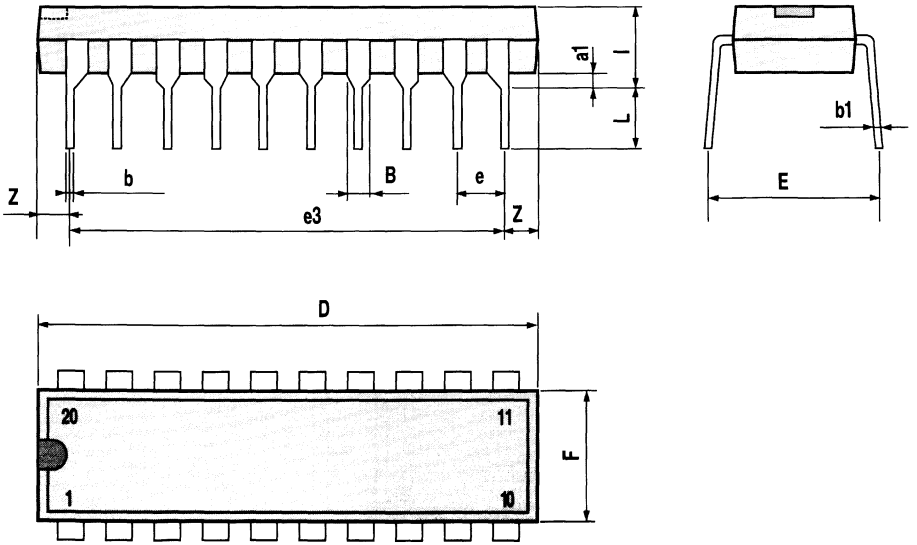
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



POWERDIP (16+2+2)

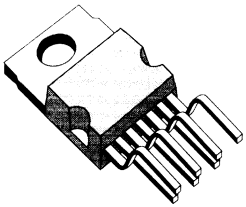


P001X

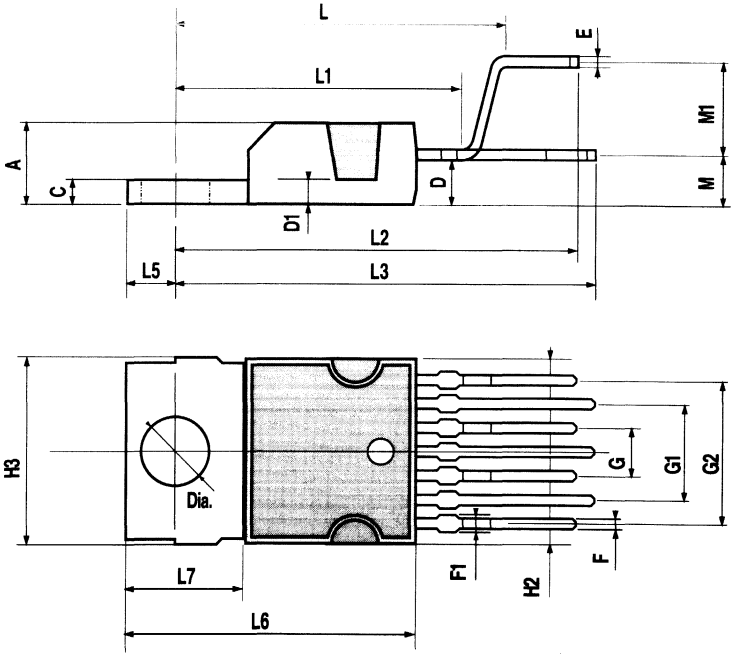
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Heptawatt V

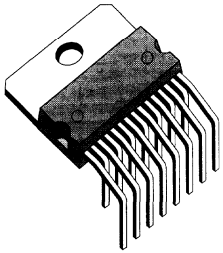


P023A

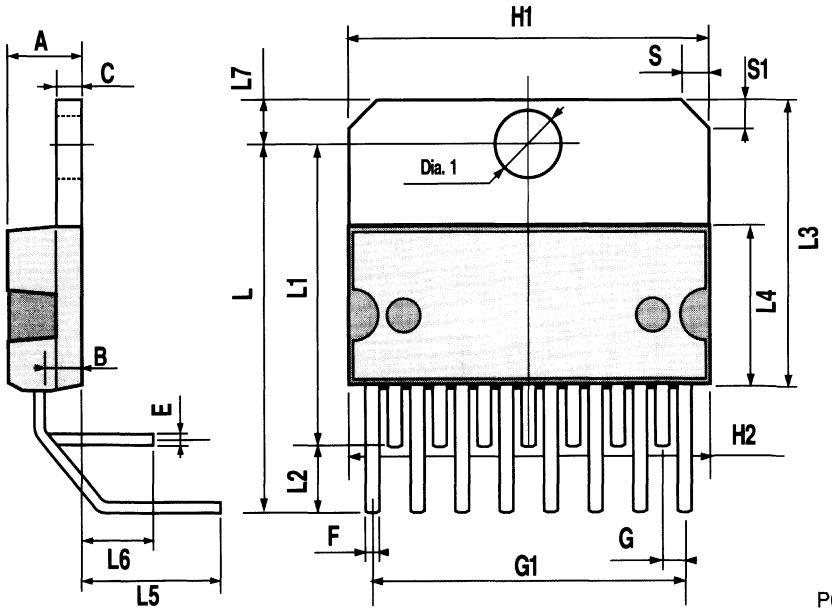
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Multiwatt15 H

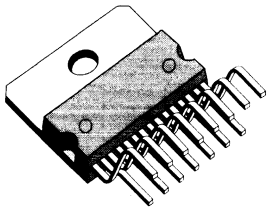


P017H

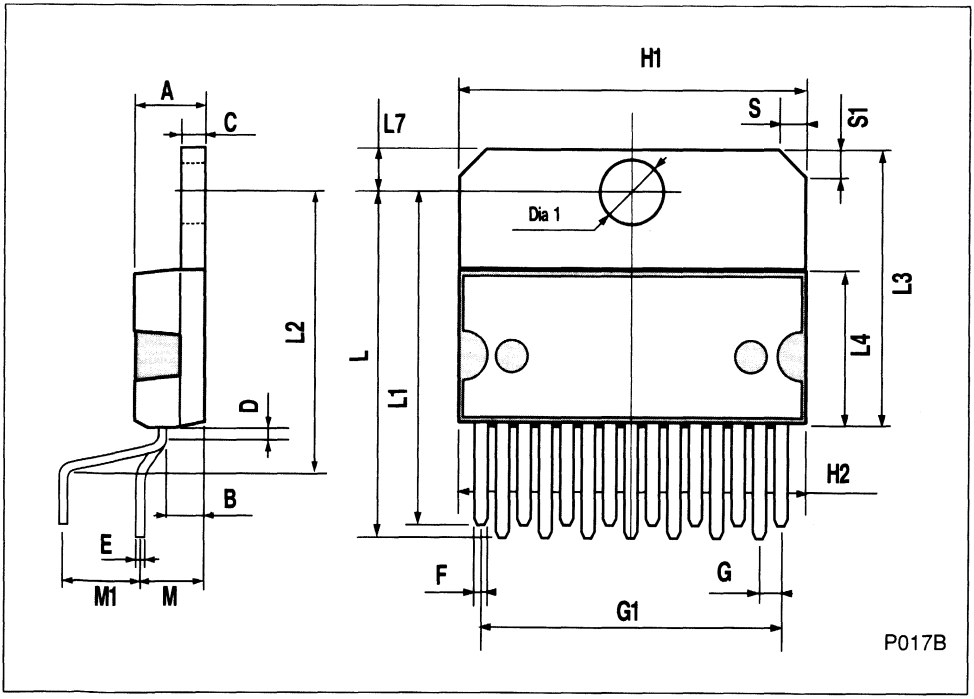
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



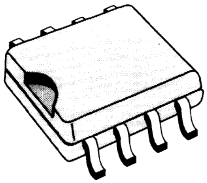
Multiwatt15 V



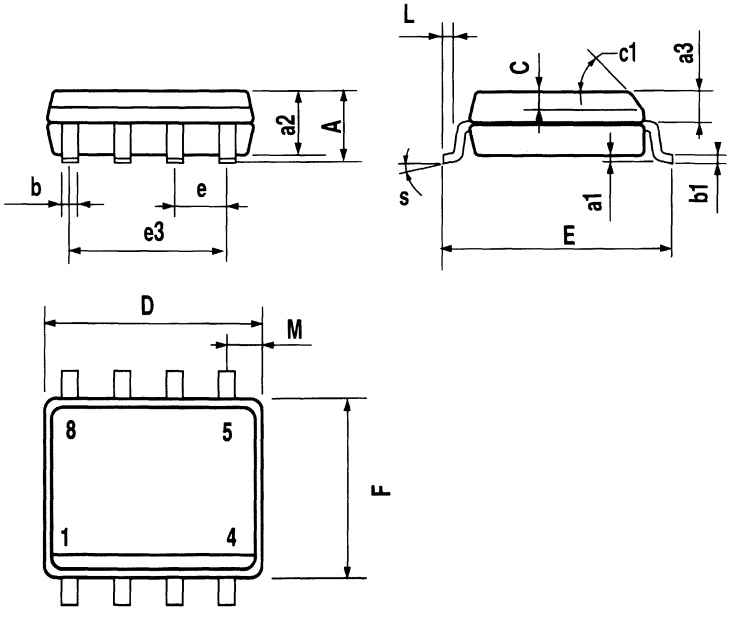
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO8

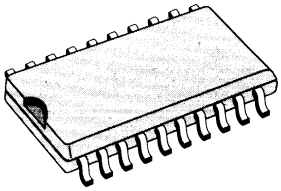


P013M

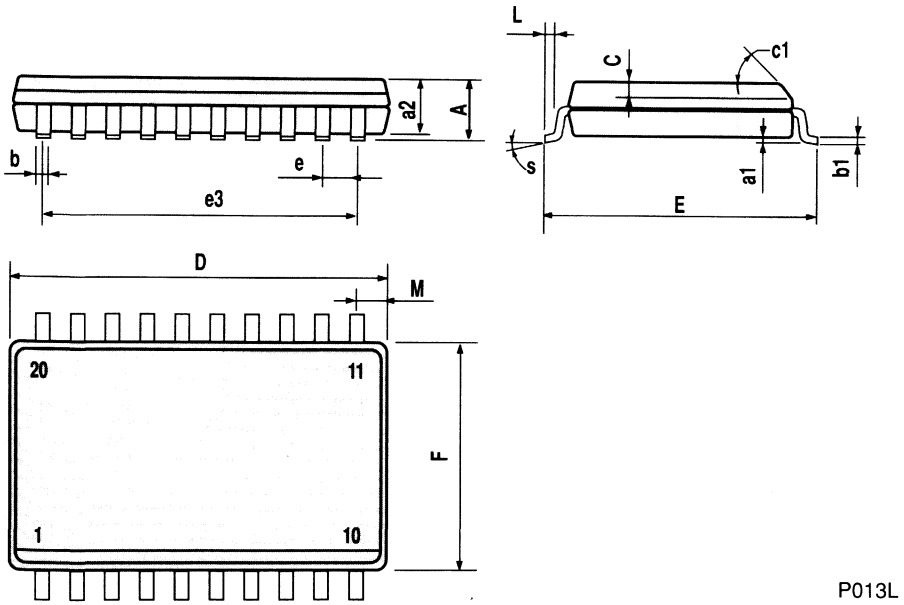
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20



P013L

EUROPE

DENMARK

2730 HERLEV
Herlev Torv, 4
Tel. (45-44) 94.85.33
Telex: 35411
Telefax: (45-44) 948694

FINLAND

LOHJA SF-08150
Ratakatu, 26
Tel. (358-12) 155.11
Telefax. (358-12) 155.66

FRANCE

94253 GENTILLY Cedex
7 - avenue Gallieni - BP. 93
Tel.: (33-1) 47.40.75.75
Telex: 632570 STMHQ
Telefax: (33-1) 47.40.79.10

67000 STRASBOURG
20, Place des Halles
Tel. (33-88) 75.50.66
Telefax: (33-88) 22.29.32

GERMANY

85630 GRASBRUNN
Bretonischer Ring 4
Postfach 1122
Tel.: (49-89) 460060
Telefax: (49-89) 4605454
Teletex: 897107=STDISTR

60327 FRANKFURT
Gutleutstrasse 322
Tel. (49-69) 237492-3
Telefax: (49-69) 231957
Teletex: 6997689=STVBF

30695 HANNOVER 51
Rotenburger Strasse 28A
Tel. (49-511) 615960-3
Teletex: 5118418 CSFBEH
Telefax: (49-511) 6151243

90441 NÜRNBERG 20
Erlenstegenstrasse, 72
Tel.: (49-911) 59893-0
Telefax: (49-911) 5980701

70499 STUTTGART 31
Mittlerer Pfad 2-4
Tel. (49-711) 13968-0
Telefax: (49-711) 8661427

ITALY

20090 ASSAGO (MI)
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel. (39-2) 57546.1 (10 linee)
Telex: 330131 - 330141 SGSAGR
Telefax: (39-2) 8250449

40033 CASALECCHIO DI RENO (BO)
Via R. Fucini, 12
Tel. (39-51) 593029
Telex: 512442
Telefax: (39-51) 591305

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Via A. Torlonia, 15
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Telex: 620653 SGSATE I
Telefax: (39-6) 8444474

NETHERLANDS

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Meerenakkerweg 1
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Telex: 51186
Telefax: (31-40) 528835

SPAIN

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Telefax: (34-3) 2021461

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Calle Albacete, 5
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Telex: 46033 TCCEE
Telefax: (34-1) 4031134

SWEDEN

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Telefax: (46-8) 7504950

SWITZERLAND

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Telefax: (41-22) 7984869

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Globe Park
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R. Henrique Schaumann 286-CJ33
Tel. (55-11) 883-5455
Telex: (391)11-37988 "UMBR BR"
Telefax : (55-11) 282-2367

CANADA

NEPEAN ONTARIO K2H 9C4
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Suite 307
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U.S.A.

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Tel. (61-2) 5803811
Telefax: (61-2) 5806440

HONG KONG

WANCHAI
22nd Floor - Hopewell centre
183 Queen's Road East
Tel. (852) 8615788
Telex: 60955 ESGIES HX
Telefax: (852) 8656589

INDIA

NEW DELHI 110019
Liaison Office
3rd Floor, F-Block
International Trade Tower
Nehru Place
Tel. (91-11) 644-5928/647-9415
Telex: 031-70193 STMI IN
Telefax: (91-11) 6424615

MALAYSIA

SELANGOR, PETALING JAYA 46200
Unit BM-10
PJ Industrial Park
Jalan Kemajuan 12/18
Tel.: (03) 758 1189
Telefax: (03) 758 1179

PULAU PINANG 10400
4th Floor - Suite 4-03
Bangunan FOP-123D Jalan Anson
Tel. (04) 379735
Telefax (04) 379816

KOREA

SEOUL 121
8th floor Shinwon Building
823-14, Yuksam-Dong
Kang-Nam-Gu
Tel. (82-2) 553-0399
Telex: SGSKOR K29998
Telefax: (82-2) 552-1051

SINGAPORE

SINGAPORE 2056
28 Ang Mo Kio - Industrial Park 2
Tel. (65) 4821411
Telex: RS 55201 ESGIES
Telefax: (65) 4820240

TAIWAN

TAIPEI
12th Floor
325, Section 1 Tun Hua South Road
Tel. (886-2) 755-4111
Telex: 10310 ESGIE TW
Telefax: (886-2) 755-4008

JAPAN

TOKYO 108
Nisseki - Takanawa Bld. 4F
2-18-10 Takanawa
Minato-Ku
Tel. (81-3) 3280-4121
Telefax: (81-3) 3280-4131